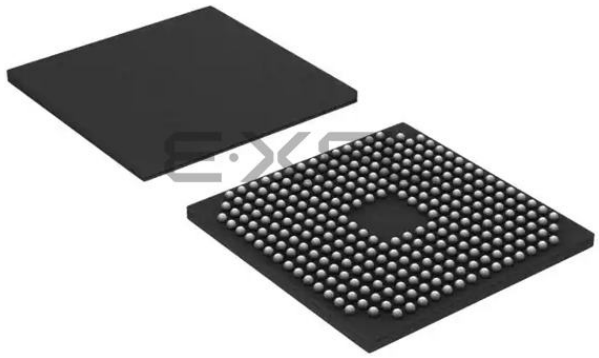

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3240fet296-01-5

- Multi-layer AHB system that provides a separate bus for each AHB master, including both an instruction and data bus for the CPU, two data busses for the DMA controller, and another bus for the USB controller, one for the LCD, and a final one for the Ethernet MAC. There are no arbitration delays in the system unless two masters attempt to access the same slave at the same time.
- External memory controller for DDR and SDR SDRAM as well as for static devices.
- Two NAND flash controllers: One for single-level NAND flash devices and the other for multi-level NAND flash devices.
- Master Interrupt Controller (MIC) and two Slave Interrupt Controllers (SIC), supporting 74 interrupt sources.
- Eight channel General Purpose DMA (GPDMA) controller on the AHB that can be used with the SD card port, the high-speed UARTs, I^2S-bus interfaces, and SPI interfaces, as well as memory-to-memory transfers.
- Serial interfaces:
  - 10/100 Ethernet MAC with dedicated DMA Controller.
  - USB interface supporting either device, host (OHCI compliant), or On-The-Go (OTG) with an integral DMA controller and dedicated PLL to generate the required 48 MHz USB clock.
  - Four standard UARTs with fractional baud rate generation and 64 byte FIFOs. One of the standard UARTs supports IrDA.
  - Three additional high-speed UARTs intended for on-board communications that support baud rates up to 921 600 when using a 13 MHz main oscillator. All high-speed UARTs provide 64 byte FIFOs.
  - Two SPI controllers.
  - Two SSP controllers.
  - Two I^2C-bus interfaces with standard open-drain pins. The I^2C-bus interfaces support single master, slave, and multi-master I^2C-bus configurations.
  - Two I^2S-bus interfaces, each with separate input and output channels. Each channel can be operated independently on three pins, or both input and output channels can be used with only four pins and a shared clock.
- Additional peripherals:
  - LCD controller supporting both STN and TFT panels, with dedicated DMA controller. Programmable display resolution up to 1024×768.
  - Secure Digital (SD) memory card interface, which conforms to the *SD Memory Card Specification Version 1.01*.
  - General Purpose (GP) input, output, and I/O pins. Includes 12 GP input pins, 24 GP output pins, and 51 GP I/O pins.
  - 10-bit, 400 kHz Analog-to-Digital Converter (ADC) with input multiplexing from three pins. Optionally, the ADC can operate as a touch screen controller.
  - Real-Time Clock (RTC) with separate power pin and dedicated 32 kHz oscillator. NXP implemented the RTC in an independent on-chip power domain so it can remain active while the rest of the chip is not powered. The RTC also includes a 32-byte scratch pad memory.
  - 32-bit general purpose high-speed timer with a 16-bit pre-scaler. This timer includes one external capture input pin and a capture connection to the RTC clock. Interrupts may be generated using three match registers.

4. Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
LPC3220FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3230FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3240FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3250FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1

[1] F = −40 °C to +85 °C temperature range. Note that Revision “A” parts with and without the /01 suffix are identical. For example, LPC3220FET296 Revision “A” is identical to LPC3220FET296/01 Revision “A”.

[2] Available starting with Revision “A”.

4.1 Ordering options

Table 2. Part options

Type number	SRAM (kB)	10/100 Ethernet	LCD controller	Temperature range (°C)	Package
LPC3220FET296/01	128	0	0	−40 to +85	TFBGA296
LPC3230FET296/01	256	0	1	−40 to +85	TFBGA296
LPC3240FET296/01	256	1	0	−40 to +85	TFBGA296
LPC3250FET296/01	256	1	1	−40 to +85	TFBGA296

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
VDD_IOC	F7, G6, H6, J5	VDD_IOC	power	1.8 V or 3.3 V supply for IOC domain
VDD_IOD	F13, F9	VDD_IOD	power	1.8 V to 3.3 V supply for IOD domain
VDD_OSC	T18	VDD_OSC	power	1.2 V supply for main oscillator
VDD_PLL397	T16	VDD_PLL397	power	1.2 V supply for 397x PLL
VDD_PLLHCLK	R17	VDD_PLLHCLK	power	1.2 V supply for HCLK PLL
VDD_PLLUSB	P15	VDD_PLLUSB	power	1.2 V supply for USB PLL
VDD_FUSE	N14	VDD_FUSE	power	1.2 V supply
VDD_RTC	K14	VDD_RTC	power	1.2 V supply for RTC I/O
VDD_RTCCORE	L13	VDD_RTCCORE	power	1.2 V supply for RTC
VDD_RTCOSC	N15	VDD_RTCOSC	power	1.2 V supply for RTC oscillator
VSS_AD	P13	-	power	Ground for ADC/touch screen
VSS_CORE	G8, G10, G12, H7, K12, L7, M9, M10, M12	-	power	Ground for core
VSS_EMC	K5, L5, M5, N5, N6, P6, P7, P8, P9, P10, P11	-	power	Ground for EMC
VSS_IOA	K13	-	power	Ground VDD_IOA domain
VSS_IOB	F6	-	power	Ground VDD_IOB domain
VSS_IOC	F5, G5, H5	-	power	Ground VDD_IOC domain
VSS_IOD	F10, F11, F12, H12	-	power	Ground VDD_IOD domain
VSS_OSC	P14	-	power	Ground for main oscillator
VSS_PLL397	T15	-	power	Ground for 397x PLL
VSS_PLLHCLK	R18	-	power	Ground for HCLK PLL

Table 6. Supply domains

Supply domain	Voltage range	Related supply pins	Description
VDD_IOA[1]	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOA	Peripheral supply.
VDD_IOB[1]	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOB	Peripheral supply.
VDD_IOC[1]	1.7 V to 1.95 V or 2.3 V to 3.6 V	VDD_IOC	Peripheral supply.
VDD_IOD[1]	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOD	Peripheral supply.

[1] The VDD_IOA, VDD_IOB, VDD_IOC, and VDD_IOD supply domains can be operated at a voltage independent of the other domains as long as all pins connected to the same peripheral are at the same voltage level. There are two special cases for determining supply domain voltages (for details see *application note AN10777*):

a) Ethernet configured in MII mode: VDD_IOD must be the same as VDD_IOB.

b) UART 3 when used with hardware flow control or when sharing an RS-232 transceiver with another UART: VDD_IOA must be the same as VDD_IOD.

7.5.1.2 Single-Level Cell (SLC) NAND flash controller

The SLC NAND flash controller interfaces to single-level NAND flash devices. DMA page transfers are supported, including a 20-byte DMA read and write FIFO. Hardware support for ECC (Error Checking and Correction) is included for the main data area. Software can correct a single bit error.

7.5.2 SD card controller

The SD interface allows access to external SD memory cards. The SD card interface conforms to the *SD Memory Card Specification Version 1.01*.

7.5.2.1 Features

- 1-bit and 4-bit data line interface support.
- DMA is supported through the system DMA controller.
- Provides all functions specific to the SD memory card. These include the clock generation unit, power management control, command and data transfer.

7.5.3 External memory controller

The LPC3220/30/40/50 includes a memory controller that supports data bus SDRAM, DDR SDRAM, and static memory devices. The memory controller provides an interface between the system bus and external (off-chip) memory devices.

The controller supports 16-bit and 32-bit wide SDR SDRAM devices of 64 Mbit, 128 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit sizes, as well as 16-bit wide data bus DDR SDRAM devices of 64 Mbit, 128 Mbit, 128 Mbit, 256 Mbit, and 512 Mbit sizes. Two dynamic memory chip selects are supplied, supporting two groups of SDRAM:

- DYCS0 in the address range 0x8000 0000 to 0x9FFF FFFF
- DYCS1 in the address range 0xA000 0000 to 0xBFFF FFFF

The memory controller also supports 8-bit, 16-bit, and 32-bit wide asynchronous static memory devices, including RAM, ROM, and flash, with or without asynchronous page mode. Four static memory chip selects are supplied for SRAM devices:

- CS0 in the address range 0xE000 0000 to 0xE0FF FFFF
- CS1 in the address range 0xE100 0000 to 0xE1FF FFFF
- CS2 in the address range 0xE200 0000 to 0xE2FF FFFF
- CS3 in the address range 0xE300 0000 to 0xE3FF FFFF

The SDRAM controller uses three data ports to allow simultaneous requests from multiple on-chip AHB bus masters and has the following features.

- Dynamic memory interface supports SDRAM, DDR-SDRAM, and low-power variants.
- Read and write buffers to reduce latency and improve performance.
- Static memory features include
  - asynchronous page mode read
  - programmable wait states
  - bus turnaround cycles
  - output enable and write enable delays

  - extended wait
- Power-saving modes dynamically control EMC_CKE[1:0] and EMC_CLK.
- Dynamic memory self-refresh mode supported by software.
- Controller supports 2 k, 4 k, and 8 k row address synchronous memory parts. That is, typical 512 MB, 256 MB, 128 MB, and 16 MB parts, with 8, 16, or 32 data bits per device.
- Two reset domains enable dynamic memory contents to be preserved over a soft reset.
- This controller does not support synchronous static memory devices (burst mode devices).

7.6 AHB master peripherals

The LPC3220/30/40/50 implements four AHB master peripherals, which include a General Purpose Direct Memory Access (GPDMA) controller, a 10/100 Ethernet Media Access Controller (MAC), a Universal Serial Bus (USB) controller, and an LCD controller. Each of these four peripherals contain an integral DMA controller optimized to support the performance demands of the peripheral.

7.6.1 General Purpose DMA (GPDMA) controller

The GPDMA controller allows peripheral-to memory, memory-to-peripheral, peripheral-to-peripheral, and memory-to-memory transactions. Each DMA stream provides unidirectional serial DMA transfers for a single source and destination. For example, a bidirectional port requires one stream for transmit and one for receive. The source and destination areas can each be either a memory region or a peripheral, and can be accessed through the same AHB master, or one area by each master. The DMA controller supports the following peripheral device transfers.

- Secure Digital (SD) Memory interface
- High-speed UARTs
- I^2S0 and I^2S1 ports
- SPI1 and SPI2 interfaces
- SSP0 and SSP1 interfaces
- Memory

The DMA controls eight DMA channels with hardware prioritization. The DMA controller interfaces to the system via two AHB bus masters, each with a full 32-bit data bus width. DMA operations may be set up for 8-bit, 16-bit, and 32-bit data widths, and can be either big-endian or little-endian. Incrementing or non-incrementing addressing for source and destination are supported, as well as programmable DMA burst size. Scatter or gather DMA is supported through the use of linked lists. This means that the source and destination areas do not have to occupy contiguous areas of memory.

7.6.2 Ethernet MAC

The Ethernet block contains a full featured 10 Mbit/s or 100 Mbit/s Ethernet MAC designed to provide optimized performance through the use of DMA hardware acceleration. Features include a generous suite of control registers, half or full duplex operation, flow control, control frames, hardware acceleration for transmit retry, receive

condition is indicated via status registers. An interrupt is also generated if enabled. The DMA controller when enabled transfers data between the endpoint buffer and the USB RAM.

Features

- Fully compliant with *USB 2.0 full-speed specification*.
- Supports 32 physical (16 logical) endpoints.
- Supports control, bulk, interrupt and isochronous endpoints.
- Scalable realization of endpoints at run time.
- Endpoint maximum packet size selection (up to USB maximum specification) by software at run time.
- RAM message buffer size based on endpoint realization and maximum packet size.
- Supports bus-powered capability with low suspend current.
- Supports DMA transfer on all non-control endpoints.
- One duplex DMA channel serves all endpoints.
- Allows dynamic switching between CPU controlled and DMA modes.
- Double buffer implementation for bulk and isochronous endpoints.

7.6.3.2 USB host controller

The host controller enables data exchange with various USB devices attached to the bus. It consists of register interface, serial interface engine and DMA controller. The register interface complies to the *OHCI specification*.

Features

- OHCI compliant.
- OHCI specifies the operation and interface of the USB host controller and software driver.
- The host controller has four USB states visible to the software driver:
  - USBOperational: Process lists and generate SOF tokens.
  - USBReset: Forces reset signaling on the bus, SOF disabled.
  - USBSuspend: Monitor USB for wake-up activity.
  - USBResume: Forces resume signaling on the bus.
- HCCA register points to interrupt and isochronous descriptors list.
- ControlHeadED and BulkHeadED registers point to control and bulk descriptors list.

7.6.3.3 USB OTG controller

USB OTG (On-The-Go) is a supplement to the *USB 2.0 specification* that augments the capability of existing mobile devices and USB peripherals by adding host functionality for connection to USB peripherals.

Features

- Fully compliant with *On-The-Go supplement to the USB Specification 2.0 Revision 1.0*.

7.8.1 UARTs

The LPC3220/30/40/50 contains seven UARTs. Four are standard UARTs, and three are high-speed UARTs.

7.8.1.1 Standard UARTs

The four standard UARTs are compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32, 48, and 60 Bytes.
- Transmitter FIFO trigger points at 0, 4, 8, and 16 Bytes.
- Register locations conform to the “550” industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

7.8.1.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock for on-board communication in low noise conditions. This is accomplished by changing the over sampling from 16× to 14× and altering the rate generation logic.

Features

- Each high-speed UART has 64-byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 B.
- Transmitter FIFO trigger points at 0, 4, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- The three high speed UARTs only support (8N1) 8-bit data word length, 1-stop bit, no parity, and no flow control as a the communications protocol.
- Each UART includes an internal loopback mode.

7.8.2 SPI serial I/O controller

The LPC3220/30/40/50 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

9. Limiting values

Table 7. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).[1]

Symbol	Parameter	Conditions	Notes	Min	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)		[2]	−0.5	+1.4	V
$V_{DD(EMC)}$	external memory controller supply voltage		[3]	−0.5	+4.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)		[4]	−0.5	+4.6	V
$V_{DD(IO)}$	input/output supply voltage		[5]	−0.5	+4.6	V
V_{IA}	analog input voltage			−0.5	+4.6	V
V_I	input voltage	1.8 V pins	[6]	−0.5	+2.4	V
		3.3 V pins	[6]	−0.5	+4.6	V
I_{DD}	supply current	per supply pin		-	100	mA
I_{SS}	ground current	per ground pin		-	100	mA
T_{stg}	storage temperature			−65	+150	°C
$P_{tot(pack)}$	total power dissipation (per package)	max. junction temp 125 °C max. ambient temp 85 °C	[7]	-	1.12	W
V_{ESD}	electrostatic discharge voltage	HBM	[8]	-	2500	V
		CDM	[9]	-	1000	V

[1] The following applies to Table 7:

a) This product includes circuitry specifically designed for the protection of its internal devices from the damaging effects of excessive static charge. Nonetheless, it is suggested that conventional precautions be taken to avoid applying greater than the rated maximum.

b) Parameters are valid over operating temperature range unless otherwise specified. All voltages are with respect to V_{SS} unless otherwise noted.

[2] Core, PLL, oscillator, and RTC supplies; applies to pins VDD_CORE, VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[3] I/O pad supply; applies to domains VDD_EMC.

[4] Applies to VDD_AD pins.

[5] Applies to pins in the following domains VDD_IOA, VDD_IOB, VDD_IOC, and VDD_IOD.

[6] Including voltage on outputs in 3-state mode.

[7] Based on package heat transfer, not device power consumption. Calculated package thermal resistance ($Theta_{JA}$): 35.766 °C/W (with JEDEC Test Board and 0 m/s airflow, ±15 % accuracy).

[8] Human body model: equivalent to discharging a 100 pF capacitor through a 1.5 kΩ series resistor.

[9] Charge device model per AEC-Q100-011.

10. Static characteristics

Table 8. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)	core supply voltage for full performance; 266 MHz (see Figure 4); VDD_CORE supply domain	[2]	1.31	1.35	1.39	V
		core supply voltage for normal performance; 208 MHz (see Figure 4); VDD_CORE supply domain	[2]	1.1	1.2	1.39	V
		core supply voltage for reduced power; up to 14 MHz CPU; VDD_CORE supply domain	[2]	0.9	-	1.39	V
		RTC supply voltage; VDD_RTC supply domain	[3]	0.9	-	1.39	V
		PLL and oscillator supply voltage	[4]	1.1	1.2	1.39	V
$V_{DD(EMC)}$	external memory controller supply voltage	in 1.8 V range	[5]	1.7	1.8	1.95	V
		in 2.5 V range	[6]	2.3	2.5	2.7	V
		in 3.3 V range	[7]	2.7	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage	VDD_IOA, VDD_IOB, and VDD_IOD supply domain in 1.8 V range		1.7	1.8	1.95	V
		in 3.3 V range		2.7	3.3	3.6	V
		VDD_IOC supply domain in 1.8 V range		1.7	1.8	1.95	V
		in 3.3 V range		2.3	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	applies to pins in VDD_AD power domain		2.7	3.3	3.6	V

10.1 Minimum core voltage requirements

Figure 4 shows the minimum core supply voltage that should be applied for a given core frequency on pin VDD_CORE to ensure stable operation of the LPC3220/30/40/50.

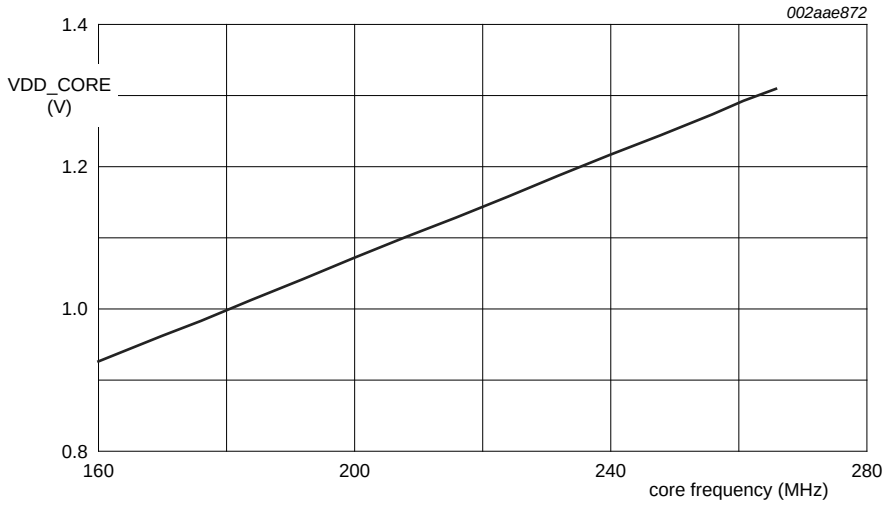

Fig 4. Minimum required core supply voltage for different core frequencies

10.2 Power supply sequencing

The LPC32x0 has no power sequencing requirements, that is, $V_{DD(1V2)}$, $V_{DD(EMC)}$, $V_{DD(IO)}$, and $V_{DDA(3V3)}$ can be switched on or off independent of each other. An internal circuit ensures that the system correctly powers up in the absence of core power. During IO power-up this circuit takes care that the system is powered in a defined mode. The same is valid for core power-down.

10.3 Power consumption per peripheral

Table 9. Power consumption per peripheral

T_{amb} = 25 °C; CPU clock = 208 MHz; I-cache/D-cache, MMU disabled; VDD_CORE = 1.2 V; $V_{DD(IO)}$ = 1.8 V; USB AHB, IRAM, and IROM clocks always on; all peripherals are at their default state at reset. Peripheral clocks are disabled except for peripheral measured.

Peripheral	$I_{DD(run)}$ / mA
High-speed UART (set to 115 200 Bd (8N1))	0.3
I^2C-bus	0.3
SSP	0.6
I^2S	0.5
DMA	6.3
EMC	7.3
Multi-level NAND controller	1.4
Single-level NAND controller	0.3
LCD	5.6
Ethernet MAC[1]	2.9

[1] All three Ethernet clocks are in enabled in the MAC_CLK_CTRL register (see *LPC32x0 User manual*).

10.5 ADC static characteristics

Table 10. ADC static characteristics

$V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C unless otherwise specified; ADC clock frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	±0.5	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	±0.6	±1	LSB
E_O	offset error		[1][5]	-	±1	±3	LSB
E_G	gain error		[1][6]	-	±0.3	±0.6	%
E_T	absolute error		[1][7]	-		±4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V (on pin VSS_AD); $V_{DDA(3V3)}$ = 3.3 V (on pin VDD_AD).

[2] The ADC is monotonic; there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 6.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 6.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 6.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 6.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 6.

11. Dynamic characteristics

11.1 Clocking and I/O port pins

Table 11. Dynamic characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1]

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
Reset							
$t_{w(\overline{RESET})ext}$	external $\overline{RESET}$ pulse width		[2]	10	-	-	ms
External clock							
f_{ext}	external clock frequency		[3]	1	13	20	MHz
Port pins							
t_r	rise time			-	5	-	ns
t_f	fall time			-	5	-	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] After supply voltages are stable

[3] Supplied by an external crystal.

11.2 Static memory controller

Table 12. Dynamic characteristics: static external memory interface

C_L = 25 pF, T_{amb} = 20 °C, $V_{DD(EMC)}$ = 1.8 V, 2.5 V, or 3.3 V.

Symbol	Parameter	Notes	Min	Typ	Max	Unit
Common to read and write cycles						
T_{CLCL}	clock cycle time	[1]	7.5	9.6	-	ns
t_{CSLAV}	$\overline{CS}$ LOW to address valid time		-	0	-	ns
Read cycle parameters						
t_{OELAV}	$\overline{OE}$ LOW to address valid time	[2]	-	$0 - WAITOEN \times T_{CLCL}$	-	ns
t_{BLSLAV}	$\overline{BLS}$ LOW to address valid time	[2]	-	$0 - WAITOEN \times T_{CLCL}$	-	ns
t_{CSLOEL}	$\overline{CS}$ LOW to $\overline{OE}$ LOW time		-	$0 + WAITOEN \times T_{CLCL}$	-	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	[2]	-	$0 + WAITOEN \times T_{CLCL}$	-	ns
t_{OELOEH}	$\overline{OE}$ LOW to $\overline{OE}$ HIGH time	[2][3]	-	$(WAITRD - WAITOEN + 1) \times T_{CLCL}$	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[2][3]	-	$(WAITRD - WAITOEN + 1) \times T_{CLCL}$	-	ns
$t_{su(DQ)}$	data input/output set-up time	[6]	-	8.4	-	ns
$t_{h(DQ)}$	data input/output hold time	[6]	-	0	-	ns
t_{CSHOEH}	$\overline{CS}$ HIGH to $\overline{OE}$ HIGH time		-	0	-	ns
$t_{CSHBLSH}$	$\overline{CS}$ HIGH to $\overline{BLS}$ HIGH time		-	0	-	ns
t_{OEHANV}	$\overline{OE}$ HIGH to address invalid time		-	$1 \times T_{CLCL}$	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		-	$1 \times T_{CLCL}$	-	ns
Write cycle parameters						
t_{CSLDV}	$\overline{CS}$ LOW to data valid time		-	0	-	ns
t_{CSLWEL}	$\overline{CS}$ LOW to $\overline{WE}$ LOW time	[4]	-	$(WAITWEN + 1) \times T_{CLCL}$	-	ns
$t_{CSLBLSL}$	$\overline{CS}$ LOW to $\overline{BLS}$ LOW time	[4]	-	$(WAITWEN + 1) \times T_{CLCL}$	-	ns
t_{WELDV}	$\overline{WE}$ LOW to data valid time	[4]	-	$0 - (WAITWEN + 1) \times T_{CLCL}$	-	ns

Table 18. Dynamic characteristics of SLC NAND flash memory controller *…continued*
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{WH}	$\overline{WE}$ HIGH hold time	write	[1][6][7]	-	$T_{HCLK} \times (Wsu + Wh)$	-	ns
t_{WHR}	$\overline{WE}$ HIGH to $\overline{RE}$ LOW time	write	[1][7][9]	-	$(T_{HCLK} \times Wh) + (2 \times T_{HCLK} \times Wb)$	-	ns
t_{WP}	$\overline{WE}$ pulse width	write	[1][8]	-	$T_{HCLK} \times Ww$	-	ns
t_{REHRBL}	$\overline{RE}$ HIGH to R/$\overline{B}$ LOW time	write	[1][3][5]	-	$(T_{HCLK} \times Rh) + (2 \times T_{HCLK} \times Rb)$	-	ns

[1] T_{HCLK} = 1/HCLK

[2] Rsu = bit field R_SETUP[3:0] in register SLC_TAC[3:0] for reads

[3] Rh = bit field R_HOLD[3:0] in register SLC_TAC[7:4] for reads

[4] Rw = bit field R_WIDTH[3:0] in register SLC_TAC[11:8] for reads

[5] Rb = bit field R_RDY[3:0] in register SLC_TAC[15:12] for reads

[6] Wsu = bit field W_SETUP[3:0] in register SLC_TAC[19:16] for writes

[7] Wh = bit field W_HOLD[3:0] in register SLC_TAC[23:20] for writes

[8] Ww = bit field W_WIDTH[3:0] in register SLC_TAC[27:24] for writes

[9] Wb = bit field W_RDY[3:0] in register SLC_TAC[31:28] for writes

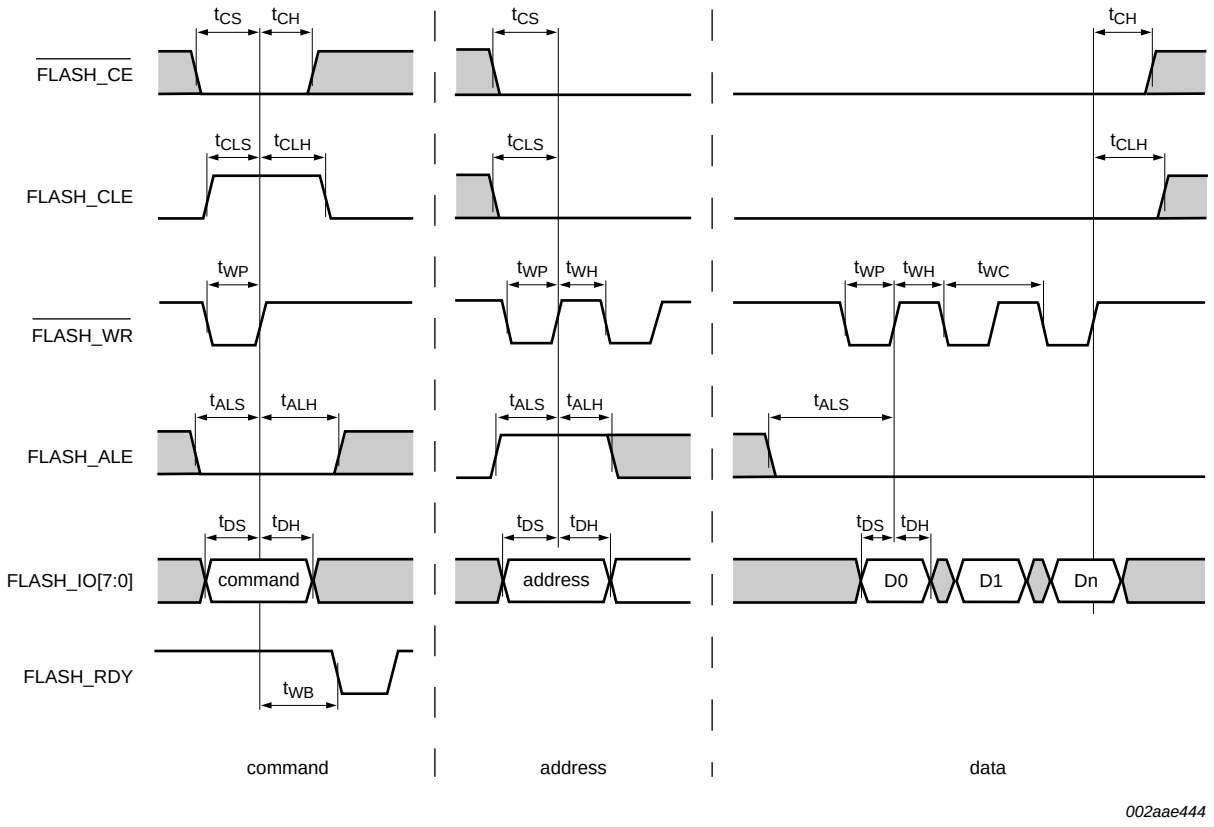

Fig 17. MLC NAND flash memory write timing (writing to NAND flash)

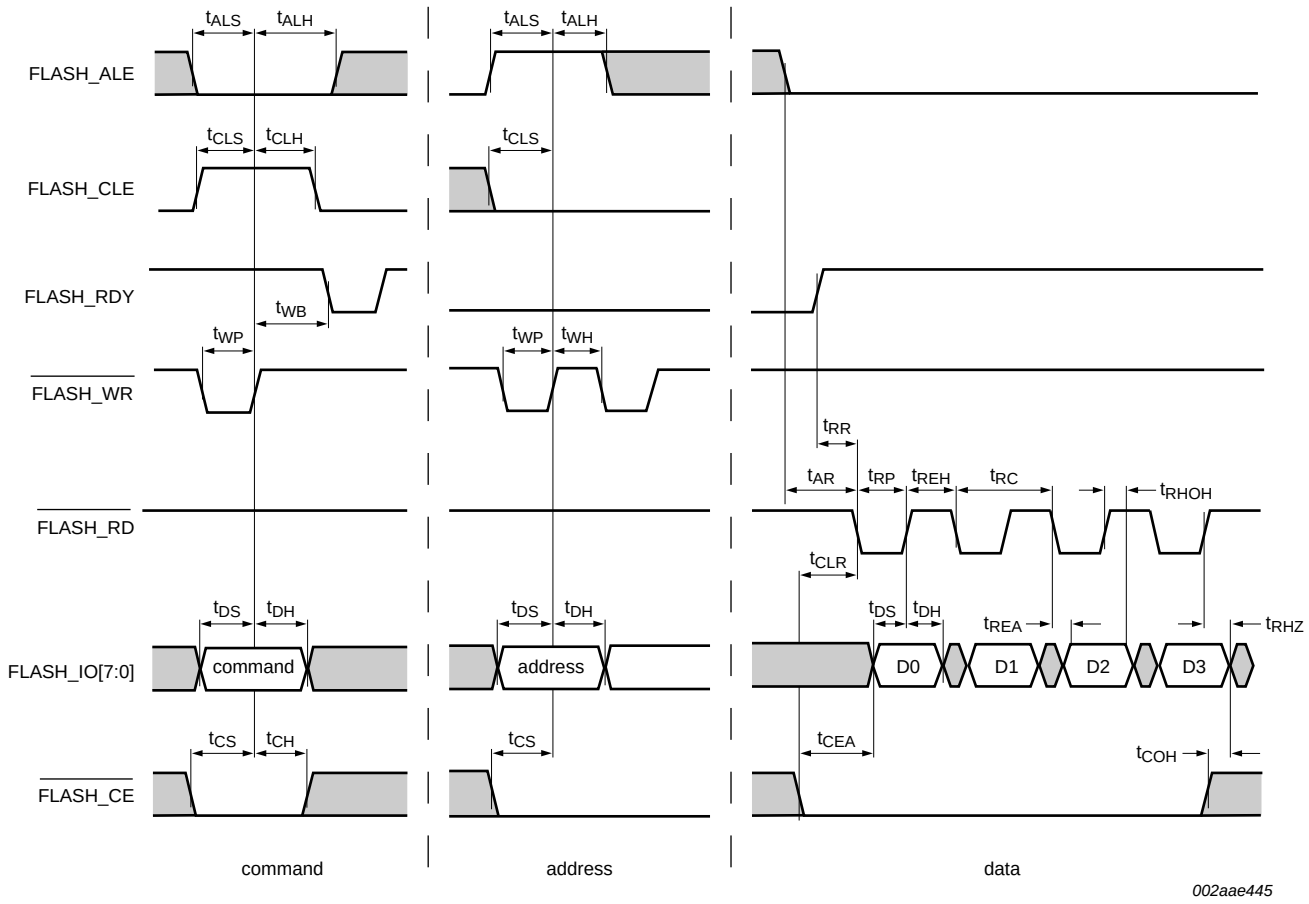

Fig 18. MLC NAND Flash memory read timing (reading from NAND flash)

11.9.2 Timing diagrams for SPI and SSP (in SPI mode)

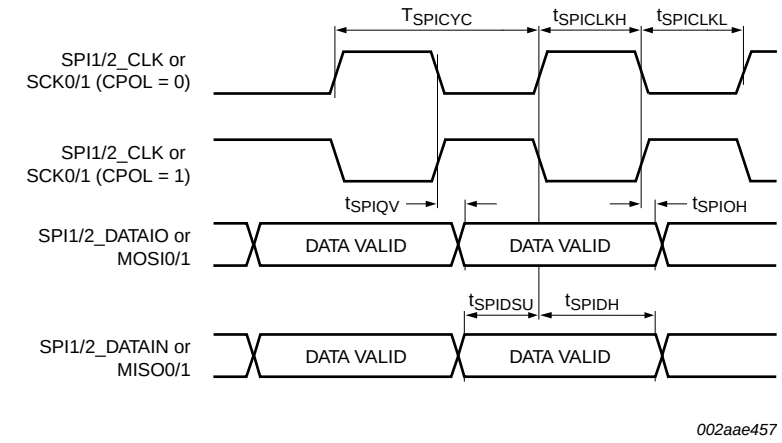

Fig 20. SPI master timing (CPHA = 0)

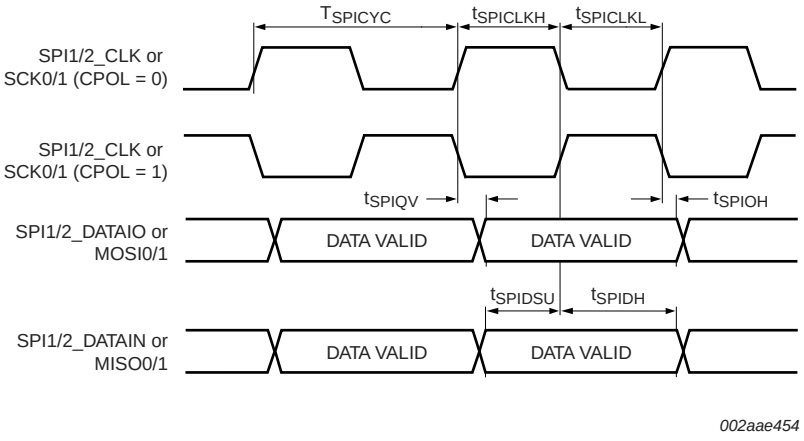

Fig 21. SPI master timing (CPHA = 1)

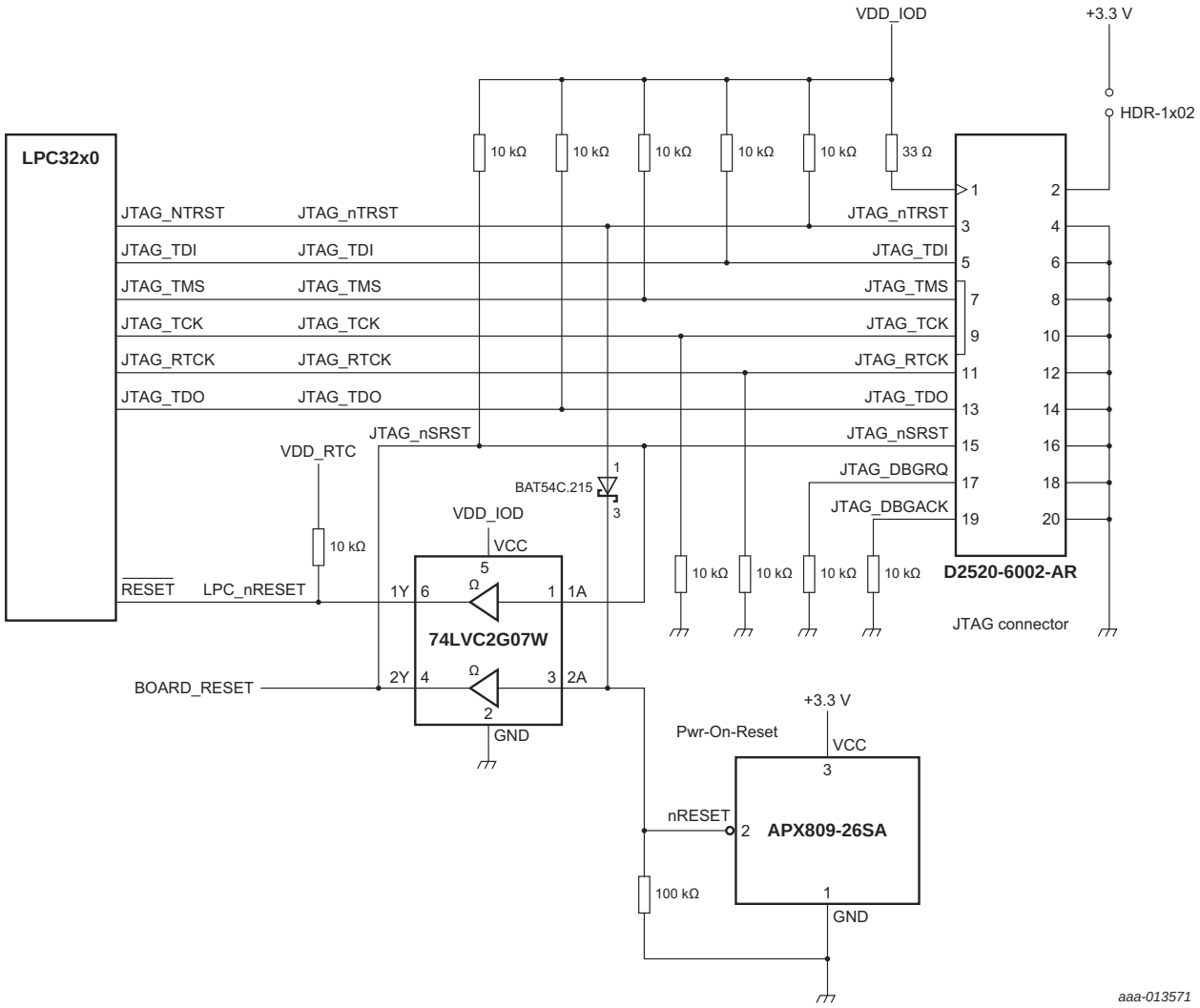

Fig 24. Circuit for holding JTAG_NTRST LOW during POR

Table 20. Abbreviations *…continued*

Acronym	Description
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus
VFP	Vector Floating Point processor

15. References

[1] LPC3220/30/40/50 User manual UM10326: http://www.nxp.com/documents/user_manual/UM10326.pdf

[2] LPC3220/30/40/50 Errata sheet: http://www.nxp.com/documents/errata_sheet/ES_LPC3250.pdf

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