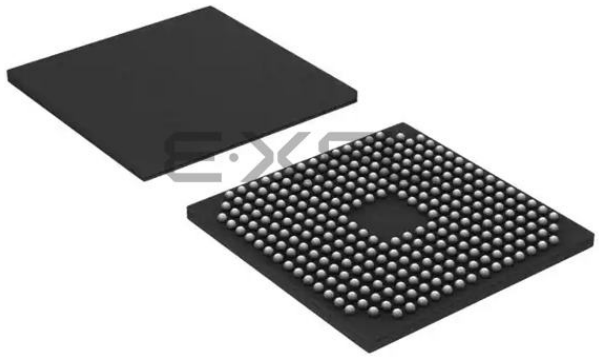

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3240fet296-551

- Six enhanced timer/counters which are architecturally identical except for the peripheral base address. Two capture inputs and two match outputs are pinned out to four timers. Timer 1 brings out a third match output, timers 2 and 3 bring out all four match outputs, timer 4 has one match output, and timer 5 has no inputs or outputs.
- 32-bit millisecond timer driven from the RTC clock. This timer can generate interrupts using two match registers.
- WatchDog timer clocked by the peripheral clock.
- Two single-output PWM blocks.
- Motor control PWM.
- Keyboard scanner function allows automatic scanning of an up to 8 × 8 key matrix.
- Up to 18 external interrupts.

- Standard ARM test/debug interface for compatibility with existing tools.
- Emulation Trace Buffer (ETB) with 2048 × 24 bit RAM allows trace via JTAG.
- Stop mode saves power while allowing many peripheral functions to restart CPU activity.
- On-chip crystal oscillator.
- An on-chip PLL allows CPU operation up to the maximum CPU rate without the requirement for a high frequency crystal. Another PLL allows operation from the 32 kHz RTC clock rather than the external crystal.
- Boundary scan for simplified board testing.
- User-accessible unique serial ID number for each chip.
- TFBGA296 package with a 15 mm × 15 mm × 0.7 mm body.

3. Applications

- Consumer
- Medical
- Industrial
- Network control

6. Pinning information

6.1 Pinning

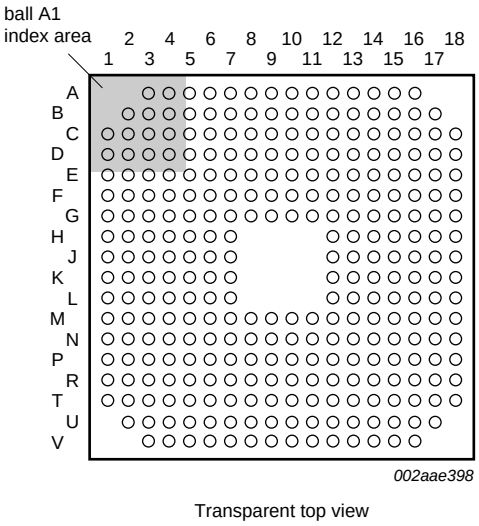


Fig 2. Pin configuration for SOT1048-1 (TFBGA296)

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
Row A					
				A3	I2C2_SCL
A4	I2S1TX_CLK/MAT3[0]	A5	I2C1_SCL	A6	MS_BS/MAT2[1]
A7	MS_DIO1/MAT0[1]	A8	MS_DIO0/MAT0[0]	A9	SPI2_DATIO/MOSI1/LCDVD[20][1]
A10	SPI2_DATIN/MISO1/ LCDVD[21][1]/GPI_27	A11	GPIO_1	A12	GPIO_0
A13	GPO_21/U4_TX/LCDVD[3][1]	A14	GPO_15/MCOA1/LCDFP[1]	A15	GPO_7/LCDVD[2][1]
A16	GPO_6/LCDVD[18][1]				
Row B					
		B2	GPO_20	B3	GPO_5
B4	I2S1TX_WS/CAP3[0]	B5	P0[0]/I2S1RX_CLK	B6	I2C1_SDA
B7	MS_SCLK/MAT2[0]	B8	MS_DIO2/MAT0[2]	B9	SPI1_DATIO/MOSI0/MCI2
B10	SPI2_CLK/SCK1/LCDVD[23][1]	B11	GPIO_4/SSEL1/LCDVD[22][1]	B12	GPO_12/MCOA2/LCDLE[1]
B13	GPO_13/MCOB1/LCDDCLK[1]	B14	GPO_2/MAT1[0]/LCDVD[0][1]	B15	GPI_19/U4_RX
B16	GPI_8/KEY_COL6/ SPI2_BUSY/ENET_RX_DV[2]	B17	n.c.		
Row C					
C1	$\overline{\text{FLASH\_RD}}$	C2	GPO_19	C3	GPO_0/TST_CLK1
C4	$\overline{\text{USB\_ATX\_INT}}$	C5	USB_SE0_VM/U5_TX	C6	TST_CLK2
C7	GPI_6/HSTIM_CAP/ ENET_RXD2[2]	C8	MS_DIO3/MAT0[3]	C9	SPI1_CLK/SCK0

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
H16	HIGHCORE/LCDVD[17][1]	H17	JTAG_NTRST	H18	JTAG_RTCK
Row J					
J1	EMC_A[20]/P1[20]	J2	EMC_A[21]/P1[21]	J3	EMC_A[22]/P1[22]
J4	EMC_A[23]/P1[23]	J5	VDD_IOC	J6	VDD_EMC
J7	VDD_CORE				
				J12	VDD_CORE
J13	VDD_IOA	J14	U3_RX/GPI_18	J15	JTAG_TDO
J16	JTAG_TDI	J17	U3_TX	J18	U2_HCTS/U3_CTS/GPI_16
Row K					
K1	EMC_A[19]/P1[19]	K2	EMC_A[18]/P1[18]	K3	EMC_A[16]/P1[16]
K4	EMC_A[17]/P1[17]	K5	VSS_EMC	K6	VDD_EMC
K7	VDD_EMC				
				K12	VSS_CORE
K13	VSS_IOA	K14	VDD_RTC	K15	U1_RX/CAP1[0]/GPI_15
K16	U1_TX	K17	U2_TX/U3_DTR	K18	U2_RX/U3_DSR/GPI_17
Row L					
L1	EMC_A[15]/P1[15]	L2	EMC_CKE1	L3	EMC_A[0]/P1[0]
L4	EMC_A[1]/P1[1]	L5	VSS_EMC	L6	VDD_EMC
L7	VSS_CORE				
				L12	VDD_COREFXD
L13	VDD_RTCCORE	L14	VSS_RTCCORE	L15	P0[4]/I2S0RX_WS/LCDVD[6][1]
L16	P0[5]/I2S0TX_SDA/LCDVD[7][1]	L17	P0[6]/I2S0TX_CLK/ LCDVD[12][1]	L18	P0[7]/I2S0TX_WS/LCDVD[13][1]
Row M					
M1	EMC_A[2]/P1[2]	M2	EMC_A[3]/P1[3]	M3	EMC_A[4]/P1[4]
M4	EMC_A[8]/P1[8]	M5	VSS_EMC	M6	VDD_EMC
M7	VDD_CORE	M8	VDD_EMC	M9	VSS_CORE
M10	VSS_CORE	M11	VDD_CORE	M12	VSS_CORE
M13	VDD_COREFXD	M14	$\overline{\text{RESET}}$	M15	ONSW
M16	GPO_23/U2_HRTS/U3_RTS	M17	P0[2]/I2S0RX_SDA/ LCDVD[4][1]	M18	P0[3]/I2S0RX_CLK/LCDVD[5][1]
Row N					
N1	EMC_A[5]/P1[5]	N2	EMC_A[6]/P1[6]	N3	EMC_A[7/P1[7]
N4	EMC_A[12]/P1[12]	N5	VSS_EMC	N6	VSS_EMC
N7	VDD_EMC	N8	VDD_EMC	N9	VDD_EMC
N10	VDD_EMC	N11	VDD_EMC	N12	VDD_AD
N13	VDD_AD	N14	VDD_FUSE	N15	VDD_RTCOSC
N16	GPI_5/U3_DCD	N17	GPI_28/U3_RI	N18	GPO_17
Row P					
P1	EMC_A[9]/P1[9]	P2	EMC_A[10]/P1[10]	P3	EMC_A[11]/P1[11]
P4	EMC_DQM[1]	P5	EMC_DQM[3]	P6	VSS_EMC

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
P7	VSS_EMC	P8	VSS_EMC	P9	VSS_EMC
P10	VSS_EMC	P11	VSS_EMC	P12	EMC_BLS[3]
P13	VSS_AD	P14	VSS_OSC	P15	VDD_PLLUSB
P16	RTCX_IN	P17	RTCX_OUT	P18	VSS_RTCOSC
Row R					
R1	EMC_A[13]/P1[13]	R2	EMC_A[14]/P1[14]	R3	EMC_DQM[0]
R4	$\overline{\text{EMC\_WR}}$	R5	$\overline{\text{EMC\_CAS}}$	R6	$\overline{\text{EMC\_DYCS0}}$
R7	EMC_D[1]	R8	EMC_D[7]	R9	EMC_D[17]/EMC_DQS1
R10	EMC_D[24]/P2[5]	R11	$\overline{\text{EMC\_CS1}}$	R12	EMC_BLS[2]
R13	TS_XP	R14	PLL397_LOOP	R15	SYSX_OUT
R16	VSS_PLLUSB	R17	VDD_PLLHCLK	R18	VSS_PLLHCLK
Row T					
T1	EMC_DQM[2]	T2	$\overline{\text{EMC\_RAS}}$	T3	EMC_CLK
T4	EMC_CLKIN	T5	EMC_D[2]	T6	EMC_D[6]
T7	EMC_D[11]	T8	EMC_D[14]	T9	EMC_D[20]/P2[1]
T10	EMC_D[23]/P2[4]	T11	EMC_D[27]/P2[8]	T12	$\overline{\text{EMC\_CS2}}$
T13	EMC_BLS[1]	T14	ADIN1/TS_XM	T15	VSS_PLL397
T16	VDD_PLL397	T17	SYSX_IN	T18	VDD_OSC
Row U					
		U2	n.c.	U3	EMC_CKE0
U4	EMC_D[0]	U5	EMC_D[3]	U6	EMC_D[9]
U7	EMC_D[12]	U8	EMC_D[15]	U9	EMC_D[19]/P2[0]
U10	EMC_D[22]/P2[3]	U11	EMC_D[26]/P2[7]	U12	EMC_D[30]/P2[11]
U13	$\overline{\text{EMC\_CS0}}$	U14	EMC_BLS[0]	U15	ADIN0/TS_YM
U16	TS_YP	U17	n.c.		
Row V					
				V3	EMC_D[4]
V4	EMC_D[5]	V5	EMC_D[8]	V6	EMC_D[10]
V7	EMC_D[13]	V8	EMC_D[16]/EMC_DQS0	V9	EMC_D[18]/$\overline{\text{EMC\_CLK}}$
V10	EMC_D[21]/P2[2]	V11	EMC_D[25]/P2[6]	V12	EMC_D[28]/P2[9]
V13	EMC_D[29]/P2[10]	V14	EMC_D[31]/P2[12]	V15	$\overline{\text{EMC\_CS3}}$
V16	ADIN2/TS_AUX_IN				

[1] LCD on LPC3230 and LPC3250 only.

[2] Ethernet on LPC3240 and LPC3250 only.

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
U7_HCTS/ CAP0[1]/ LCDCLKIN/ GPI_22	G13	VDD_IOD	I	HS UART 7 CTS in
			I	Timer 0 capture input 1
			I	LCD panel clock in (LPC3230 and LPC3250 only)
			I	General purpose input bit 22
U7_RX/ CAP0[0]/ LCDVD[10]/ GPI_23	E17	VDD_IOD	I/O	HS UART 7 receive
			I/O	Timer 0 capture input 0
			I/O	LCD data bit 10 (LPC3230 and LPC3250 only)
			I/O	General purpose input bit 23
U7_TX/ MAT1[1]/ LCDVD[11]	E18	VDD_IOD	O	HS UART 7 transmit
			O	Timer 1 match output 1
			O	LCD data bit 11 (LPC3230 and LPC3250 only)
$\overline{\text{USB\_ATX\_INT}}$	C4	VDD_IOC	I	Interrupt from USB ATX
USB_DAT_VP/ U5_RX	D5	VDD_IOC	I/O: P	USB transmit data, D+ receive
			I/O: P	UART 5 receive
USB_I2C_SCL	E5	VDD_IOC	I/O T	I^2C clock for USB ATX interface
USB_I2C_SDA	E6	VDD_IOC	I/O T	I^2C data for USB ATX interface
$\overline{\text{USB\_OE\_TP}}$	D6	VDD_IOC	I/O	USB transmit enable for DAT/SE0
USB_SE0_VM/ U5_TX	C5	VDD_IOC	I/O: P	USB single ended zero transmit, D− Receive
			I/O: P	UART 5 transmit
VDD_AD	N12, N13	VDD_AD	power	3.3 V supply for ADC/touch screen
VDD_CORE	G7, G9, G11, J7, J12, M7, M11	VDD_CORE	power	1.2 V or 0.9 V supply for core
VDD_COREFXD	L12, M13	VDD_COREFXD	power	Fixed 1.2 V supply for digital portion of the analog block
VDD_EMC	J6, K6, K7, L6, M6, M8, N7, N8, N9, N10, N11	VDD_EMC	power	1.8 V or 2.5 V or 3.3 V supply for External Memory Controller (EMC)
VDD_IOA	H13, J13	VDD_IOA	power	1.8 V or 3.3 V supply for IOA domain
VDD_IOB	F8	VDD_IOB	power	1.8 V or 3.3 V supply for IOB domain

7.1.3.2 Embedded trace buffer

The Embedded Trace Module (ETM) is connected directly to the ARM core. It compresses the trace information and exports it through a narrow trace port. An internal Embedded Trace Buffer (ETB) of 2048 × 24 bits captures the trace information under software debugger control. Data from the ETB is recovered by the debug software through the JTAG port.

The trace contains information about when the ARM core switches between states. Instruction shows the flow of execution of the processor and provides a list of all the instructions that were executed. Instruction trace is significantly compressed by only broadcasting branch addresses as well as a set of status signals that indicate the pipeline status on a cycle by cycle basis. For data accesses either data or address or both can be traced.

7.2 AHB matrix

The LPC3220/30/40/50 has a multi-layer AHB matrix for inter-block communication. AHB is an ARM defined high-speed bus, which is part of the ARM bus architecture. AHB is a high-bandwidth low-latency bus that supports multi-master arbitration and a bus grant/request mechanism. For systems that have only one (CPU), or two (CPU and DMA) bus masters a simple AHB works well. However, if a system requires multiple bus masters and the CPU needs access to external memory, a single AHB bus can cause a bottleneck.

To increase performance, the LPC3220/30/40/50 uses an expanded AHB architecture known as Multi-layer AHB. A Multi-layer AHB replaces the request/grant and arbitration mechanism used in a simple AHB with an interconnect matrix that moves arbitration out toward the slave devices. Thus, if a CPU and a DMA controller want access to the same memory, the interconnect matrix arbitrates between the two when granting access to the memory. This advanced architecture allows simultaneous access by bus masters to different resources with an increase in arbitration complexity. In this architectural implementation, removing guaranteed central arbitration and allowing more than one bus master to be active at the same time provides better overall microcontroller performance.

In the LPC3220/30/40/50, the multi-Layer AHB system has a separate bus for each of seven AHB Masters:

- CPU data bus
- CPU instruction bus
- General purpose DMA Master 0
- General purpose DMA Master 1
- Ethernet controller
- USB controller
- LCD controller

There are no arbitration delays unless two masters attempt to access the same slave at the same time.

7.4 Internal memory

7.4.1 On-chip ROM

The built-in 16 kB ROM contains a program which runs a boot procedure to load code from one of four external sources, UART 5, SSP0 (SPI mode), EMC Static CS0 memory, or NAND FLASH.

After reset, execution always begins from the internal ROM. The bootstrap software first reads the $\overline{\text{SERVICE}}$ input (GPI_1). If $\overline{\text{SERVICE}}$ is LOW, the bootstrap starts a service boot and can download a program over serial link UART 5 to IRAM and transfer execution to the downloaded code.

If the $\overline{\text{SERVICE}}$ pin is HIGH, the bootstrap routine jumps to normal boot. The normal boot process first tests SPI memory for boot information if present it uploads the boot code and transfers execution to the uploaded software. If the SPI is not present or no software is loaded, the bootloader will test the EMC Static CS0 memory for the presence of boot code and if present boots from static memory, If this test fails the boot loader will test external NAND flash for boot code and boot if code is present.

The boot loader consumes no user memory space because it is in ROM.

7.4.2 On-chip SRAM

On-chip SRAM may be used for code and/or data storage. The SRAM may be accessed as 8, 16, or 32 bit memory. The LPC3220/30/40/50 provides 256 kB of internal SRAM.

7.5 External memory interfaces

The LPC3220/30/40/50 includes three external memory interfaces, NAND Flash controllers, Secure Digital Memory Controller, and an external memory controller for SDRAM, DDR SDRAM, and Static Memory devices.

7.5.1 NAND flash controllers

The LPC3220/30/40/50 includes two NAND flash controllers, one for multi-level cell NAND flash devices and one for single-level cell NAND flash devices. The two NAND flash controllers use the same pins to interface to external NAND flash devices, so only one interface is active at a time.

7.5.1.1 Multi-Level Cell (MLC) NAND flash controller

The MLC NAND flash controller interfaces to either multi-level or single-level NAND flash devices. An external NAND flash device is used to allow the bootloader to automatically load a portion of the application code into internal SRAM for execution following reset.

The MLC NAND flash controller supports small (528 byte) and large (2114 byte) pages. Programmable NAND timing parameters allow support for a variety of NAND flash devices. A built-in Reed-Solomon encoder/decoder provides error detection and correction capability. A 528 byte data buffer reduces the need for CPU supervision during loading. The MLC NAND flash controller also provides DMA support.

packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU. The Ethernet DMA can access off-chip memory via the EMC, as well as the IRAM. The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.6.2.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching. Wake-on-LAN power management support allows system wake-up using the receive filters or a magic frame detection filter.
- Physical interface
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.6.3 USB interface

The LPC3220/30/40/50 supports USB in either device, host, or OTG configuration.

7.6.3.1 USB device controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error

7.7.4 Clocking and power control features

7.7.4.1 Clocking

Clocking in the LPC3220/30/40/50 is designed to be versatile, so that system and peripheral requirements may be met, while allowing optimization of power consumption. Clocks to most functions may be turned off if not needed and some peripherals do this automatically.

The LPC3220/30/40/50 supports three operational modes, two of which are specifically designed to reduce power consumption. The modes are: Run mode, Direct run mode, and Stop mode.These three operational modes give control over processing speed and power consumption. In addition, clock rates to different functional blocks may be changed by switching clock sources, changing PLL values, or altering clock divider configurations. This allows a trade-off of power versus processing speed based on application requirements.

7.7.4.2 Crystal oscillator

The main oscillator is the basis for the clocks most chip functions use by default. Optionally, many functions can be clocked instead by the output of a PLL (with a fixed 397x rate multiplication) which runs from the RTC oscillator. In this mode, the main oscillator may be turned off unless the USB interface is enabled. If a SYSCLK frequency other than 13 MHz is required in the application, or if the USB block is not used, the main oscillator may be used with a frequency of between 1 MHz and 20 MHz.

7.7.4.3 PLLs

The LPC3220/30/40/50 includes three PLLs: The 397x PLL allows boosting the RTC frequency to 13.008896 MHz for use as the primary system clock. The USB PLL provides the 48 MHz clock required by the USB block, and the HCLK PLL provides the basis for the CPU clock, the AHB bus clock, and the main peripheral clock.

The 397x PLL multiplies the 32768 Hz RTC clock by 397 to obtain a 13.008896 MHz clock. The 397x PLL is designed for low power operation and low jitter. This PLL requires an external RC loop filter for proper operation.

The HCLK PLL accepts an input clock from either the main oscillator or the output of the 397x PLL. The USB PLL only accepts an input clock from the main oscillator.The USB input clock runs through a divide-by-N pre-divider before entering the USB PLL.

The input to the HCLK and USB PLLs may initially be divided down by a pre-divider value ‘N’, which may have the values 1, 2, 3, or 4. This pre-divider can allow a greater number of possibilities for the output frequency. Following the PLL input divider is the PLL multiplier. This can multiply the pre-divider output by a value ‘M’, in the range of 1 through 256. The resulting frequency must be in the range of 156 MHz to 320 MHz. The multiplier works by dividing the output of a Current Controlled Oscillator (CCO) by the value of M, then using a phase detector to compare the divided CCO output to the pre-divider output. The error value is used to adjust the CCO frequency.

At the PLL output, there is a post-divider that can be used to bring the CCO frequency down to the desired PLL output frequency. The post-divider value can divide the CCO output by 1, 2, 4, 8, or 16. The post-divider can also be bypassed, allowing the PLL CCO

7.8.1 UARTs

The LPC3220/30/40/50 contains seven UARTs. Four are standard UARTs, and three are high-speed UARTs.

7.8.1.1 Standard UARTs

The four standard UARTs are compatible with the INS16Cx50. These UARTs support rates up to 460800 bit/s from a 13 MHz peripheral clock.

Features

- Each standard UART has 64 byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 16, 32, 48, and 60 Bytes.
- Transmitter FIFO trigger points at 0, 4, 8, and 16 Bytes.
- Register locations conform to the “550” industry standard.
- Each standard UART has a fractional rate pre-divider and an internal baud rate generator.
- The standard UARTs support three clocking modes: on, off, and auto-clock. The auto-clock mode shuts off the clock to the UART when it is idle.
- UART 6 includes an IrDA mode to support infrared communication.
- The standard UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800) bit/s.
- Each UART includes an internal loopback mode.

7.8.1.2 High-speed UARTs

The three high-speed UARTs are designed to support rates up to 921600 bit/s from a 13 MHz peripheral clock for on-board communication in low noise conditions. This is accomplished by changing the over sampling from 16× to 14× and altering the rate generation logic.

Features

- Each high-speed UART has 64-byte Receive and Transmit FIFOs.
- Receiver FIFO trigger points at 1, 4, 8, 16, 32, and 48 B.
- Transmitter FIFO trigger points at 0, 4, and 8 B.
- Each high-speed UART has an internal baud rate generator.
- The high-speed UARTs are designed to support data rates of (2400, 4800, 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600) bit/s.
- The three high speed UARTs only support (8N1) 8-bit data word length, 1-stop bit, no parity, and no flow control as a the communications protocol.
- Each UART includes an internal loopback mode.

7.8.2 SPI serial I/O controller

The LPC3220/30/40/50 has two Serial Peripheral Interfaces (SPI). The SPI is a 3-wire serial interface that is able to interface with a large range of serial peripheral or memory devices (SPI mode 0 to 3 compatible slave devices).

There is a separate slave transmit FIFO. The slave transmit FIFO (TXS) and its level are only available when the controller is configured as a Master/Slave device and is operating in a multi-master environment. Separate TX FIFOs are needed in a multi-master because a controller might have a message queued for transmission when an external master addresses it to be come a slave-transmitter, a second source of data is needed.

Note that the I^2C clock must be enabled in the I2CCLK_CTRL register before using the I^2C. The I^2C clock can be disabled between communications, if used as a single master I^2C-bus interface, software has full control of when I^2C communication is taking place on the bus.

7.8.4.1 Features

- The two I^2C-bus blocks are standard I^2C-bus compliant interfaces that may be used in Single-master, Multi-master or Slave modes.
- Programmable clock to allow adjustment of I^2C-bus transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

7.8.5 I^2S-bus audio controller

The I^2S-bus provides a standard communication interface for digital audio applications The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. Each I^2S connection can act as a master or a slave. The master connection determines the frequency of the clock line and all other slaves are driven by this clock source. The two I^2S-bus interfaces on the LPC3220/30/40/50 provides a separate transmit and receive channel, providing a total of two transmit channels and two receive channels. Each I^2S channel supports monaural or stereo formatted data.

7.8.5.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- Supports standard sampling frequencies (8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz).
- Word select period can be configured in master mode (separately for I^2S input and output).
- Two eight-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop, and mute options separately for I^2S input and I^2S output.

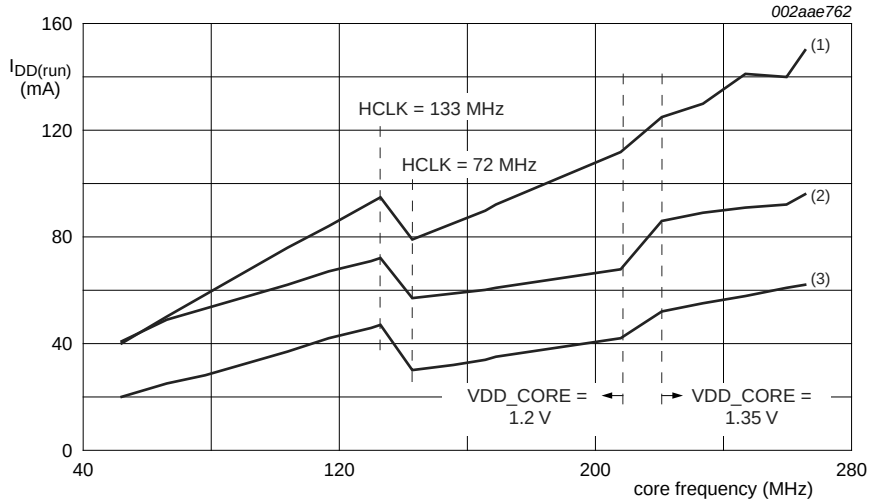
Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(RTC)}$	RTC supply current	normal operation; VDD_RTC = VDD_RTCCORE = VDD_RTCOSC = 1.2 V; T_{amb} = 25 °C	[8]	-	13	-	μA
		RTC back up operation; Rev "-" silicon	[9]	-	30	-	μA
		Rev "A" silicon	[9]	-	4	-	
I_{DD}	supply current	for HCLK; PLL output frequency = 266 MHz; VDD_PLLHCLK = 1.2 V		-	2	-	mA
		for USB; VDD_PLLUSB = 1.2 V		-	2	-	mA
		for ADC; interrupt driven loop converting ADIN[2:0]; VDD_AD = 3.3 V		-	< 1	-	mA
Input pins and I/O pins configured as input							
V_I	input voltage		[10][12]	0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		0.7 × $V_{DD(IO)}$	-	-	V
		3.3 V inputs		0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	0.3 × $V_{DD(IO)}$	V
		3.3 V inputs		-	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage	1.8 V inputs		0.1 × $V_{DD(IO)}$	-	-	V
		3.3 V inputs		0.1 × $V_{DD(IO)}$	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	μA
I_{IH}	HIGH-level input current	V_I = $V_{DD(IO)}$; no pull-down	[10]	-	-	1	μA
I_{latch}	I/O latch-up current	−(1.5$V_{DD(IO)}$) < V_I < (1.5$V_{DD(IO)}$)	[10]	-	-	100	mA
I_{pu}	pull-up current	1.8 V inputs with pull-up; V_I = 0 V		6	12	22	μA
		3.3 V inputs with pull-up; V_I = 0 V		25	50	80	μA
I_{pd}	pull-down current	1.8 V inputs with pull-down; V_I = $V_{DD(IO)}$		5	12	22	μA
		3.3 V inputs with pull-down; V_I = $V_{DD(IO)}$		25	50	85	μA
I_I	input current	bus keeper inputs; V_I = V_{DD}		-	-	1	μA
		V_I = 0.67 × V_{DD}		-	-	55	μA
		V_I = 0.33 × V_{DD}		-	-	60	μA
		V_I = 0 V		-	-	1	μA
C_i	input capacitance	Excluding bonding pad capacitance		-	-	3.3	pF

10.4 Power consumption in Run mode

Power consumption is shown in Figure 5 for WinCE applications running under typical conditions from SDRAM. MMU and I-cache/D-cache are enabled. The VFP is turned on but not used. I^2S-interface (channel 1), LCD, SLC NAND controller, I^2C1-bus, SD card, touchscreen ADC, and UART 3 are turned on. All other peripherals are turned off.

The AHB clock HCLK is identical to the core clock for frequencies up to 133 MHz, which is the maximum allowed HCLK frequency. For higher core frequencies, the HCLK PLL output must be divided by 2 to obtain an HCLK frequency lower than or equal to 133 MHz resulting in correspondingly lower power consumption by the AHB peripherals.



Conditions: T_{amb} = 25 °C; VDD_CORE = 1.2 V for core frequencies ≤ 208 MHz; VDD_CORE = 1.35 V for core frequencies > 208 MHz; $V_{DD(IO)}$ = 1.8 V.

(1) WinCE running from SDRAM; playing wmv file at 20 frames/s, 32 kHz mono.

(2) WinCE running from SDRAM; playing mp3 file at 128 kbit/s, stereo.

(3) WinCE running from SDRAM; no application running.

Fig 5. Core current versus core frequency for WinCE applications

10.5 ADC static characteristics

Table 10. ADC static characteristics

$V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C unless otherwise specified; ADC clock frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	±0.5	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	±0.6	±1	LSB
E_O	offset error		[1][5]	-	±1	±3	LSB
E_G	gain error		[1][6]	-	±0.3	±0.6	%
E_T	absolute error		[1][7]	-		±4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V (on pin VSS_AD); $V_{DDA(3V3)}$ = 3.3 V (on pin VDD_AD).

[2] The ADC is monotonic; there are no missing codes.

[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 6.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 6.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 6.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 6.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 6.

Table 12. Dynamic characteristics: static external memory interface *…continued*
C_L = 25 pF, T_{amb} = 20 °C, $V_{DD(EMC)}$ = 1.8 V, 2.5 V, or 3.3 V.

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns

[1] T_{CLCL} = 1/HCLK

[2] Refer to the *LPC32x0 User manual* EMCStaticWaitOen0-3 register for the programming of WAITOEN value.

[3] Refer to the *LPC32x0 User manual* EMCStaticWaitRd0-3 register for the programming of WAITRD value.

[4] Refer to the *LPC32x0 User manual* EMCStaticWaitWen0-3 register for the programming of WAITWEN value.

[5] Refer to the *LPC32x0 User manual* EMCStaticWaitWr0-3 register for the programming of WAITWR value.

[6] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

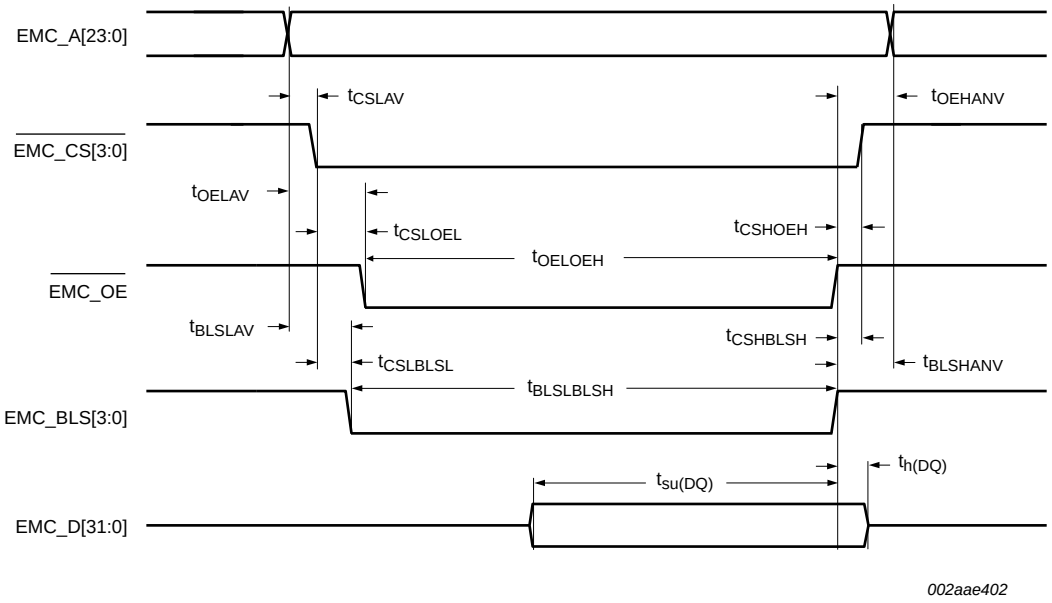


Fig 7. External memory read access

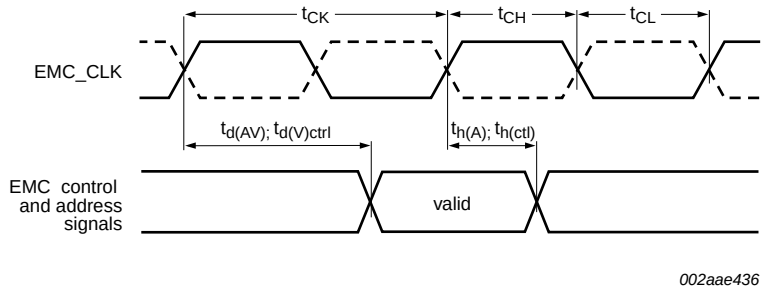


Fig 10. DDR control timing parameters

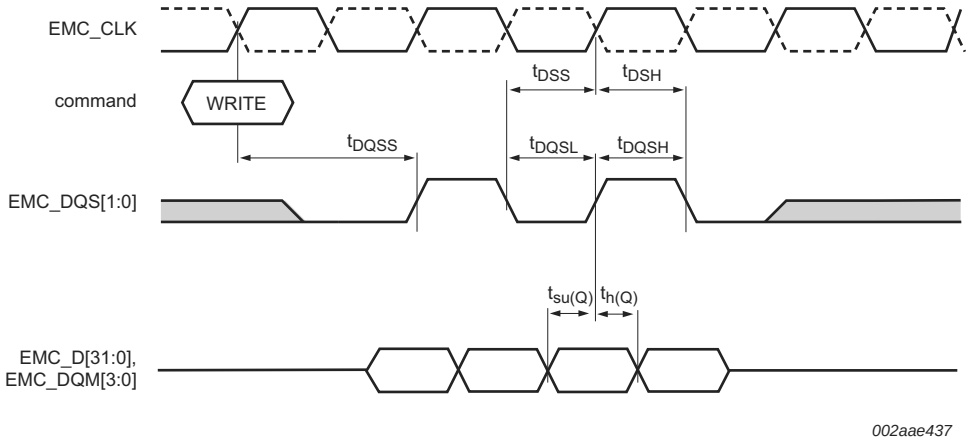
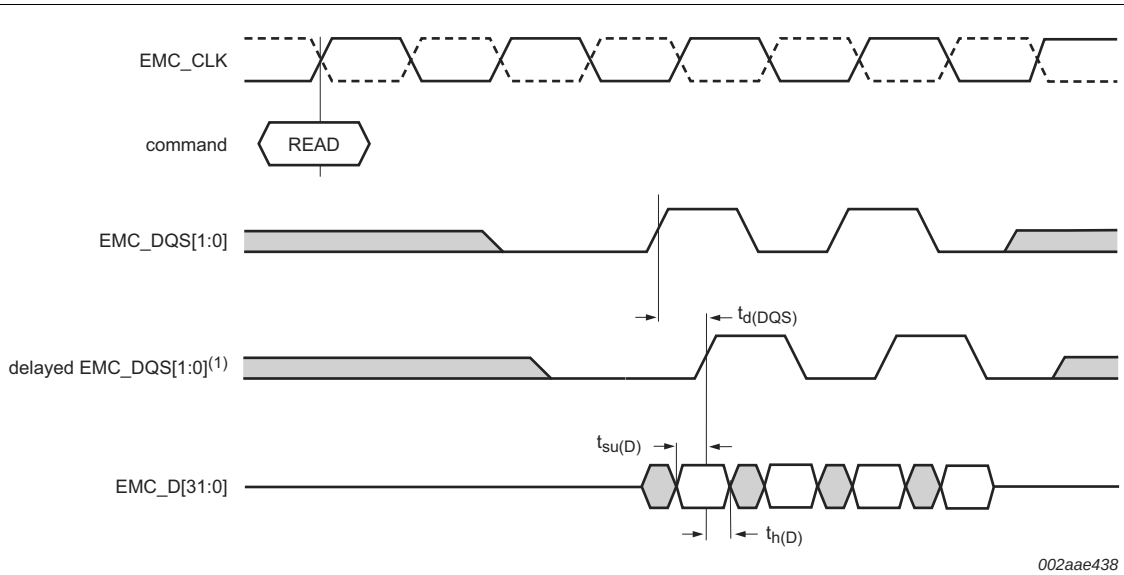


Fig 11. DDR write timing parameters



(1) The delay of the EMC_DQS[1:0] signal is determined by the DQS_DELAY settings. See *LPC32x0 User manual, External Memory Controller Chapter, section DDR DQS delay calibration* for details on configuring this value.

Fig 12. DDR read timing parameters

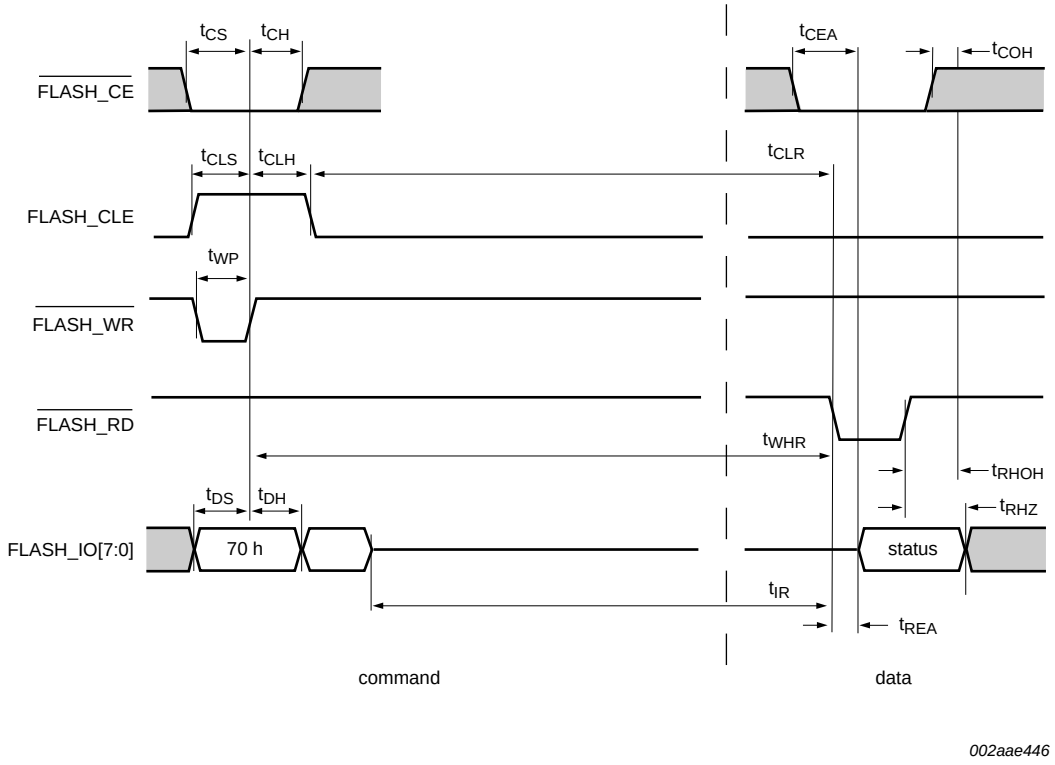


Fig 19. MLC NAND flash memory status timing

11.9 SPI and SSP Controller

11.9.1 SPI

Table 19. Dynamic characteristics of SPI pins on SPI master controller
T_{amb} = −40 °C to +85 °C.

Symbol	Parameter		Min	Typ	Max	Unit
Common to SPI1 and SPI2						
T_{SPICYC}	SPI cycle time	[1]	2 × T_{HCLK}	-	256 × T_{HCLK}	ns
SPI1						
t_{SPIDSU}	SPI data set-up time		-	6	-	ns
t_{SPIDH}	SPI data hold time		-	0	-	ns
t_{SPIDV}	SPI enable to output data valid time		-	2	-	ns
t_{SPIOH}	SPI output data hold time		-	0	-	ns
SPI2						
t_{SPIDSU}	SPI data set-up time		-	10	-	ns
t_{SPIDH}	SPI data hold time		-	0	-	ns
t_{SPIDV}	SPI enable to output data valid time		-	2	-	ns
t_{SPIOH}	SPI output data hold time		-	0	-	ns

[1] T_{HCLK} = period time of SPI IP block input clock (HCLK)

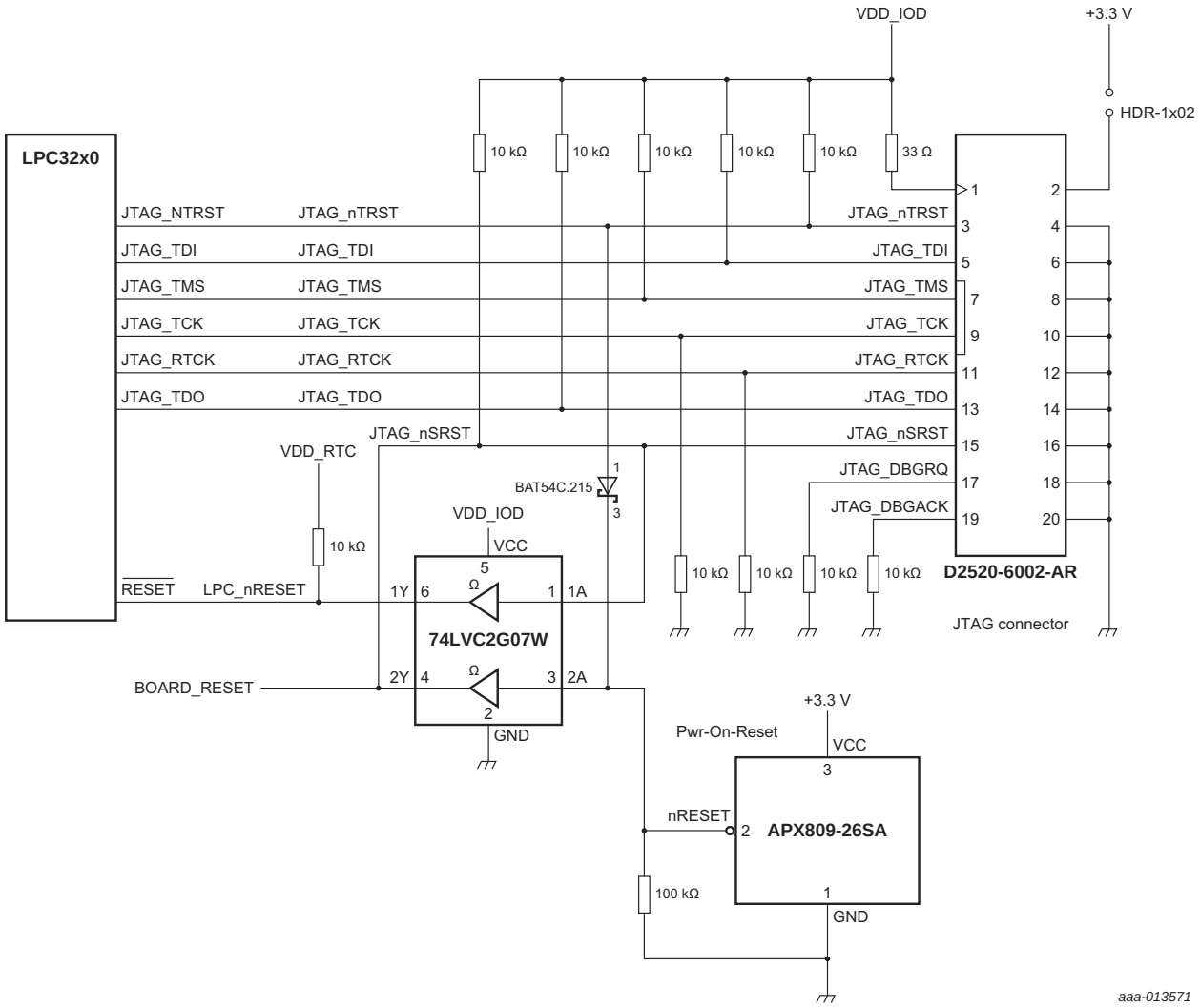
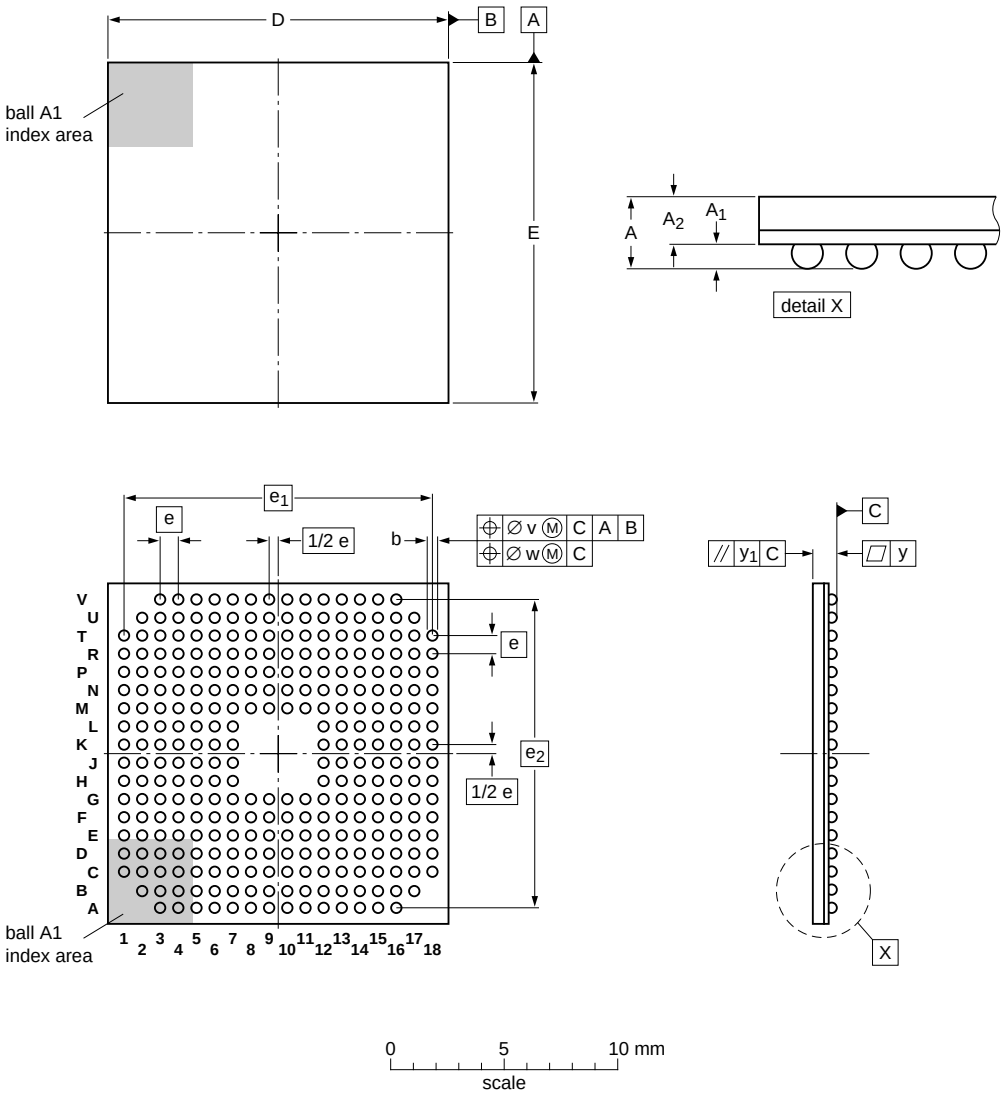


Fig 24. Circuit for holding JTAG_NTRST LOW during POR

13. Package outline

TFBGA296: plastic thin fine-pitch ball grid array package; 296 balls **SOT1048-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	1.2	0.4 0.3	0.80 0.65	0.5 0.4	15.1 14.9	15.1 14.9	0.8	13.6	13.6	0.15	0.08	0.12	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT1048-1		MO-216				~~07-10-19~~ 07-11-02

Fig 25. Package outline SOT1048-1 (TFBGA296)

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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