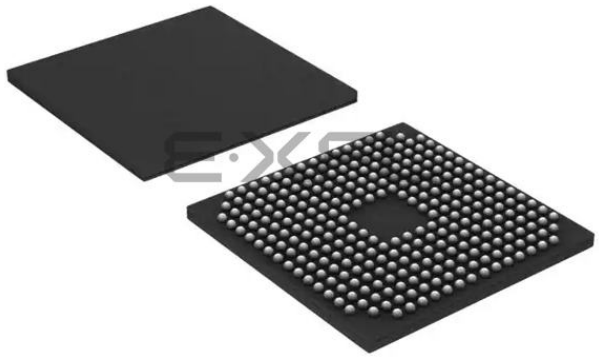


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Discontinued at Digi-Key
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3250fet296-01-5

Table 3. Pin allocation table (TFBGA296)

Pin	Symbol	Pin	Symbol	Pin	Symbol
C10	SPI1_DATIN/MISO0/GPI_25/ MCI1	C11	GPIO_3/KEY_ROW7/ ENET_MDIO[2]	C12	GPO_9/LCDVD[9][1]
C13	GPO_8/LCDVD[8][1]	C14	GPI_2/CAP2[0]/ ENET_RXD3[2]	C15	GPI_1/$\overline{\text{SERVICE}}$
C16	GPI_0/I2S1RX_SDA	C17	KEY_ROW4/ENET_TXD0[2]	C18	KEY_ROW5/ENET_TXD1[2]
Row D					
D1	FLASH_RDY	D2	FLASH_ALE	D3	GPO_14
D4	GPO_1	D5	USB_DAT_VP/U5_RX	D6	$\overline{\text{USB\_OE\_TP}}$
D7	P0[1]/I2S1RX_WS	D8	GPO_4	D9	GPIO_2/KEY_ROW6/ENET_MDC[2]
D10	GPO_16/MCOB0/LCDENAB[1]/ LCDM[1]	D11	GPO_18/MCOA0/LCDLP[1]	D12	GPO_3/LCDVD[1][1]
D13	GPI_7/CAP4[0]/$\overline{\text{MCABORT}}$	D14	PWM_OUT1/LCDVD[16][1]	D15	PWM_OUT2/INTSTAT/LCDVD[19][1]
D16	KEY_ROW3/ENET_TX_EN[2]	D17	KEY_COL2/ENET_RX_ER[2]	D18	KEY_COL3/ENET_CRS[2]
Row E					
E1	FLASH_IO[3]	E2	FLASH_IO[7]	E3	$\overline{\text{FLASH\_CE}}$
E4	I2C2_SDA	E5	USB_I2C_SCL	E6	USB_I2C_SDA
E7	I2S1TX_SDA/MAT3[1]	E8	GPO_11	E9	GPIO_5/SSEL0/MCI0
E10	GPO_22/U7_HRTS/ LCDVD[14][1]	E11	GPO_10/MCOB2/LCDPWR[1]	E12	GPI_9/KEY_COL7/ENET_COL[2]
E13	GPI_4/SPI1_BUSY	E14	KEY_ROW1/ENET_TXD2[2]	E15	KEY_ROW0/ENET_TX_ER[2]
E16	KEY_COL1/ENET_RX_CLK[2]/ ENET_REF_CLK[2]	E17	U7_RX/CAP0[0]/ LCDVD[10][1]/GPI_23	E18	U7_TX/MAT1[1]/LCDVD[11][1]
Row F					
F1	FLASH_IO[2]	F2	$\overline{\text{FLASH\_WR}}$	F3	FLASH_CLE
F4	GPI_3	F5	VSS_IOC	F6	VSS_IOB
F7	VDD_IOC	F8	VDD_IOB	F9	VDD_IOD
F10	VSS_IOD	F11	VSS_IOD	F12	VSS_IOD
F13	VDD_IOD	F14	KEY_ROW2/ENET_TXD3[2]	F15	KEY_COL0/ENET_TX_CLK[2]
F16	KEY_COL5/ENET_RXD1[2]	F17	U6_IRRX/GPI_21	F18	U5_RX/GPI_20
Row G					
G1	$\overline{\text{EMC\_DYCS1}}$	G2	FLASH_IO[5]	G3	FLASH_IO[6]
G4	$\overline{\text{RESOUT}}$	G5	VSS_IOC	G6	VDD_IOC
G7	VDD_CORE	G8	VSS_CORE	G9	VDD_CORE
G10	VSS_CORE	G11	VDD_CORE	G12	VSS_CORE
G13	U7_HCTS/CAP0[1]/ LCDCLKIN[1]/GPI_22	G14	DBGEN	G15	KEY_COL4/ENET_RXD0[2]
G16	U6_IRTX	G17	SYSCLKEN/LCDVD[15][1]	G18	JTAG_TMS
Row H					
H1	$\overline{\text{EMC\_OE}}$	H2	FLASH_IO[0]	H3	FLASH_IO[1]
H4	FLASH_IO[4]	H5	VSS_IOC	H6	VDD_IOC
H7	VSS_CORE				
				H12	VSS_IOD
H13	VDD_IOA	H14	JTAG_TCK	H15	U5_TX

6.2 Pin description

Table 4. Pin description

Symbol	Pin	Power supply domain	Type	Description
ADIN0/TS_YM	U15	VDD_AD	analog in	ADC input 0/touch screen Y minus
ADIN1/TS_XM	T14	VDD_AD	analog in	ADC input 0/touch screen X minus
ADIN2/TS_AUX_IN	V16	VDD_AD	analog in	ADC input 2/touch screen AUX input
DBGEN	G14	VDD_IOD	I: PD	Device test input LOW = JTAG in-circuit debug available; normal operation. HIGH = I/O cell boundary scan test; for board assembly BSDL test.
EMC_A[0]/P1[0]	L3	VDD_EMC	I/O	EMC address bit 0
			I/O	Port 1 GPIO bit 0
EMC_A[1]/P1[1]	L4	VDD_EMC	I/O	EMC address bit 1
			I/O	Port 1 GPIO bit 1
EMC_A[2]/P1[2]	M1	VDD_EMC	I/O	EMC address bit 2
			I/O	Port 1 GPIO bit 2
EMC_A[3]/P1[3]	M2	VDD_EMC	I/O	EMC address bit 3
			I/O	Port 1 GPIO bit 3
EMC_A[4]/P1[4]	M3	VDD_EMC	I/O	EMC address bit 4
			I/O	Port 1 GPIO bit 4
EMC_A[5]/P1[5]	N1	VDD_EMC	I/O	EMC address bit 5
			I/O	Port 1 GPIO bit 5
EMC_A[6]/P1[6]	N2	VDD_EMC	I/O	EMC address bit 6
			I/O	Port 1 GPIO bit 6
EMC_A[7/P1[7]	N3	VDD_EMC	I/O	EMC address bit 7
			I/O	Port 1 GPIO bit 7
EMC_A[8]/P1[8]	M4	VDD_EMC	I/O	EMC address bit 8
			I/O	Port 1 GPIO bit 8
EMC_A[9]/P1[9]	P1	VDD_EMC	I/O	EMC address bit 9
			I/O	Port 1 GPIO bit 9
EMC_A[10]/P1[10]	P2	VDD_EMC	I/O	EMC address bit 10
			I/O	Port 1 GPIO bit 10
EMC_A[11]/P1[11]	P3	VDD_EMC	I/O	EMC address bit 11
			I/O	Port 1 GPIO bit 11
EMC_A[12]/P1[12]	N4	VDD_EMC	I/O	EMC address bit 12
			I/O	Port 1 GPIO bit 12
EMC_A[13]/P1[13]	R1	VDD_EMC	I/O	EMC address bit 13
			I/O	Port 1 GPIO bit 13
EMC_A[14]/P1[14]	R2	VDD_EMC	I/O	EMC address bit 14
			I/O	Port 1 GPIO bit 14

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
GPI_7/CAP4[0]/ $\overline{\text{MCABORT}}$	D13	VDD_IOD	I	General purpose input 7
			I	Timer 4 capture input 0
			I	Motor control PWM LOW-active fast abort input
GPI_8/KEY_COL6/ SPI2_BUSY/ ENET_RX_DV	B16	VDD_IOD	I	General purpose input 8
			I	Keyscan column 6 input
			I	SPI2 busy input
			I	Ethernet receive data valid input (LPC3240 and LPC3250 only)
GPI_9/KEY_COL7/ ENET_COL	E12	VDD_IOD	I	General purpose input 9
			I	Keyscan column 7 input
			I	Ethernet collision input (LPC3240 and LPC3250 only)
GPI_19/U4_RX	B15	VDD_IOD	I	General purpose input 19
			I	UART 4 receive
GPI_28/U3_RI	N17	VDD_IOA	I	General purpose input 28
			I	UART 3 ring indicator input
GPIO_0	A12	VDD_IOD	I/O	General purpose input/output 0
GPIO_1	A11	VDD_IOD	I/O	General purpose input/output 1
GPIO_2/ KEY_ROW6/ ENET_MDC	D9	VDD_IOD	I/O	General purpose input/output 2
			O	Keyscan row 6 output
			O	Ethernet PHY interface clock (LPC3240 and LPC3250 only)
GPIO_3/ KEY_ROW7/ ENET_MDIO	C11	VDD_IOD	I/O	General purpose input/output 3
			I/O	Keyscan row 7 output
			I/O	Ethernet PHY interface data (LPC3240 and LPC3250 only)
GPIO_4/ SSEL1/ LCDVD[22]	B11	VDD_IOD	I/O	General purpose input/output 4
			I/O	SSP1 Slave Select
			I/O	LCD data bit 22 (LPC3230 and LPC3250 only)
GPIO_5/ SSEL0/ MCI0	E9	VDD_IOD	I/O	General purpose input/output 5
			I/O	SSP0 Slave Select
			I/O	Motor control channel 0 input
GPO_0/ TST_CLK1	C3	VDD_IOC	O	General purpose output 0
			O	Test clock 1 out
GPO_1	D4	VDD_IOC	O	General purpose output 1
GPO_2/ MAT1[0]/ LCDVD[0]	B14	VDD_IOD	O	General purpose output 2
			O	Timer 1 match output 0
			O	LCD data bit 0 (LPC3230 and LPC3250 only)
GPO_3/ LCDVD[1]	D12	VDD_IOD	O	General purpose output 3
			O	LCD data bit 1 (LPC3230 and LPC3250 only)
GPO_4	D8	VDD_IOB	O	General purpose output 4

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
P0[1]/ I2S1RX_WS	D7	VDD_IOB	I/O	Port 0 GPIO bit 1
			I/O	I^2S1 receive word select
P0[2]/ I2S0RX_SDA/ LCDVD[4]	M17	VDD_IOA	I/O	Port 0 GPIO bit 2
			I/O	I^2S0 receive data
			I/O	LCD data bit 4 (LPC3230 and LPC3250 only)
P0[3]/ I2S0RX_CLK/ LCDVD[5]	M18	VDD_IOA	I/O	Port 0 GPIO bit 3
			I/O	I^2S0 receive clock
			I/O	LCD data bit 5 (LPC3230 and LPC3250 only)
P0[4]/ I2S0RX_WS/ LCDVD[6]	L15	VDD_IOA	I/O	Port 0 GPIO bit 4
			I/O	I^2S0 receive word select
			I/O	LCD data bit 6 (LPC3230 and LPC3250 only)
P0[5]/ I2S0TX_SDA/ LCDVD[7]	L16	VDD_IOA	I/O	Port 0 GPIO bit 5
			I/O	I^2S0 transmit data
			I/O	LCD data bit 7 (LPC3230 and LPC3250 only)
P0[6]/ I2S0TX_CLK/ LCDVD[12]	L17	VDD_IOA	I/O	Port 0 GPIO bit 6
			I/O	I^2S0 transmit clock
			I/O	LCD data bit 12 (LPC3230 and LPC3250 only)
P0[7]/ I2S0TX_WS/ LCDVD[13]	L18	VDD_IOA	I/O	Port 0 GPIO bit 7
			I/O	I^2S0 transmit word select
			I/O	LCD data bit 13 (LPC3230 and LPC3250 only)
PLL397_LOOP	R14	VDD_PLL397	analog filter	PLL397 loop filter (for external components)
PWM_OUT1/ LCDVD[16]	D14	VDD_IOD	O	PWM1 out
			O	LCD data bit 16 (LPC3230 and LPC3250 only)
PWM_OUT2/INTSTAT/ LCDVD[19]	D15	VDD_IOD	O	PWM2 output/internal interrupt status[1]
			O	LCD data bit 19 (LPC3230 and LPC3250 only)
$\overline{\text{RESET}}$	M14	VDD_RTC	I	Reset input, active LOW
$\overline{\text{RESOUT}}$	G4	VDD_IOC	O	Reset out. Reflects external and WDT reset
RTCX_IN	P16	VDD_RTC	analog in	RTC oscillator input
RTCX_OUT	P17	VDD_RTC	analog out	RTC oscillator output
SPI1_CLK/ SCK0	C9	VDD_IOD	O	SPI1 clock out
			O	SSP0 clock out
SPI1_DATIN/ MISO0/ GPI_25/ MCI1	C10	VDD_IOD	I/O	SPI1 data in
			I/O	SSP0 MISO
			I/O	General purpose input bit 25
			I	Motor control channel 1 input
SPI1_DATIO/ MOSI0/ MCI2	B9	VDD_IOD	I/O	SPI1 data out (and optional input)
			I/O	SSP0 MOSI
			I	Motor control channel 2 input

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
VSS_PLLUSB	R16	-	power	Ground for USB PLL
VSS_RTCCORE	L14	-	power	Ground for RTC
VSS_RTCOSC	P18	-	power	Ground for RTC oscillator

[1] The PWM2_CTRL register controls this pin function (see *LPC32x0 User manual*).

Table 5. Digital I/O pad types[1]

Parameter	Abbreviation
I/O type	I = input. O = output. I/O = bidirectional. I/O T = bidirectional or high impedance.
Pin detail	BK: pin has a bus keeper function that weakly retains the last logic level driven on an I/O pin. Bus keeper current for different I/O pin voltages: 0 V= 1 μA (max) VDD_x = 1 μA (max) 2/3 × VDD_x = 55 μA (max) 1/3 × VDD_x = 60 μA (max) PU: pin has a nominal 50 μA internal pull-up connected. PD: pin has a nominal 50 μA internal pull-down connected. P: pin has programmable input characteristics.

[1] See *LPC32x0 User manual* for details.

Table 6. Supply domains

Supply domain	Voltage range	Related supply pins	Description
VDD_CORE	0.9 V to 1.39 V	VDD_CORE	Core power domain.
VDD_COREFXD	1.2 V	VDD_COREFXD	Fixed 1.2 V supply for digital portion of the analog block.
other core domains	1.2 V	VDD_PLL397, VDD_PLLHCLK, VDD_PLLUSB, VDD_FUSE, VDD_OSC	1.2 V supplies, tied to VDD_COREFXD.
VDD_RTC	0.9 V to 1.39 V	VDD_RTC, VDD_RTCCORE, VDD_RTCOSC	RTC supply domain. Can be connected to a battery backed-up power source.
VDD_AD	2.7 V to 3.6 V	VDD_AD	3.3 V supply for ADC and touch screen.
VDD_EMC	1.7 V to 1.95 V 2.3 V to 2.7 V 2.7 V to 3.6 V	VDD_EMC	External memory interface IO pins in 1.8 V range, 2.5 V range, or 3.3 V range.

Table 6. Supply domains

Supply domain	Voltage range	Related supply pins	Description
VDD_IOA[1]	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOA	Peripheral supply.
VDD_IOB[1]	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOB	Peripheral supply.
VDD_IOC[1]	1.7 V to 1.95 V or 2.3 V to 3.6 V	VDD_IOC	Peripheral supply.
VDD_IOD[1]	1.7 V to 1.95 V or 2.7 V to 3.6 V	VDD_IOD	Peripheral supply.

[1] The VDD_IOA, VDD_IOB, VDD_IOC, and VDD_IOD supply domains can be operated at a voltage independent of the other domains as long as all pins connected to the same peripheral are at the same voltage level. There are two special cases for determining supply domain voltages (for details see *application note AN10777*):

a) Ethernet configured in MII mode: VDD_IOD must be the same as VDD_IOB.

b) UART 3 when used with hardware flow control or when sharing an RS-232 transceiver with another UART: VDD_IOA must be the same as VDD_IOD.

packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU. The Ethernet DMA can access off-chip memory via the EMC, as well as the IRAM. The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.6.2.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching. Wake-on-LAN power management support allows system wake-up using the receive filters or a magic frame detection filter.
- Physical interface
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.6.3 USB interface

The LPC3220/30/40/50 supports USB in either device, host, or OTG configuration.

7.6.3.1 USB device controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error

Only a single master and a single slave can communicate on the interface during a given data transfer. During a data transfer the master always sends a byte of data to the slave, and the slave always sends a byte of data to the master. The SPI implementation on the LPC3220/30/40/50 does not support operation as a slave.

7.8.2.1 Features

- Supports slaves compatible with SPI modes 0 to 3.
- Half duplex synchronous transfers.
- DMA support for data transmit and receive.
- 1-bit to 16-bit word length.
- Choice of LSB or MSB first data transmission.
- 64 × 16-bit input or output FIFO.
- Bit rates up to 52 Mbit/s.
- Busy input function.
- DMA time out interrupt to allow detection of end of reception when using DMA.
- Timed interrupt to facilitate emptying the FIFO at the end of a transmission.
- SPI clock and data pins may be used as general purpose pins if the SPI is not used.
- Slave selects can be supported using GPO or GPIO pins

7.8.3 SSP serial I/O controller

The LPC3220/30/40/50 contains two SSP controllers. The SSP controller is capable of operation on a SPI, 4-wire SSI, or Microwire bus. It can interact with multiple masters and slaves on the bus. Only a single master and a single slave can communicate on the bus during a given data transfer. The SSP supports full duplex transfers, with frames of 4 bits to 16 bits of data flowing from the master to the slave and from the slave to the master. In practice, often only one of these data flows carries meaningful data.

7.8.3.1 Features

- Compatible with Motorola SPI, 4-wire TI SSI, and National Semiconductor Microwire buses
- Synchronous serial communication
- Master or slave operation
- 8-frame FIFOs for both transmit and receive
- 4-bit to 16-bit frame
- Maximum SPI bus data bit rate of $\frac{1}{2}$ (Master mode) and $\frac{1}{2}$ (Slave mode) of the input clock rate
- DMA transfers supported by GPDMA

7.8.4 I^2C-bus serial I/O controller

There are two I^2C-bus interfaces in the LPC32x0 family of controllers. These I^2C blocks can be configured as a master, multi-master or slave supporting up to 400 kHz. The I^2C blocks also support 7 or 10 bit addressing. Each has a four word FIFO for both transmit and receive. An interrupt signal is available from each block.

There is a separate slave transmit FIFO. The slave transmit FIFO (TXS) and its level are only available when the controller is configured as a Master/Slave device and is operating in a multi-master environment. Separate TX FIFOs are needed in a multi-master because a controller might have a message queued for transmission when an external master addresses it to be come a slave-transmitter, a second source of data is needed.

Note that the I^2C clock must be enabled in the I2CCLK_CTRL register before using the I^2C. The I^2C clock can be disabled between communications, if used as a single master I^2C-bus interface, software has full control of when I^2C communication is taking place on the bus.

7.8.4.1 Features

- The two I^2C-bus blocks are standard I^2C-bus compliant interfaces that may be used in Single-master, Multi-master or Slave modes.
- Programmable clock to allow adjustment of I^2C-bus transfer rates.
- Bidirectional data transfer.
- Serial clock synchronization allows devices with different bit rates to communicate via one serial bus.
- Serial clock synchronization can be used as a handshake mechanism to suspend and resume serial transfer.

7.8.5 I^2S-bus audio controller

The I^2S-bus provides a standard communication interface for digital audio applications The I^2S-bus specification defines a 3-wire serial bus using one data line, one clock line, and one word select signal. Each I^2S connection can act as a master or a slave. The master connection determines the frequency of the clock line and all other slaves are driven by this clock source. The two I^2S-bus interfaces on the LPC3220/30/40/50 provides a separate transmit and receive channel, providing a total of two transmit channels and two receive channels. Each I^2S channel supports monaural or stereo formatted data.

7.8.5.1 Features

- The interface has separate input/output channels each of which can operate in master or slave mode.
- Capable of handling 8-bit, 16-bit, and 32-bit word sizes.
- Mono and stereo audio data supported.
- Supports standard sampling frequencies (8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 96 kHz).
- Word select period can be configured in master mode (separately for I^2S input and output).
- Two eight-word FIFO data buffers are provided, one for transmit and one for receive.
- Generates interrupt requests when buffer levels cross a programmable boundary.
- Two DMA requests, controlled by programmable buffer levels. These are connected to the GPDMA block.
- Controls include reset, stop, and mute options separately for I^2S input and I^2S output.

Two 32-bit match registers are readable and writable by the processor. A match will result in an interrupt provided that the interrupt is enabled. The ONSW output pin can also be triggered by a match event and cause an external power supply to turn on all of the operating voltages, as a way to startup after power has been removed.

The RTC block is implemented in a separate voltage domain. The block is supplied via a separate supply pin from a battery or other power source.

The RTC block also contains 32 words (128 bytes) of very low voltage SRAM. This SRAM is able to hold its contents down to the minimum RTC operating voltage.

7.9.4.1 Features

- Measures the passage of time in seconds.
- 32-bit up and down seconds counters.
- Ultra-low power design to support battery powered systems.
- Dedicated 32 kHz oscillator.
- An output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC.
- Two 32-bit match registers with interrupt option.
- 32 words (128 bytes) of very low voltage SRAM.
- The RTC and battery RAM power have an independent power domain and dedicated supply pins, which can be powered from a battery or power supply.

Remark: The LPC3220/30/40/50 will run at voltages down to 0.9 V at frequencies below 14 MHz. However, the ARM core cannot access the RTC registers and battery RAM when the core supply voltage is at 0.9 V and the RTC supply is at 1.2 V.

7.9.5 Enhanced 32-bit timers/external event counters

The LPC3220/30/40/50 includes six 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.9.5.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit pre-scaler.
- Counter or Timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - continuous operation with optional interrupt generation on match
  - stop timer on match with optional interrupt generation
  - reset timer on match with optional interrupt generation
- Up to four external outputs corresponding to match registers, with the following capabilities:

- set LOW on match
- set HIGH on match
- toggle on match
- do nothing on match

7.9.6 High-speed timer

The high-speed timer block is clocked by the main peripheral clock. The clock is first divided down in a 16-bit programmable pre-scale counter which clocks a 32-bit timer/counter.

The high-speed timer includes three match registers that are compared to the timer/counter value. A match can generate an interrupt and cause the timer/counter to either continue to run, stop, or be reset. The high-speed timer also includes two capture registers that can take a snapshot of the timer/counter value when an input signal transitions. A capture event may also generate an interrupt.

7.9.6.1 Features

- 32-bit timer/counter with programmable 16-bit pre-scaler.
- Counter or timer operation.
- Two 32-bit capture registers.
- Three 32-bit match registers that allow:
  - Continuous operation with optional interrupt generation on match.
  - Stop timer on match with optional interrupt generation.
  - Reset timer on match with optional interrupt generation.
- Pause control to stop counting when core is in debug state.

7.9.7 Pulse Width Modulators (PWMs)

The LPC3220/30/40/50 provides two simple PWMs. They are clocked separately by either the main peripheral clock or the 32 kHz RTC clock. Both PWMs have a duty cycle programmable in 255 steps.

7.9.7.1 Features

- Clocked by the main peripheral clock or the 32 kHz RTC clock.
- Programmable 4-bit pre-scaler.
- Duty cycle programmable in 255 steps.
- Output frequency up to 50 kHz when using a 13 MHz peripheral clock.

7.9.8 Motor control pulse width modulator

The Motor Control PWM (MCPWM) provides a set of features for three-phase AC and DC motor control applications in a single peripheral. The MCPWM can also be configured for use in other generalized timing, counting, capture, and compare applications.

7.9.8.1 Features

- 32-bit timer
- 32-bit period register

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Power consumption in Run, direct Run, and Stop modes							
$I_{DD(run)}$	Run mode supply current	T_{amb} = 25 °C; code `while(1){}` executed from IRAM; all peripherals enabled					
		I-cache/D-cache, MMU enabled; CPU clock = 208 MHz; VDD_CORE = 1.2 V		-	150	-	mA
		I-cache/D-cache, MMU enabled; CPU clock = 266 MHz; VDD_CORE = 1.35 V		-	218	-	mA
		I-cache/D-cache, MMU disabled; CPU clock = 208 MHz; VDD_CORE = 1.2 V		-	78	-	mA
		I-cache/D-cache, MMU disabled; CPU clock = 266 MHz; VDD_CORE = 1.35 V		-	111	-	mA
$I_{DD(drun)}$	direct Run mode supply current	T_{amb} = 25 °C; CPU clock = 13 MHz; code `while(1){}` executed from IRAM; all peripherals disabled					
		I-cache/D-cache, MMU enabled; VDD_CORE = 1.2 V		-	7.8	-	mA
		I-cache/D-cache, MMU enabled; VDD_CORE = 0.9 V		-	5.6	-	mA
		I-cache/D-cache, MMU disabled; VDD_CORE = 1.2 V		-	5	-	mA
		I-cache/D-cache, MMU disabled; VDD_CORE = 0.9 V		-	3.5	-	mA
$I_{DD(stop)}$	Stop mode supply current	T_{amb} = 25 °C; CPU clock stopped internally; all peripherals disabled					
		VDD_CORE = 1.2 V		-	400	-	μA
		VDD_CORE = 0.9 V		-	400	-	μA

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{IH}	HIGH-level input current	$V_I = V_{DD}$; no pull-down	[10]	-	-	1	μA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD}$; no pull-up/down	[10]	-	-	1	μA
I_{latch}	I/O latch-up current	$-(1.5V_{DD}) < V_I < (1.5V_{DD})$	[10]	-	-	100	mA

[1] Typical ratings are not guaranteed. The values listed are at room temperature (25 °C), nominal supply voltages.

[2] Applies to VDD_CORE pins.

[3] Applies to pins VDD_RTC, VDD_RTCCORE, and VDD_RTCOSC.

[4] Applies to pins VDD_COREFXD, VDD_OSC, VDD_PLL397, VDD_PLLHCLK, and VDD_PLLUSB.

[5] Applies when using 1.8 V Mobile DDR or Mobile SDR SDRAM.

[6] Applies when using 2.5 V DDR memory.

[7] Applies when using 3.3 V SDR SDRAM and SRAM.

[8] Specifies current on combined VDD_RTCx during normal chip operation: VDD_RTC, VDD_CORE, VDD_OSC = 1.2 V and VDD_CORE, VDD_IOx at typical voltage.

[9] Specifies current on combined VDD_RTCx during backup operation: VDD_RTC, VDD_CORE, VDD_OSC = 1.2 V and all other VDD_x at 0 V.

[10] Referenced to the applicable V_{DD} for the pin.

[11] Including voltage on outputs in 3-state mode.

[12] The applicable V_{DD} voltage for the pin must be present.

[13] 3-state outputs go into 3-state mode when the applicable V_{DD} voltage for the pin is grounded.

[14] Accounts for 100 mV voltage drop in all supply lines.

[15] Allowed as long as the current limit does not exceed the maximum current allowed by the device.

10.1 Minimum core voltage requirements

Figure 4 shows the minimum core supply voltage that should be applied for a given core frequency on pin VDD_CORE to ensure stable operation of the LPC3220/30/40/50.

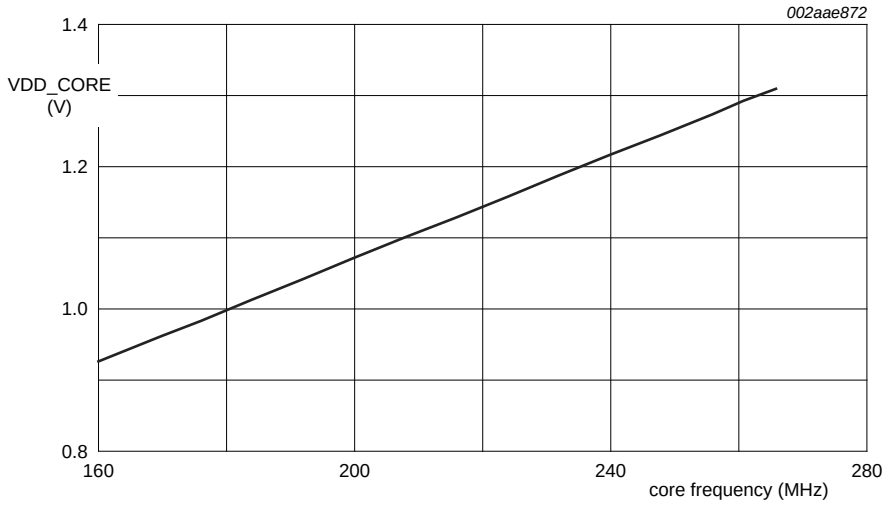


Fig 4. Minimum required core supply voltage for different core frequencies

10.2 Power supply sequencing

The LPC32x0 has no power sequencing requirements, that is, $V_{DD(1V2)}$, $V_{DD(EMC)}$, $V_{DD(IO)}$, and $V_{DDA(3V3)}$ can be switched on or off independent of each other. An internal circuit ensures that the system correctly powers up in the absence of core power. During IO power-up this circuit takes care that the system is powered in a defined mode. The same is valid for core power-down.

10.3 Power consumption per peripheral

Table 9. Power consumption per peripheral

T_{amb} = 25 °C; CPU clock = 208 MHz; I-cache/D-cache, MMU disabled; VDD_CORE = 1.2 V; $V_{DD(IO)}$ = 1.8 V; USB AHB, IRAM, and IROM clocks always on; all peripherals are at their default state at reset. Peripheral clocks are disabled except for peripheral measured.

Peripheral	$I_{DD(run)}$ / mA
High-speed UART (set to 115 200 Bd (8N1))	0.3
I^2C-bus	0.3
SSP	0.6
I^2S	0.5
DMA	6.3
EMC	7.3
Multi-level NAND controller	1.4
Single-level NAND controller	0.3
LCD	5.6
Ethernet MAC[1]	2.9

[1] All three Ethernet clocks are in enabled in the MAC_CLK_CTRL register (see *LPC32x0 User manual*).

10.5 ADC static characteristics

Table 10. ADC static characteristics

$V_{DDA(3V3)}$ = 3.3 V; T_{amb} = 25 °C unless otherwise specified; ADC clock frequency 4.5 MHz.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IA}	analog input voltage			0	-	$V_{DDA(3V3)}$	V
C_{ia}	analog input capacitance			-	-	1	pF
E_D	differential linearity error		[1][2][3]	-	±0.5	±1	LSB
$E_{L(adj)}$	integral non-linearity		[1][4]	-	±0.6	±1	LSB
E_O	offset error		[1][5]	-	±1	±3	LSB
E_G	gain error		[1][6]	-	±0.3	±0.6	%
E_T	absolute error		[1][7]	-		±4	LSB
R_{vsi}	voltage source interface resistance			-	-	40	kΩ

[1] Conditions: V_{SSA} = 0 V (on pin VSS_AD); $V_{DDA(3V3)}$ = 3.3 V (on pin VDD_AD).

[2] The ADC is monotonic; there are no missing codes.

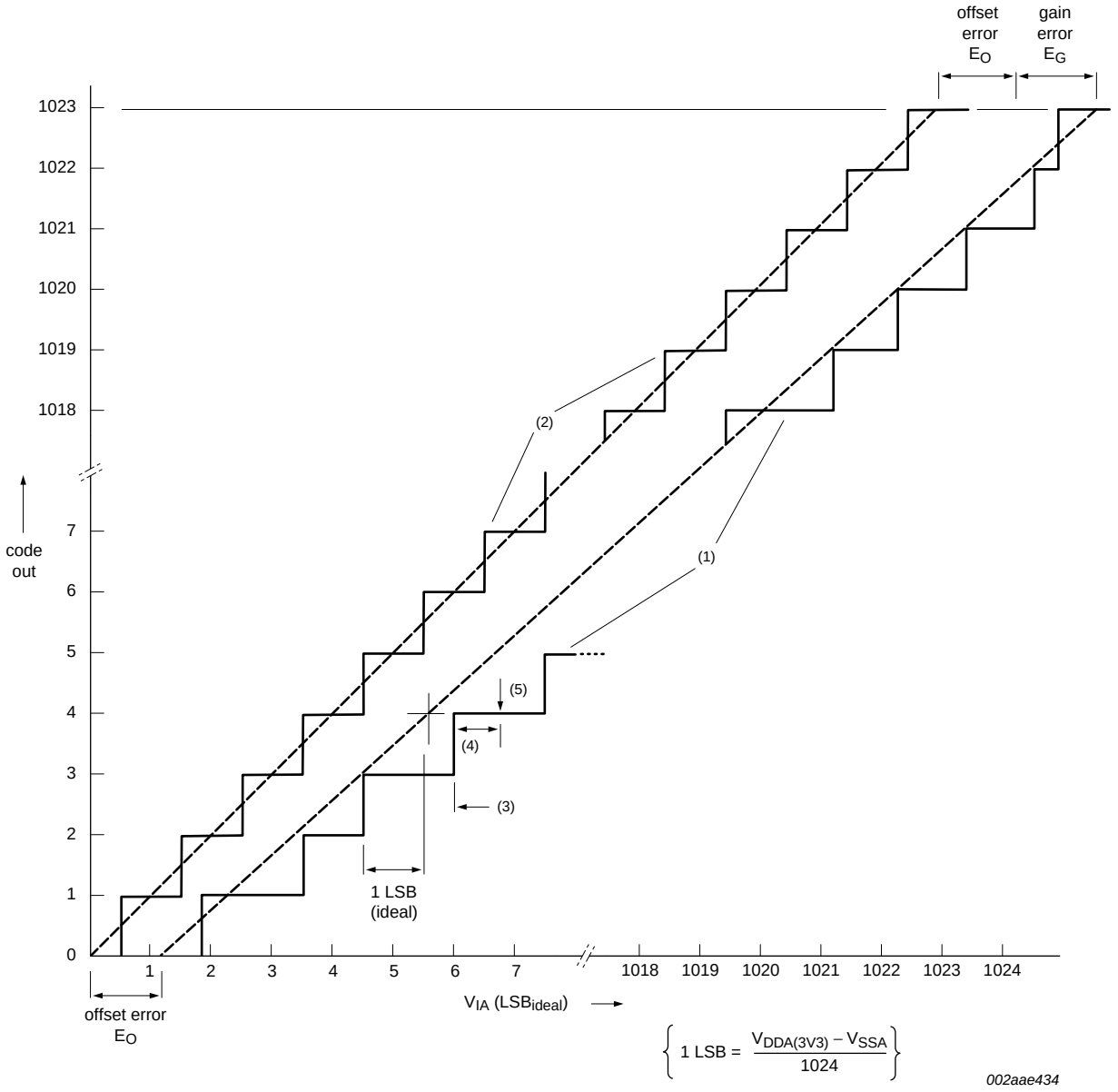
[3] The differential linearity error (E_D) is the difference between the actual step width and the ideal step width. See Figure 6.

[4] The integral non-linearity ($E_{L(adj)}$) is the peak difference between the center of the steps of the actual and the ideal transfer curve after appropriate adjustment of gain and offset errors. See Figure 6.

[5] The offset error (E_O) is the absolute difference between the straight line which fits the actual curve and the straight line which fits the ideal curve. See Figure 6.

[6] The gain error (E_G) is the relative difference in percent between the straight line fitting the actual transfer curve after removing offset error, and the straight line which fits the ideal transfer curve. See Figure 6.

[7] The absolute error (E_T) is the maximum difference between the center of the steps of the actual transfer curve of the non-calibrated ADC and the ideal transfer curve. See Figure 6.



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 6. ADC characteristics

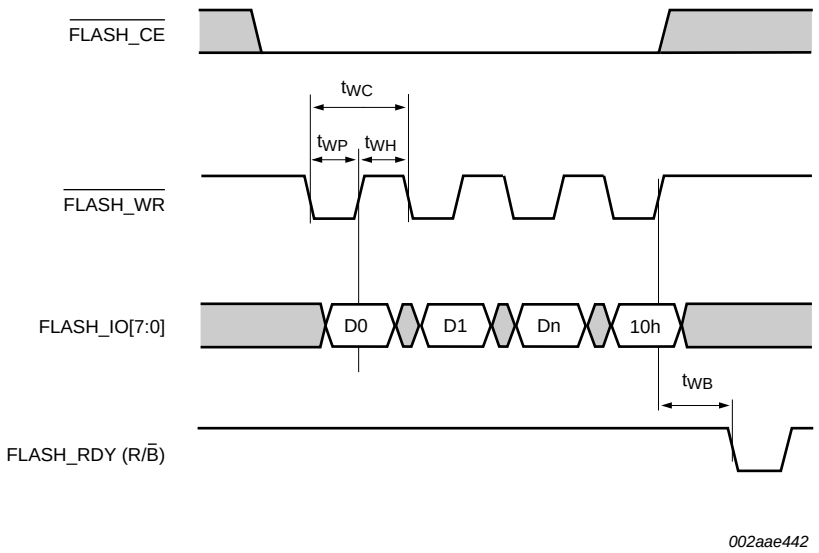


Fig 15. MLC NAND flash controller write timing (writing to NAND flash)

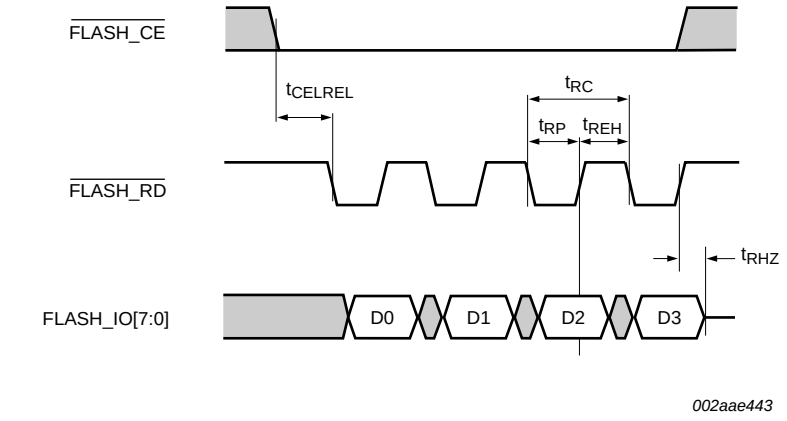


Fig 16. MLC NAND flash controller read timing (reading from NAND flash)

11.8 SLC NAND flash memory controller

Table 18. Dynamic characteristics of SLC NAND flash memory controller

T_{amb} = −40 °C to +85 °C.

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{ALS}	ALE set-up time	read	[1][2][4][6]	-	$T_{HCLK} \times (Rsu + Rw)$	-	ns
		write		-	$T_{HCLK} \times (Wsu + Ww)$	-	ns
t_{ALH}	ALE hold time	read	[1][7]	-	$T_{HCLK} \times Rh$	-	ns
		write		-	$T_{HCLK} \times Wh$	-	ns
t_{AR}	ALE to $\overline{RE}$ delay time	read	[1][2][6]	-	$T_{HCLK} \times Rsu$	-	ns
		write		-	$T_{HCLK} \times Wsu$	-	ns

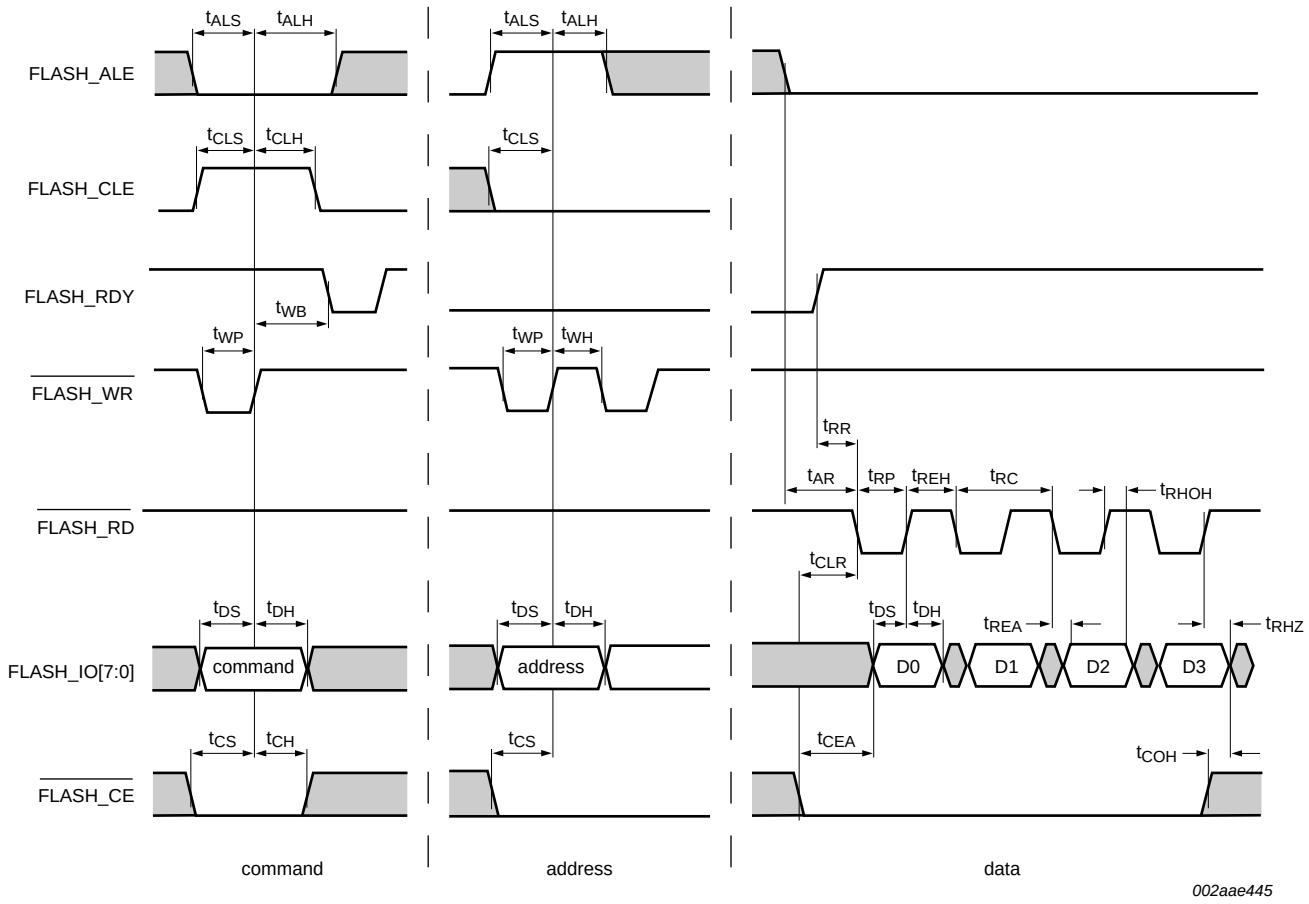


Fig 18. MLC NAND Flash memory read timing (reading from NAND flash)

14. Abbreviations

Table 20. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BSDL	Boundary Scan Description Language
CISC	Complex Instruction Set Computer
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
DMA	Direct Memory Access
DSP	Digital Signal Processing
ETM	Embedded Trace Macrocell
FAB	Fast Access Bus
FIFO	First In, First Out
FIQ	Fast Interrupt Request
GPIO	General Purpose Input/Output
I/O	Input/Output
IRQ	Interrupt Request
HS	High-Speed
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SDR SDRAM	Single Data Rate Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TFT	Thin Film Transistor
TTL	Transistor-Transistor Logic
STN	Super Twisted Nematic

19. Contents

continued >>