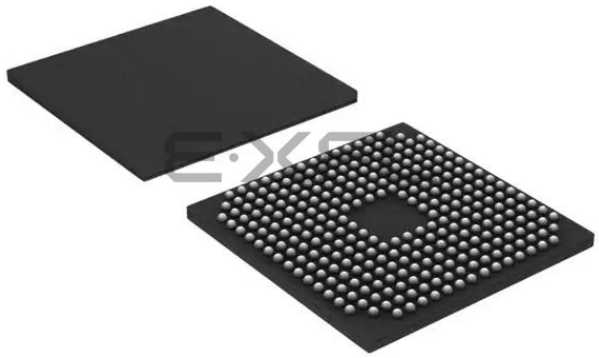

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ARM926EJ-S
Core Size	16/32-Bit
Speed	266MHz
Connectivity	EBI/EMI, Ethernet, I²C, IrDA, Microwire, SPI, SSI, SSP, UART/USART, USB OTG
Peripherals	DMA, I²S, LCD, Motor Control PWM, PWM, WDT
Number of I/O	51
Program Memory Size	-
Program Memory Type	ROMless
EEPROM Size	-
RAM Size	256K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	A/D 3x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	296-TFBGA
Supplier Device Package	296-TFBGA (15x15)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/lpc3250fet296-551

4. Ordering information

Table 1. Ordering information

Type number[1]	Package		
	Name	Description	Version
LPC3220FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3230FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3240FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1
LPC3250FET296/01[2]	TFBGA296	plastic thin fine-pitch ball grid array package; 296 balls	SOT1048-1

[1] F = −40 °C to +85 °C temperature range. Note that Revision “A” parts with and without the /01 suffix are identical. For example, LPC3220FET296 Revision “A” is identical to LPC3220FET296/01 Revision “A”.

[2] Available starting with Revision “A”.

4.1 Ordering options

Table 2. Part options

Type number	SRAM (kB)	10/100 Ethernet	LCD controller	Temperature range (°C)	Package
LPC3220FET296/01	128	0	0	−40 to +85	TFBGA296
LPC3230FET296/01	256	0	1	−40 to +85	TFBGA296
LPC3240FET296/01	256	1	0	−40 to +85	TFBGA296
LPC3250FET296/01	256	1	1	−40 to +85	TFBGA296

Table 4. Pin description *…continued*

Symbol	Pin	Power supply domain	Type	Description
GPO_22/ U7_HRTS/ LCDVD[14]	E10	VDD_IOD	O	General purpose output 22
			O	HS UART 7 RTS out
			O	LCD data bit 14 (LPC3230 and LPC3250 only)
GPO_23/ U2_HRTS/ U3_RTS	M16	VDD_IOA	O	General purpose output 23
			O	HS UART 2 RTS out
			O	UART 3 RTS out
HIGHCORE/ LCDVD[17]	H16	VDD_IOD	O	Core voltage control out
			O	LCD data bit 17 (LPC3230 and LPC3250 only)
I2C1_SCL	A5	VDD_IOB	I/O T	I^2C1 serial clock input/output
I2C1_SDA	B6	VDD_IOB	I/O T	I^2C1 serial data input/output
I2C2_SCL	A3	VDD_IOC	I/O T	I^2C2 serial clock input/output
I2C2_SDA	E4	VDD_IOC	I/O T	I^2C2 serial data input/output
I2S1TX_CLK/ MAT3[0]	A4	VDD_IOB	I/O	I^2S1 transmit clock
			O	Timer 3 match output 0
I2S1TX_SDA/ MAT3[1]	E7	VDD_IOB	I/O	I^2S1 transmit data
			O	Timer 3 match output 1
I2S1TX_WS/ CAP3[0]	B4	VDD_IOB	I/O	I^2S1 transmit word select
			I/O	Timer 3 capture input 0
JTAG_NTRST	H17	VDD_IOD	I: PU	JTAG1 reset input. Must be LOW during power-on reset. See Section 12.1 “Connecting the JTAG_NTRST pin”.
JTAG_RTCK	H18	VDD_IOD	O	JTAG1 return clock out
JTAG_TCK	H14	VDD_IOD	I	JTAG1 clock input
JTAG_TDI	J16	VDD_IOD	I: PU	JTAG1 data input
JTAG_TDO	J15	VDD_IOD	O	JTAG1 data out
JTAG_TMS	G18	VDD_IOD	I: PU	TAG1 test mode select input
KEY_COL0/ ENET_TX_CLK	F15	VDD_IOD	I	Keyscan column 0 input
			I	Ethernet transmit clock (LPC3240 and LPC3250 only)
KEY_COL1/ ENET_RX_CLK/ ENET_REF_CLK	E16	VDD_IOD	I	Keyscan column 1 input
			I	Ethernet receive clock (MII mode, LPC3240 and LPC3250 only)
			I	Ethernet reference clock (RMII mode, LPC3240 and LPC3250 only)
KEY_COL2/ ENET_RX_ER	D17	VDD_IOD	I	Keyscan column 2 input
			I	Ethernet receive error input (LPC3240 and LPC3250 only)
KEY_COL3/ ENET_CRS	D18	VDD_IOD	I	Keyscan column 3 input
			I	Ethernet carrier sense input (LPC3240 and LPC3250 only)

7.2.1 APB

Many peripheral functions are accessed by on-chip APBs that are attached to the higher speed AHB. The APB performs reads and writes to peripheral registers in three peripheral clocks.

7.2.2 FAB

Some peripherals are placed on a special bus called FAB that allows faster CPU access to those peripheral functions. A write access to FAB peripherals takes a single AHB clock and a read access to FAB peripherals takes two AHB clocks.

7.3 Physical memory map

The physical memory map incorporates several distinct regions, as shown in Figure 3. When an application is running, the CPU interrupt vectors are re-mapped to allow them to reside in on-chip SRAM (IRAM).

packet filtering and wake-up on LAN activity. Automatic frame transmission and reception with scatter-gather DMA off-loads many operations from the CPU. The Ethernet DMA can access off-chip memory via the EMC, as well as the IRAM. The Ethernet block interfaces between an off-chip Ethernet PHY using the Media Independent Interface (MII) or Reduced MII (RMII) protocol and the on-chip Media Independent Interface Management (MIIM) serial bus.

7.6.2.1 Features

- Ethernet standards support:
  - Supports 10 Mbit/s or 100 Mbit/s PHY devices including 10 Base-T, 100 Base-TX, 100 Base-FX, and 100 Base-T4.
  - Fully compliant with IEEE standard 802.3.
  - Fully compliant with 802.3x Full Duplex Flow Control and Half Duplex back pressure.
  - Flexible transmit and receive frame options.
  - Virtual Local Area Network (VLAN) frame support.
- Memory management:
  - Independent transmit and receive buffers memory mapped to SRAM.
  - DMA managers with scatter/gather DMA and arrays of frame descriptors.
  - Memory traffic optimized by buffering and pre-fetching.
- Enhanced Ethernet features:
  - Receive filtering.
  - Multicast and broadcast frame support for both transmit and receive.
  - Optional automatic Frame Check Sequence (FCS) insertion with Circular Redundancy Check (CRC) for transmit.
  - Selectable automatic transmit frame padding.
  - Over-length frame support for both transmit and receive allows any length frames.
  - Promiscuous receive mode.
  - Automatic collision back-off and frame retransmission.
  - Includes power management by clock switching. Wake-on-LAN power management support allows system wake-up using the receive filters or a magic frame detection filter.
- Physical interface
  - Attachment of external PHY chip through standard MII or RMII interface.
  - PHY register access is available via the MIIM interface.

7.6.3 USB interface

The LPC3220/30/40/50 supports USB in either device, host, or OTG configuration.

7.6.3.1 USB device controller

The USB device controller enables 12 Mbit/s data exchange with a USB host controller. It consists of register interface, serial interface engine, endpoint buffer memory and DMA controller. The serial interface engine decodes the USB data stream and writes data to the appropriate end point buffer memory. The status of a completed USB transfer or error

Two 32-bit match registers are readable and writable by the processor. A match will result in an interrupt provided that the interrupt is enabled. The ONSW output pin can also be triggered by a match event and cause an external power supply to turn on all of the operating voltages, as a way to startup after power has been removed.

The RTC block is implemented in a separate voltage domain. The block is supplied via a separate supply pin from a battery or other power source.

The RTC block also contains 32 words (128 bytes) of very low voltage SRAM. This SRAM is able to hold its contents down to the minimum RTC operating voltage.

7.9.4.1 Features

- Measures the passage of time in seconds.
- 32-bit up and down seconds counters.
- Ultra-low power design to support battery powered systems.
- Dedicated 32 kHz oscillator.
- An output pin is included to assist in waking up when the chip has had power removed to all functions except the RTC.
- Two 32-bit match registers with interrupt option.
- 32 words (128 bytes) of very low voltage SRAM.
- The RTC and battery RAM power have an independent power domain and dedicated supply pins, which can be powered from a battery or power supply.

Remark: The LPC3220/30/40/50 will run at voltages down to 0.9 V at frequencies below 14 MHz. However, the ARM core cannot access the RTC registers and battery RAM when the core supply voltage is at 0.9 V and the RTC supply is at 1.2 V.

7.9.5 Enhanced 32-bit timers/external event counters

The LPC3220/30/40/50 includes six 32-bit Timer/Counters. The Timer/Counter is designed to count cycles of the system derived clock or an externally-supplied clock. It can optionally generate interrupts or perform other actions at specified timer values, based on four match registers. The Timer/Counter also includes four capture inputs to trap the timer value when an input signal transitions, optionally generating an interrupt.

7.9.5.1 Features

- A 32-bit Timer/Counter with a programmable 32-bit pre-scaler.
- Counter or Timer operation.
- Up to four 32-bit capture channels per timer, that can take a snapshot of the timer value when an input signal transitions. A capture event may also optionally generate an interrupt.
- Four 32-bit match registers that allow:
  - continuous operation with optional interrupt generation on match
  - stop timer on match with optional interrupt generation
  - reset timer on match with optional interrupt generation
- Up to four external outputs corresponding to match registers, with the following capabilities:

10. Static characteristics

Table 8. Static characteristics

T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$V_{DD(1V2)}$	supply voltage (1.2 V)	core supply voltage for full performance; 266 MHz (see Figure 4); VDD_CORE supply domain	[2]	1.31	1.35	1.39	V
		core supply voltage for normal performance; 208 MHz (see Figure 4); VDD_CORE supply domain	[2]	1.1	1.2	1.39	V
		core supply voltage for reduced power; up to 14 MHz CPU; VDD_CORE supply domain	[2]	0.9	-	1.39	V
		RTC supply voltage; VDD_RTC supply domain	[3]	0.9	-	1.39	V
		PLL and oscillator supply voltage	[4]	1.1	1.2	1.39	V
$V_{DD(EMC)}$	external memory controller supply voltage	in 1.8 V range	[5]	1.7	1.8	1.95	V
		in 2.5 V range	[6]	2.3	2.5	2.7	V
		in 3.3 V range	[7]	2.7	3.3	3.6	V
$V_{DD(IO)}$	input/output supply voltage	VDD_IOA, VDD_IOB, and VDD_IOD supply domain in 1.8 V range		1.7	1.8	1.95	V
		in 3.3 V range		2.7	3.3	3.6	V
		VDD_IOC supply domain in 1.8 V range		1.7	1.8	1.95	V
		in 3.3 V range		2.3	3.3	3.6	V
$V_{DDA(3V3)}$	analog supply voltage (3.3 V)	applies to pins in VDD_AD power domain		2.7	3.3	3.6	V

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(RTC)}$	RTC supply current	normal operation; VDD_RTC = VDD_RTCCORE = VDD_RTCOSC = 1.2 V; T_{amb} = 25 °C	[8]	-	13	-	μA
		RTC back up operation; Rev "-" silicon	[9]	-	30	-	μA
		Rev "A" silicon	[9]	-	4	-	
I_{DD}	supply current	for HCLK; PLL output frequency = 266 MHz; VDD_PLLHCLK = 1.2 V		-	2	-	mA
		for USB; VDD_PLLUSB = 1.2 V		-	2	-	mA
		for ADC; interrupt driven loop converting ADIN[2:0]; VDD_AD = 3.3 V		-	< 1	-	mA
Input pins and I/O pins configured as input							
V_I	input voltage		[10][12]	0	-	$V_{DD(IO)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		0.7 × $V_{DD(IO)}$	-	-	V
		3.3 V inputs		0.7 × $V_{DD(IO)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	0.3 × $V_{DD(IO)}$	V
		3.3 V inputs		-	-	0.3 × $V_{DD(IO)}$	V
V_{hys}	hysteresis voltage	1.8 V inputs		0.1 × $V_{DD(IO)}$	-	-	V
		3.3 V inputs		0.1 × $V_{DD(IO)}$	-	-	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	μA
I_{IH}	HIGH-level input current	V_I = $V_{DD(IO)}$; no pull-down	[10]	-	-	1	μA
I_{latch}	I/O latch-up current	−(1.5$V_{DD(IO)}$) < V_I < (1.5$V_{DD(IO)}$)	[10]	-	-	100	mA
I_{pu}	pull-up current	1.8 V inputs with pull-up; V_I = 0 V		6	12	22	μA
		3.3 V inputs with pull-up; V_I = 0 V		25	50	80	μA
I_{pd}	pull-down current	1.8 V inputs with pull-down; V_I = $V_{DD(IO)}$		5	12	22	μA
		3.3 V inputs with pull-down; V_I = $V_{DD(IO)}$		25	50	85	μA
I_I	input current	bus keeper inputs; V_I = V_{DD}		-	-	1	μA
		V_I = 0.67 × V_{DD}		-	-	55	μA
		V_I = 0.33 × V_{DD}		-	-	60	μA
		V_I = 0 V		-	-	1	μA
C_i	input capacitance	Excluding bonding pad capacitance		-	-	3.3	pF

Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
Output pins and I/O pins configured as output							
V_O	output voltage		[10][11] [12][13]	0	-	$V_{DD(IO)}$	V
V_{OH}	HIGH-level output voltage	1.8 V outputs; I_{OH} = −1 mA	[14]	$V_{DD(IO)} - 0.4$	-	-	V
		3.3 V outputs; I_{OH} = −4 mA	[14]	$V_{DD(IO)} - 0.4$	-	-	V
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
		3.3 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
I_{OH}	HIGH-level output current	$V_{DD(IO)}$ = 1.8 V; $V_{OH} = V_{DD(IO)} - 0.4$ V	[10][14]	−3.3	-	-	mA
		$V_{DD(IO)}$ = 3.3 V; $V_{OH} = V_{DD(IO)} - 0.4$ V		−6.5	-	-	mA
I_{OL}	LOW-level output current	$V_{DD(IO)}$ = 1.8 V; V_{OL} = 0.4 V	[10][14]	1.5	-	-	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OL} = 0.4 V		3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; $V_O = V_{DD(IO)}$; no pull-up/down	[10]	-	-	1	μA
I_{OHS}	HIGH-level short-circuit output current	$V_{DD(IO)}$ = 1.8 V; V_{OH} = 0 V	[15]	-	-	66	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OH} = 0 V		-	-	183	mA
I_{OLS}	LOW-level short-circuit output current	$V_{DD(IO)}$ = 1.8 V; $V_{OL} = V_{DD(IO)}$	[10][15]	-	-	34	mA
		$V_{DD(IO)}$ = 3.3 V; $V_{OL} = V_{DD(IO)}$		-	-	105	mA
Z_o	output impedance	$V_{DD(IO)}$ = 1.8 V		40	-	60	Ω
		$V_{DD(IO)}$ = 3.3 V		40	-	60	Ω
EMC pins							
V_I	input voltage		[12]	0	-	$V_{DD(EMC)}$	V
V_{IH}	HIGH-level input voltage	1.8 V inputs		$0.7 \times V_{DD(EMC)}$	-	-	V
		3.3 V inputs		$0.7 \times V_{DD(EMC)}$	-	-	V
V_{IL}	LOW-level input voltage	1.8 V inputs		-	-	$0.3 \times V_{DD(EMC)}$	V
		3.3 V inputs		-	-	$0.3 \times V_{DD(EMC)}$	V
V_{hys}	hysteresis voltage	1.8 V inputs		0.4	-	0.6	V
		3.3 V inputs		0.55	-	0.85	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	0.3	μA
I_{IH}	HIGH-level input current	$V_I = V_{DD(EMC)}$; no pull-down		-	-	0.3	μA
I_{latch}	I/O latch-up current	$-(1.5V_{DD(EMC)}) < V_I < (1.5V_{DD(EMC)})$		-	-	100	mA
I_{pu}	pull-up current	1.8 V inputs with pull-up; V_I = 0		34	62	107	μA
		3.3 V inputs with pull-up; V_I = 0		97	169	271	μA

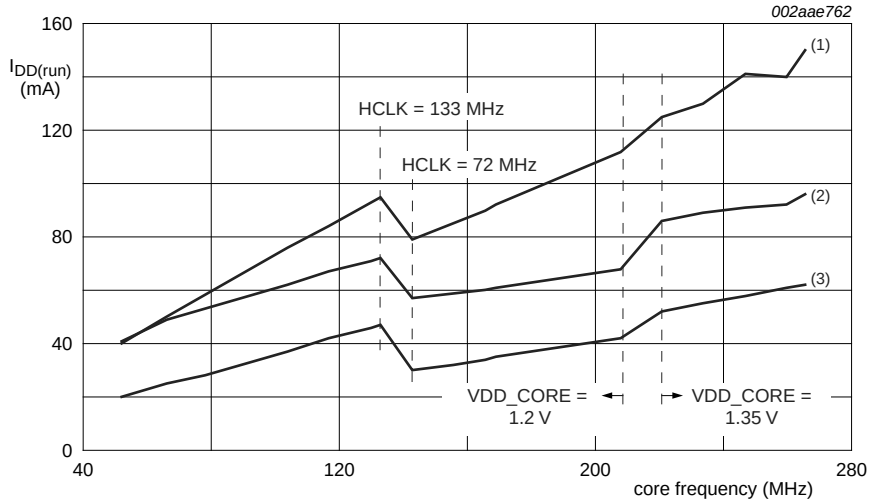
Table 8. Static characteristics *…continued*
T_{amb} = −40 °C to +85 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
C_i	input capacitance	Excluding bonding pad capacitance		-	-	1.6	pF
V_{OL}	LOW-level output voltage	1.8 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
		3.3 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
I_{OL}	LOW-level output current	$V_{DD(IO)}$ = 1.8 V; V_{OL} = 0.4 V	[10][14]	3	-	-	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OL} = 0.4 V		3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = $V_{DD(IO)}$; no pull-up/down	[10]	-	-	10	μA
I_{OLS}	LOW-level short-circuit output current	$V_{DD(IO)}$ = 1.8 V; V_{OL} = $V_{DD(IO)}$	[10][15]	-	-	40	mA
		$V_{DD(IO)}$ = 3.3 V; V_{OL} = $V_{DD(IO)}$		-	-	40	mA
ONSW pin							
V_O	output voltage		[10][11][12][13]	0	-	$V_{DD(1V2)}$	V
V_{OH}	HIGH-level output voltage	1.2 V outputs; I_{OH} = −1 mA	[14]	$V_{DD(1V2)}$ − 0.4	-	-	V
V_{OL}	LOW-level output voltage	1.2 V outputs; I_{OL} = 4 mA	[14]	-	-	0.4	V
I_{OH}	HIGH-level output current	V_{OH} = $V_{DD(1V2)}$ − 0.4 V	[10][14]	−4	-	-	mA
I_{OL}	LOW-level output current	V_{OL} = 0.4 V	[10][14]	3	-	-	mA
I_{OZ}	OFF-state output current	V_O = 0 V; V_O = $V_{DD(1V2)}$; no pull-up/down	[10]	-	-	1.5	μA
I_{OHS}	HIGH-level short-circuit output current	$V_{DD(1V2)}$ = 1.8 V; V_{OH} = 0 V	[15]	-	-	−135	mA
I_{OLS}	LOW-level short-circuit output current	V_{OL} = $V_{DD(1V2)}$	[10][15]	-	-	135	mA
Z_o	output impedance	$V_{DD(1V2)}$ = 1.2 V		40	-	60	Ω
Oscillator input/output pins							
$V_{i(xtal)}$	crystal input voltage	on pins RTCX_IN and SYSX_IN		−0.5	-	+1.3	V
$V_{o(xtal)}$	crystal output voltage	on pins RTCX_OUT and SYSX_OUT		−0.5	-	+1.3	V
$\overline{\text{RESET}}$ pin							
V_I	input voltage		[10][12]	0	-	1.95	V
V_{IH}	HIGH-level input voltage	1.2 V inputs		0.7 × $V_{DD(1V2)}$	-	-	V
V_{IL}	LOW-level input voltage	1.2 V inputs		-	-	0.3 × $V_{DD(1V2)}$	V
I_{IL}	LOW-level input current	V_I = 0 V; no pull-up		-	-	1	μA

10.4 Power consumption in Run mode

Power consumption is shown in Figure 5 for WinCE applications running under typical conditions from SDRAM. MMU and I-cache/D-cache are enabled. The VFP is turned on but not used. I^2S-interface (channel 1), LCD, SLC NAND controller, I^2C1-bus, SD card, touchscreen ADC, and UART 3 are turned on. All other peripherals are turned off.

The AHB clock HCLK is identical to the core clock for frequencies up to 133 MHz, which is the maximum allowed HCLK frequency. For higher core frequencies, the HCLK PLL output must be divided by 2 to obtain an HCLK frequency lower than or equal to 133 MHz resulting in correspondingly lower power consumption by the AHB peripherals.



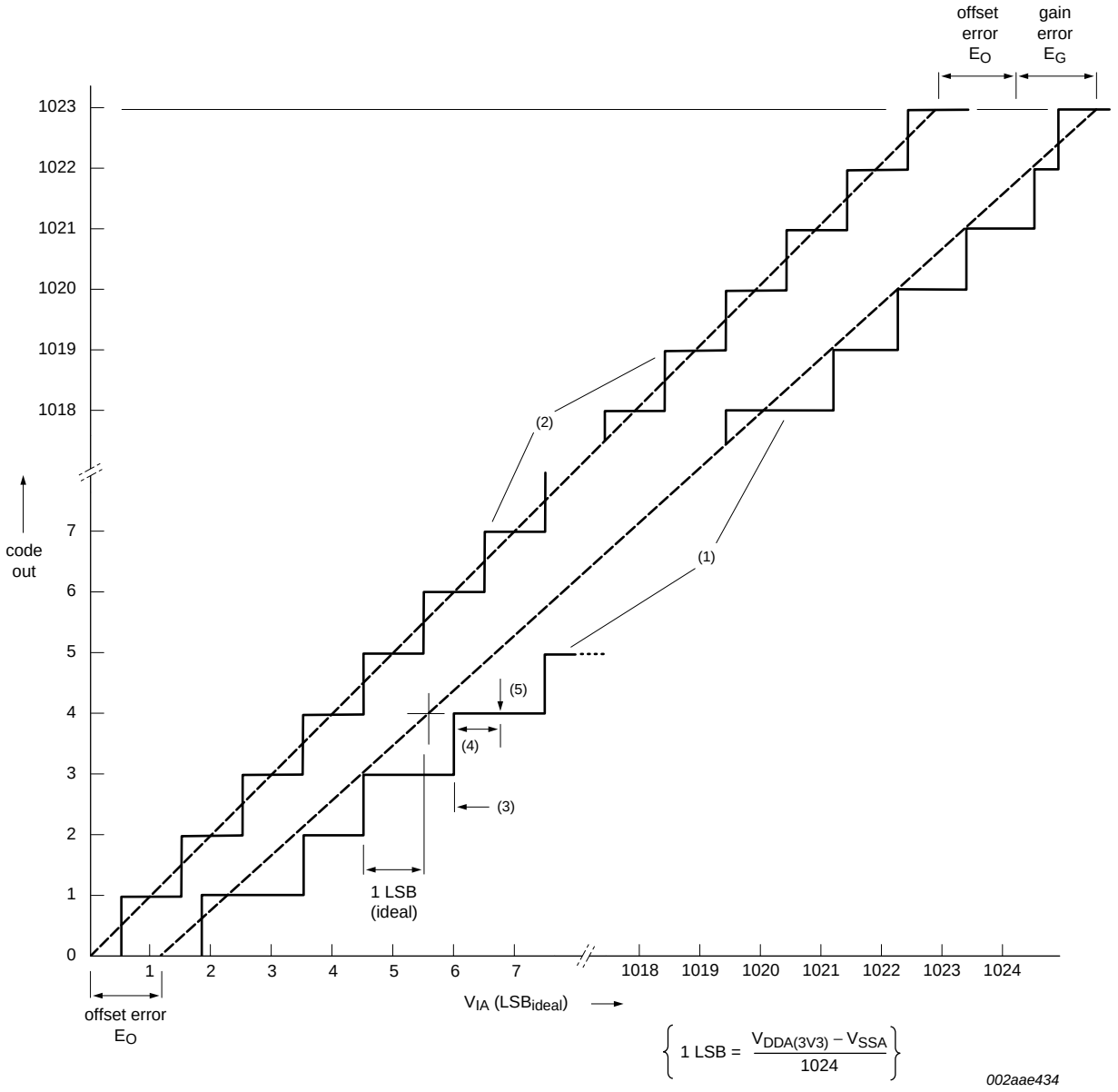
Conditions: T_{amb} = 25 °C; VDD_CORE = 1.2 V for core frequencies ≤ 208 MHz; VDD_CORE = 1.35 V for core frequencies > 208 MHz; $V_{DD(IO)}$ = 1.8 V.

(1) WinCE running from SDRAM; playing wmv file at 20 frames/s, 32 kHz mono.

(2) WinCE running from SDRAM; playing mp3 file at 128 kbit/s, stereo.

(3) WinCE running from SDRAM; no application running.

Fig 5. Core current versus core frequency for WinCE applications



(1) Example of an actual transfer curve.

(2) The ideal transfer curve.

(3) Differential linearity error (E_D).

(4) Integral non-linearity ($E_{L(adj)}$).

(5) Center of a step of the actual transfer curve.

Fig 6. ADC characteristics

Table 12. Dynamic characteristics: static external memory interface *…continued*
C_L = 25 pF, T_{amb} = 20 °C, $V_{DD(EMC)}$ = 1.8 V, 2.5 V, or 3.3 V.

Symbol	Parameter	Notes	Min	Typ	Max	Unit
t_{WELWEH}	$\overline{WE}$ LOW to $\overline{WE}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
$t_{BLSLBLSH}$	$\overline{BLS}$ LOW to $\overline{BLS}$ HIGH time	[4][5]	-	(WAITWR – WAITWEN + 1) × T_{CLCL}	-	ns
t_{WEHANV}	$\overline{WE}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
t_{WEHDNV}	$\overline{WE}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHANV}$	$\overline{BLS}$ HIGH to address invalid time		-	1 × T_{CLCL}	-	ns
$t_{BLSHDNV}$	$\overline{BLS}$ HIGH to data invalid time		-	1 × T_{CLCL}	-	ns

[1] T_{CLCL} = 1/HCLK

[2] Refer to the *LPC32x0 User manual* EMCStaticWaitOen0-3 register for the programming of WAITOEN value.

[3] Refer to the *LPC32x0 User manual* EMCStaticWaitRd0-3 register for the programming of WAITRD value.

[4] Refer to the *LPC32x0 User manual* EMCStaticWaitWen0-3 register for the programming of WAITWEN value.

[5] Refer to the *LPC32x0 User manual* EMCStaticWaitWr0-3 register for the programming of WAITWR value.

[6] Earliest of $\overline{CS}$ HIGH, $\overline{OE}$ HIGH, address change to data invalid.

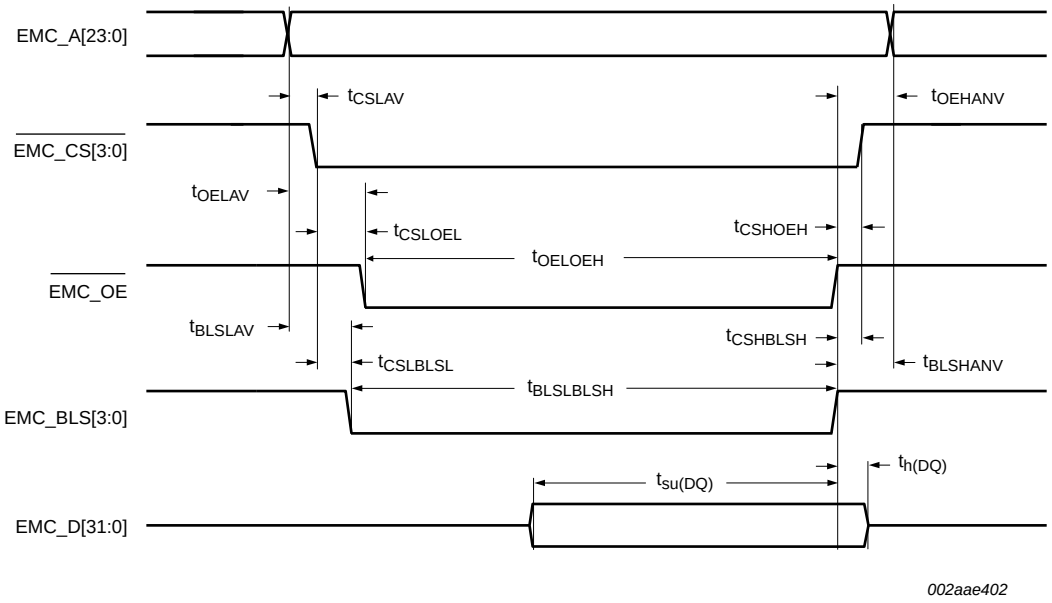


Fig 7. External memory read access

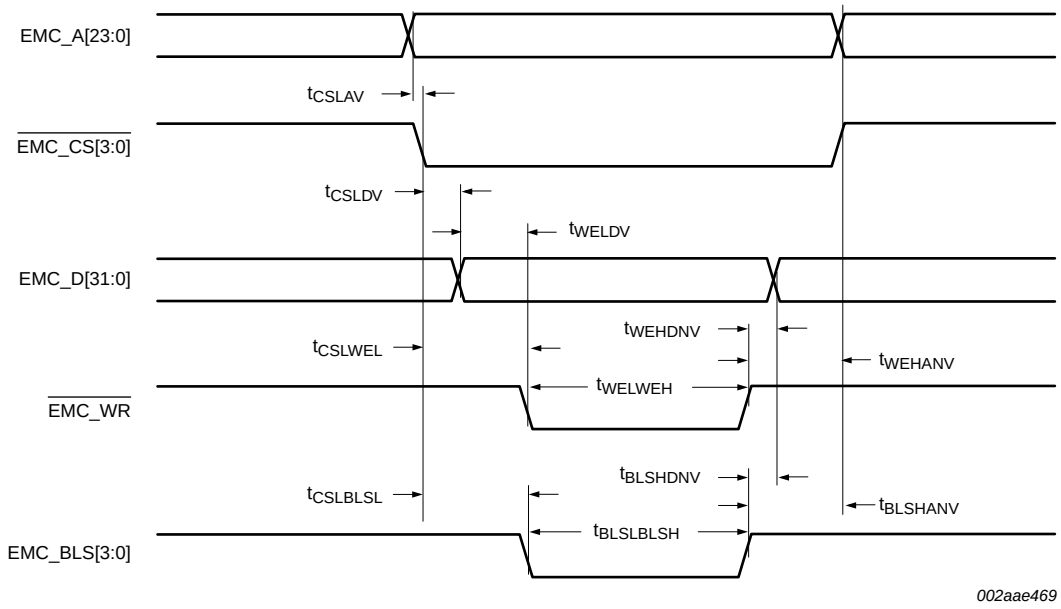


Fig 8. External memory write access

11.3 SDR SDRAM Controller

Table 13. EMC SDR SDRAM memory interface dynamic characteristics
C_L = 25 pF, T_{amb} = −40 °C to +85 °C, unless otherwise specified.[1][3]

Symbol	Parameter		Min	Typical[2]	Max	Unit
f_{oper}	operating frequency	[4]		104	133	MHz
t_{CK}	clock cycle time		7.5	9.6	-	ns
t_{CL}	CK LOW-level width		-	4.8	-	ns
t_{CH}	CK HIGH-level width		-	4.8	-	ns
$t_{d(V)ctrl}$	control valid delay time	[5][6]	-	(CMD_DLY × 0.25) + 2.7		ns
$t_{h(ctrl)}$	control hold time	[5][6]		(CMD_DLY × 0.25) + 1.2	-	ns
$t_{d(AV)}$	address valid delay time	[6]	-	(CMD_DLY × 0.25) + 3.2		ns
$t_{h(A)}$	address hold time	[6]		(CMD_DLY × 0.25) + 1.2	-	ns
$t_{d(QV)}$	data output valid delay time	[6]	-	(CMD_DLY × 0.25) + 3.5		ns
$t_{h(Q)}$	data output hold time	[6]		(CMD_DLY × 0.25) + 1.2	-	ns
$t_{su(D)}$	data input set-up time		-	0.6	-	ns
$t_{h(D)}$	data input hold time		-	0.9	-	ns
t_{QZ}	data output high-impedance time		-	-	$< t_{CK}$	ns

[1] Parameters are valid over operating temperature range unless otherwise specified.

[2] Typical values valid for EMC pads set to fast slew rate: VDD_EMC = 1.8 V, VDD_CORE = 1.2 V or slower slew rate: VDD_EMC = 3.3 V, VDD_CORE = 1.2 V (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

[3] All min or max values valid for EMC pads set to fast slew rate: VDD_EMC = 1.8 V, VDD_CORE = 1.2 V or slower slew rate: VDD_EMC = 3.3 V, VDD_CORE = 1.2 V.

[4] $f_{oper} = 1/t_{CK}$.

[5] Applies to signals: EMC_DQM[3:0], $\overline{\text{EMC\_DYCS[1:0]}}$, $\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_WR}}$, EMC_CKE[1:0].

[6] CMD_DLY = COMMAND_DELAY bit field in SDRAMCLK_CTRL[18:14] register, see *External Memory Controller (EMC) chapter in LPC32x0 User manual*.

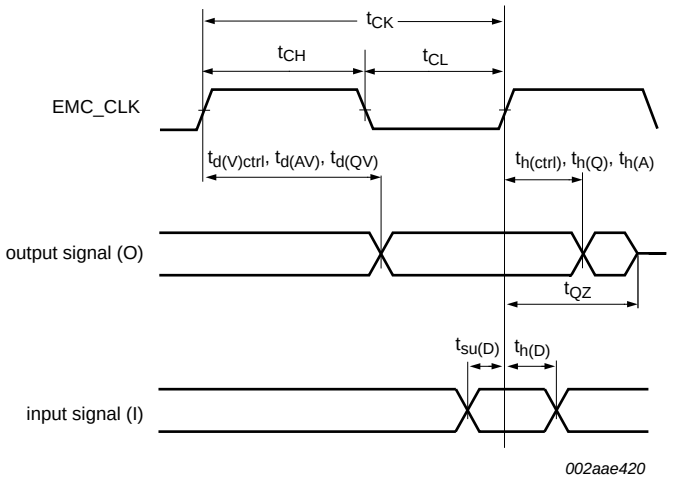


Fig 9. SDR SDRAM signal timing

11.4 DDR SDRAM controller

Table 14. EMC DDR SDRAM memory interface dynamic characteristics[1]

C_L = 25 pF, T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typical	Max	Unit
f_{oper}	operating frequency			-	104	133	MHz
t_{CK}	clock cycle time			7.5	9.6	-	ns
t_{CL}	CK LOW-level width			-	$0.5 \times t_{CK}$	-	ns
t_{CH}	CK HIGH-level width			-	$0.5 \times t_{CK}$	-	ns
$t_{d(V)ctrl}$	control valid delay time		[2][3]	-	(CMD_DLY × 0.25) + 1.5	-	ns
$t_{h(ctrl)}$	control hold time		[2][3]	-	(CMD_DLY × 0.25) − 1.5	-	ns
$t_{d(AV)}$	address valid delay time		[2]	-	(CMD_DLY × 0.25) + 1.5	-	ns
$t_{h(A)}$	address hold time		[2]	-	(CMD_DLY × 0.25) − 1.5	-	ns
$t_{su(Q)}$	data output set-up time	EMC_D[31:0] and EMC_DQM[3:0] to EMC_DQS[1:0] out	[5]	$0.08 \times t_{CK}$	$0.15 \times t_{CK}$	$0.25 \times t_{CK}$	ns
$t_{h(Q)}$	data output hold time	EMC_D[31:0] and EMC_DQM[3:0] to EMC_DQS[1:0] out	[5]	$0.25 \times t_{CK}$	$0.35 \times t_{CK}$	$0.42 \times t_{CK}$	ns
t_{DQSH}	DQS HIGH time	for WRITE command		-	$0.5 \times t_{CK}$	-	ns
t_{DQSL}	DQS LOW time	for WRITE command		-	$0.5 \times t_{CK}$	-	ns
t_{DQSS}	WRITE command to first DQS latching transition time	for DQS out		-	t_{CK} + 0.7	-	ns
t_{DSS}	DQS falling edge to CK set-up time	for DQS in		-	$0.5 \times t_{CK}$	-	ns
t_{DSH}	DQS falling edge hold time from CK	for DQS in		-	$0.5 \times t_{CK}$	-	ns
$t_{d(DQS)}$	DQS delay time	for DQS in	[4]	-	DQS_DELAY	-	ns
$t_{su(D)}$	data input set-up time			-	0.3	-	ns
$t_{h(D)}$	data input hold time			-	0.5	-	ns

[1] All values valid for EMC pads set to fast slew rate at 1.8 V unless otherwise specified (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

[2] CMD_DLY = COMMAND_DELAY bit field in SDRAMCLK_CTRL[18:14] register, see *External Memory Controller (EMC) chapter in LPC32x0 User manual*.

[3] Applies to signals EMC_DQM[3:0], $\overline{\text{EMC\_DYCS}}$[1:0], $\overline{\text{EMC\_RAS}}$, $\overline{\text{EMC\_CAS}}$, $\overline{\text{EMC\_WR}}$, EMC_CKE[1:0].

[4] DQS_DELAY, see *LPC32x0 User manual, External Memory Controller Chapter, Section 8 DDR DQS delay calibration* for details on configuring this value.

[5] Test conditions for measurements: T_{amb} = −40 °C to +85 °C; operating frequency range f_{oper} = 52 MHz to 133 MHz; EMC_DQM[3:0] and EMC_D[31:0] driving 2 inches of 50 Ω characteristic impedance trace with 10 pF capacitive load; no external source series termination resistors used. EMC pads set to fast slew rate at 1.8 V or 2.5 V (see SDRAMCLK_CTRL register in the *LPC32x0 User manual*).

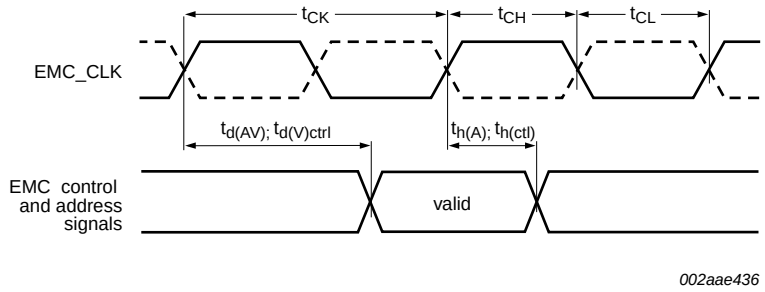


Fig 10. DDR control timing parameters

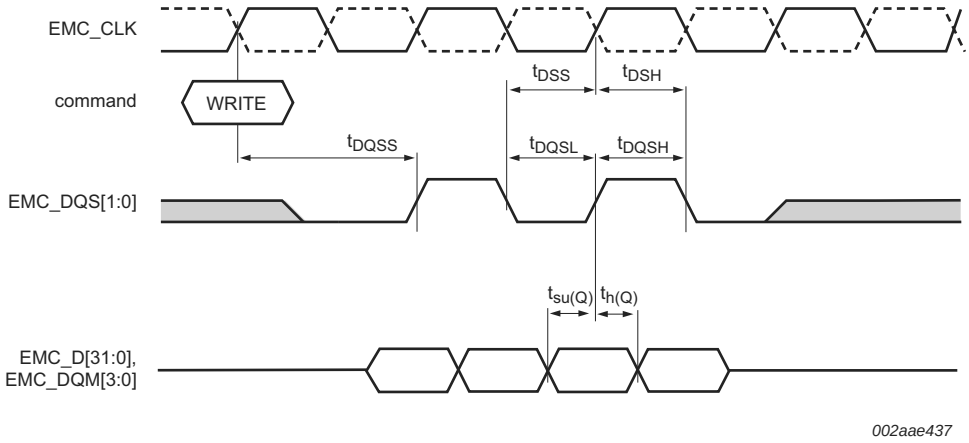
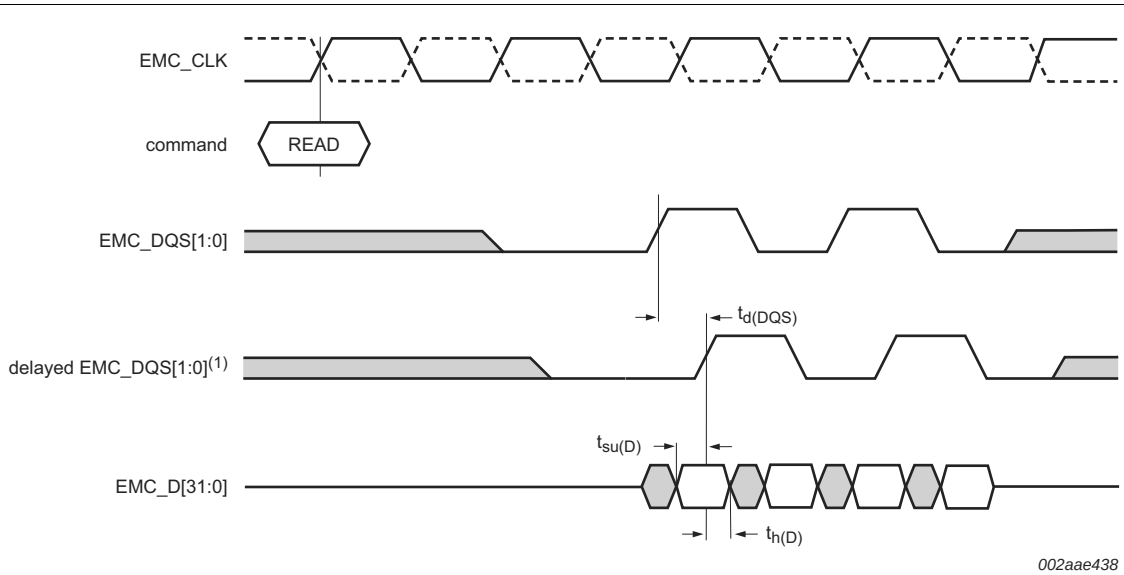


Fig 11. DDR write timing parameters



(1) The delay of the EMC_DQS[1:0] signal is determined by the DQS_DELAY settings. See *LPC32x0 User manual, External Memory Controller Chapter, section DDR DQS delay calibration* for details on configuring this value.

Fig 12. DDR read timing parameters

14. Abbreviations

Table 20. Abbreviations

Acronym	Description
ADC	Analog-to-Digital Converter
AHB	Advanced High-performance Bus
AMBA	Advanced Microcontroller Bus Architecture
APB	Advanced Peripheral Bus
BSDL	Boundary Scan Description Language
CISC	Complex Instruction Set Computer
DDR SDRAM	Double Data Rate Synchronous Dynamic Random Access Memory
DMA	Direct Memory Access
DSP	Digital Signal Processing
ETM	Embedded Trace Macrocell
FAB	Fast Access Bus
FIFO	First In, First Out
FIQ	Fast Interrupt Request
GPIO	General Purpose Input/Output
I/O	Input/Output
IRQ	Interrupt Request
HS	High-Speed
IrDA	Infrared Data Association
JTAG	Joint Test Action Group
LCD	Liquid Crystal Display
MAC	Media Access Control
MIIM	Media Independent Interface Management
OHCI	Open Host Controller Interface
OTG	On-The-Go
PHY	Physical Layer
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RMII	Reduced Media Independent Interface
SE0	Single Ended Zero
SDR SDRAM	Single Data Rate Synchronous Dynamic Random Access Memory
SPI	Serial Peripheral Interface
SSI	Serial Synchronous Interface
SSP	Synchronous Serial Port
TFT	Thin Film Transistor
TTL	Transistor-Transistor Logic
STN	Super Twisted Nematic

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Date of release: 24 June 2014
Document identifier: LPC3220_30_40_50