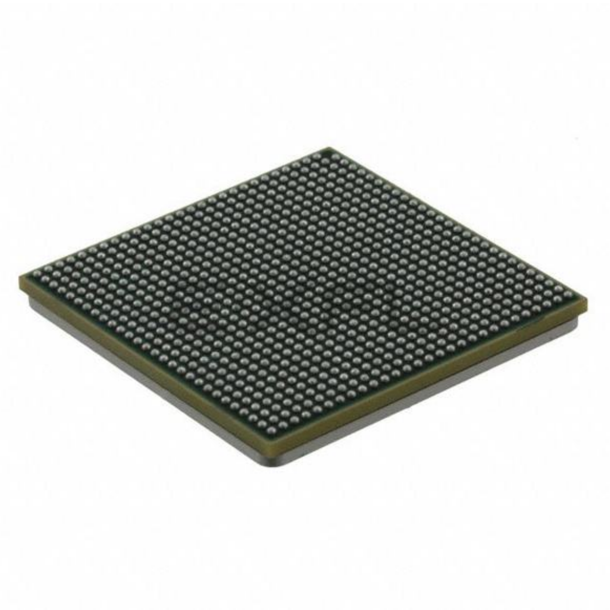

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Quad Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8254svt1000b

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
B9	M2A13	O	GVDD2
B10	VSS	Ground	N/A
B11	GVDD2	Power	N/A
B12	$\overline{\text{M2CS1}}$	O	GVDD2
B13	VSS	Ground	N/A
B14	GVDD2	Power	N/A
B15	M2DQ35	I/O	GVDD2
B16	VSS	Ground	N/A
B17	GVDD2	Power	N/A
B18	M2DQ51	I/O	GVDD2
B19	VSS	Ground	N/A
B20	GVDD2	Power	N/A
B21	Reserved	NC	—
B22	Reserved	NC	—
B23	SR1_TXD0	O	SXPVDD1
B24	$\overline{\text{SR1\_TXD0}}$	O	SXPVDD1
B25	SXCVDD1	Power	N/A
B26	SXCVSS1	Ground	N/A
B27	$\overline{\text{SR1\_RXD0}}$	I	SXCVDD1
B28	SR1_RXD0	I	SXCVDD1
C1	M2DQ28	I/O	GVDD2
C2	M2DM3	O	GVDD2
C3	M2DQ26	I/O	GVDD2
C4	M2ECC4	I/O	GVDD2
C5	M2DM8	O	GVDD2
C6	M2ECC2	I/O	GVDD2
C7	M2CKE1	O	GVDD2
C8	M2CK0	O	GVDD2
C9	$\overline{\text{M2CK0}}$	O	GVDD2
C10	M2BA1	O	GVDD2
C11	M2A1	O	GVDD2
C12	$\overline{\text{M2WE}}$	O	GVDD2
C13	M2DQ37	I/O	GVDD2
C14	M2DM4	O	GVDD2
C15	M2DQ36	I/O	GVDD2
C16	M2DQ32	I/O	GVDD2
C17	M2DQ55	I/O	GVDD2
C18	M2DM6	O	GVDD2
C19	M2DQ53	I/O	GVDD2
C20	M2DQ52	I/O	GVDD2
C21	Reserved	NC	—
C22	SR1_IMP_CAL_RX	I	SXCVDD1
C23	SXPVSS1	Ground	N/A
C24	SXPVDD1	Power	N/A
C25	SR1_REF_CLK	I	SXCVDD1
C26	$\overline{\text{SR1\_REF\_CLK}}$	I	SXCVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
C27	Reserved	NC	—
C28	Reserved	NC	—
D1	GVDD2	Power	N/A
D2	VSS	Ground	N/A
D3	M2DQ29	I/O	GVDD2
D4	GVDD2	Power	N/A
D5	VSS	Ground	N/A
D6	M2ECC5	I/O	GVDD2
D7	GVDD2	Power	N/A
D8	VSS	Ground	N/A
D9	M2A8	O	GVDD2
D10	GVDD2	Power	N/A
D11	VSS	Ground	N/A
D12	M2A0	O	GVDD2
D13	GVDD2	Power	N/A
D14	VSS	Ground	N/A
D15	M2DQ39	I/O	GVDD2
D16	GVDD2	Power	N/A
D17	VSS	Ground	N/A
D18	M2DQ54	I/O	GVDD2
D19	GVDD2	Power	N/A
D20	VSS	Ground	N/A
D21	SXPVSS1	Ground	N/A
D22	SXPVDD1	Power	N/A
D23	SR1_TXD1	O	SXPVDD1
D24	$\overline{\text{SR1\_TXD1}}$	O	SXPVDD1
D25	SXCVSS1	Ground	N/A
D26	SXCVDD1	Power	N/A
D27	$\overline{\text{SR1\_RXD1}}$	I	SXCVDD1
D28	SR1_RXD1	I	SXCVDD1
E1	M2DQ31	I/O	GVDD2
E2	M2DQ30	I/O	GVDD2
E3	M2DQ27	I/O	GVDD2
E4	M2ECC7	I/O	GVDD2
E5	M2ECC6	I/O	GVDD2
E6	M2ECC3	I/O	GVDD2
E7	M2A9	O	GVDD2
E8	M2A6	O	GVDD2
E9	M2A3	O	GVDD2
E10	M2A10	O	GVDD2
E11	$\overline{\text{M2RAS}}$	O	GVDD2
E12	M2A2	O	GVDD2
E13	M2DQ38	I/O	GVDD2
E14	$\overline{\text{M2DQS5}}$	I/O	GVDD2
E15	M2DQS5	I/O	GVDD2
E16	M2DQ33	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
H25	SXCVSS1	Ground	N/A
H26	SXCVDD1	Power	N/A
H27	$\overline{\text{SR1\_RXD3}}$/$\overline{\text{SG2\_RX}}$[4]	I	SXCVDD1
H28	SR1_RXD3/SG2_RX[4]	I	SXCVDD1
J1	M2DQS1	I/O	GVDD2
J2	$\overline{\text{M2DQS1}}$	I/O	GVDD2
J3	M2DQ10	I/O	GVDD2
J4	M2DQ11	I/O	GVDD2
J5	M2DQ14	I/O	GVDD2
J6	M2DQ23	I/O	GVDD2
J7	M2ODT0	O	GVDD2
J8	M2A12	O	GVDD2
J9	M2A14	O	GVDD2
J10	VSS	Ground	N/A
J11	GVDD2	Power	N/A
J12	VSS	Ground	N/A
J13	GVDD2	Power	N/A
J14	VSS	Ground	N/A
J15	GVDD2	Power	N/A
J16	VSS	Ground	N/A
J17	GVDD2	Power	N/A
J18	VSS	Ground	N/A
J19	GVDD2	Power	N/A
J20	Reserved	NC	—
J21	Reserved	NC	—
J22	Reserved	NC	—
J23	SXPVDD1	Power	N/A
J24	SXPVSS1	Ground	N/A
J25	SXCVDD1	Power	N/A
J26	SXCVSS1	Ground	N/A
J27	SXCVDD1	Power	N/A
J28	SXCVSS1	Ground	N/A
K1	VSS	Ground	N/A
K2	GVDD2	Power	N/A
K3	M2DM1	O	GVDD2
K4	VSS	Ground	N/A
K5	GVDD2	Power	N/A
K6	M2DQ0	I/O	GVDD2
K7	VSS	Ground	N/A
K8	GVDD2	Power	N/A
K9	M2DQ5	I/O	GVDD2
K10	VSS	Ground	N/A
K11	VDD	Power	N/A
K12	VSS	Ground	N/A
K13	VDD	Power	N/A
K14	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	VSS	Ground	N/A
P16	VSS	Ground	N/A
P17	VSS	Ground	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	NMI	I	QVDD
R3	NMI_OUT[6]	O	QVDD
R4	HRESET[6,7]	I/O	QVDD
R5	INT_OUT[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
U3	GVDD1	Power	N/A
U4	M1DQ15	I/O	GVDD1
U5	M1DQ1	I/O	GVDD1
U6	VSS	Ground	N/A
U7	GVDD1	Power	N/A
U8	M1DQ7	I/O	GVDD1
U9	M1DQ6	I/O	GVDD1
U10	VDD	Power	N/A
U11	VSS	Ground	N/A
U12	M3VDD	Power	N/A
U13	VSS	Ground	N/A
U14	VDD	Power	N/A
U15	VSS	Ground	N/A
U16	VDD	Power	N/A
U17	VSS	Ground	N/A
U18	VDD	Power	N/A
U19	VSS	Ground	N/A
U20	VSS	Ground	N/A
U21	VSS	Ground	N/A
U22	VSS	Non-user	N/A
U23	SR2_TXD0/PE_TXD0[4]	O	SXPVDD2
U24	$\overline{\text{SR2\_TXD0}}$/$\overline{\text{PE\_TXD0}}$[4]	O	SXPVDD2
U25	SXCVDD2	Power	N/A
U26	SXCVSS2	Ground	N/A
U27	$\overline{\text{SR2\_RXD0}}$/$\overline{\text{PE\_RXD0}}$[4]	I	SXCVDD2
U28	SR2_RXD0/PE_RXD0[4]	I	SXCVDD2
V1	M1DQ9	I/O	GVDD1
V2	M1DQ12	I/O	GVDD1
V3	M1DQ13	I/O	GVDD1
V4	$\overline{\text{M1DQS0}}$	I/O	GVDD1
V5	M1DQS0	I/O	GVDD1
V6	M1DM0	O	GVDD1
V7	M1DQ3	I/O	GVDD1
V8	M1DQ2	I/O	GVDD1
V9	M1DQ4	I/O	GVDD1
V10	VSS	Ground	N/A
V11	VDD	Power	N/A
V12	VSS	Ground	N/A
V13	VDD	Power	N/A
V14	VSS	Ground	N/A
V15	VDD	Power	N/A
V16	VSS	Ground	N/A
V17	VDD	Power	N/A
V18	VSS	Ground	N/A
V19	VDD	Power	N/A
V20	NVDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL[5,8]	I/O	NVDD
AC24	GPIO26/TMR3[5,8]	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0[5,8]	I/O	NVDD
AC28	GPIO22[5,8]	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	O	GVDD1
AD8	M1A6	O	GVDD1
AD9	M1A3	O	GVDD1
AD10	M1A10	O	GVDD1
AD11	$\overline{\text{M1RAS}}$	O	GVDD1
AD12	M1A2	O	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	$\overline{\text{M1DQS5}}$	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	$\overline{\text{M1DQS7}}$	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	O	NVDD
AD23	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15[5,8]	I/O	NVDD
AD24	GPIO13/$\overline{\text{IRQ13}}$/RC13[5,8]	I/O	NVDD
AD25	GE_MDC	O	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3[3]	I/O	NVDD
AD28	TDM2RCK/GE1_TD0[3]	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8254 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8254

Characteristic	Symbol	FC-PBGA 29×29 mm[2]		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	18	12	°C/W
Junction-to-ambient, four-layer board[1, 2]	$R_{\theta JA}$	13	9	°C/W
Junction-to-board (bottom)[3]	$R_{\theta JB}$	5		°C/W
Junction-to-case[4]	$R_{\theta JC}$	0.6		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESDC51-6. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-case at the top of the package determined using MIL- STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer

2.4 CLKIN Requirements

Table 5 summarizes the required characteristics for the CLKIN signal.

Table 5. CLKIN Requirements

Parameter/Condition[1]	Symbol	Min	Typ	Max	Unit	Notes
CLKIN duty cycle	—	40	—	60	%	2
CLKIN slew rate	—	1	—	4	V/ns	3
CLKIN peak period jitter	—	—	—	±150	ps	—
CLKIN jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC input swing limits	ΔV_{AC}	1.5	—	—	V	—
Input capacitance	C_{IN}	—	—	15	pf	—

Notes:
1. For clock frequencies, see the *Clock* chapter in the *MSC8254 Reference Manual.*
2. Measured at the rising edge and/or the falling edge at $V_{DDIO}/2$.
3. Slew rate as measured from ±20% to 80% of voltage swing at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF}.

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn} • DDR2 SDRAM • DDR3 SDRAM	I_{MVREFn}	—	 300 250	 µA µA

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8254 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, "HSSI AC Timing Specifications."

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{\mathrm{SR[1–2]\_TX}}$) or a receiver input (SR[1–2]_RX and $\overline{\mathrm{SR[1–2]\_RX}}$). Each signal swings between A volts and B volts where A > B.

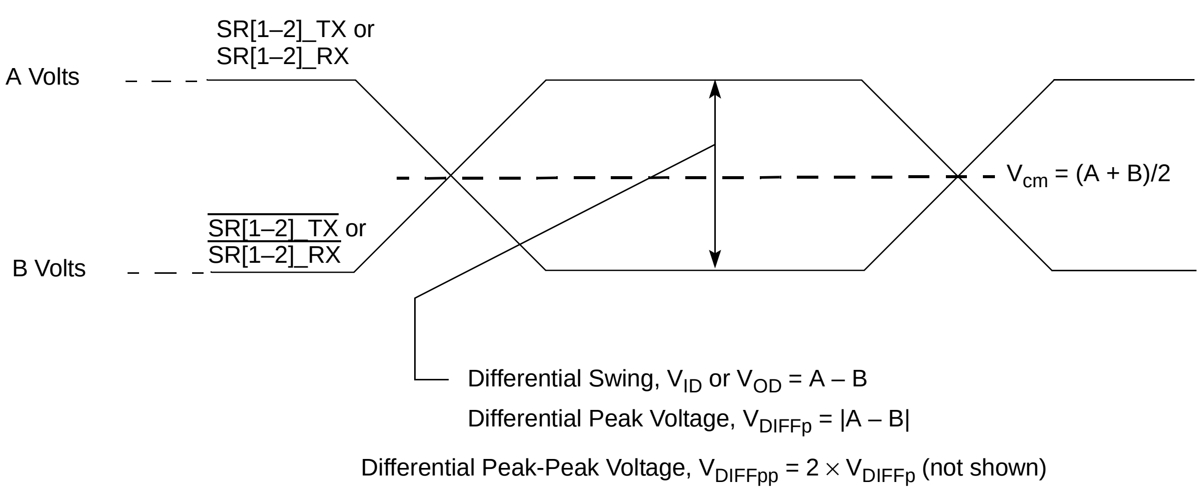


Figure 4. Differential Voltage Definitions for Transmitter or Receiver

Using this waveform, the definitions are listed in Table 10. To simplify the illustration, the definitions assume that the SerDes transmitter and receiver operate in a fully symmetrical differential signalling environment.

Table 10. Differential Signal Definitions

Term	Definition
Single-Ended Swing	The transmitter output signals and the receiver input signals SR[1–2]_TX, $\overline{\text{SR[1–2]\_TX}}$, SR[1–2]_RX and $\overline{\text{SR[1–2]\_RX}}$ each have a peak-to-peak swing of A – B volts. This is also referred to as each signal wire's single-ended swing.
Differential Output Voltage, V_{OD} (or **Differential Output Swing**):	The differential output voltage (or swing) of the transmitter, V_{OD}, is defined as the difference of the two complimentary output voltages: $V_{SR[1–2]\_TX} – V_{\overline{SR[1–2]\_TX}}$. The V_{OD} value can be either positive or negative.
Differential Input Voltage, V_{ID} (or **Differential Input Swing**)	The differential input voltage (or swing) of the receiver, V_{ID}, is defined as the difference of the two complimentary input voltages: $V_{SR[1–2]\_RX} – V_{\overline{SR[1–2]\_RX}}$. The V_{ID} value can be either positive or negative.
Differential Peak Voltage, V_{DIFFp}	The peak value of the differential transmitter output signal or the differential receiver input signal is defined as the differential peak voltage, $V_{DIFFp} = \|A – B\|$ volts.
Differential Peak-to-Peak, $V_{DIFFp-p}$	Since the differential output signal of the transmitter and the differential input signal of the receiver each range from A – B to –(A – B) volts, the peak-to-peak value of the differential transmitter output signal or the differential receiver input signal is defined as differential peak-to-peak voltage, $V_{DIFFp-p} = 2 \times V_{DIFFp} = 2 \times \|(A – B)\|$ volts, which is twice the differential swing in amplitude, or twice of the differential peak. For example, the output differential peak-peak voltage can also be calculated as $V_{TX-DIFFp-p} = 2 \times \|V_{OD}\|$.
Differential Waveform	The differential waveform is constructed by subtracting the inverting signal ($\overline{\text{SR[1–2]\_TX}}$, for example) from the non-inverting signal (SR[1–2]_TX, for example) within a differential pair. There is only one signal trace curve in a differential waveform. The voltage represented in the differential waveform is not referenced to ground. Refer to Figure 16 as an example for differential waveform.
Common Mode Voltage, V_{cm}	The common mode voltage is equal to half of the sum of the voltages between each conductor of a balanced interchange circuit and ground. In this example, for SerDes output, $V_{cm\_out} = (V_{SR[1–2]\_TX} + V_{\overline{SR[1–2]\_TX}}) \div 2 = (A + B) \div 2$, which is the arithmetic mean of the two complimentary output voltages within a differential pair. In a system, the common mode voltage may often differ from one component's output to the other's input. It may be different between the receiver input and driver output circuits within the same component. It is also referred to as the DC offset on some occasions.

To illustrate these definitions using real values, consider the example of a current mode logic (CML) transmitter that has a common mode voltage of 2.25 V and outputs, TD and $\overline{\text{TD}}$. If these outputs have a swing from 2.0 V to 2.5 V, the peak-to-peak voltage swing of each signal (TD or $\overline{\text{TD}}$) is 500 mV p-p, which is referred to as the single-ended swing for each signal. Because the differential signaling environment is fully symmetrical in this example, the transmitter output differential swing (V_{OD}) has the same amplitude as each signal single-ended swing. The differential output signal ranges between 500 mV and –500 mV. In other words, V_{OD} is 500 mV in one phase and –500 mV in the other phase. The peak differential voltage (V_{DIFFp}) is 500 mV. The peak-to-peak differential voltage ($V_{DIFFp-p}$) is 1000 mV p-p.

2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SR1_REF_CLK/$\overline{\text{SR1\_REF\_CLK}}$ or SR2_REF_CLK/$\overline{\text{SR2\_REF\_CLK}}$. Figure 5 shows a receiver reference diagram of the SerDes reference clocks.

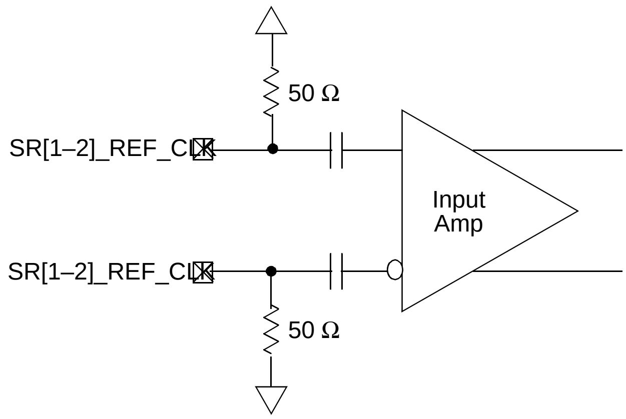


Figure 5. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for V_{DDSXC} are as specified in **Table 3.**
- The SerDes reference clock receiver reference circuit structure is as follows:
  - — The SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 5. Each differential clock input (SR[1–2]_REF_CLK or $\overline{\text{SR[1–2]\_REF\_CLK}}$) has on-chip 50-Ω termination to GND_{SXC} followed by on-chip AC-coupling.
  - — The external reference clock driver must be able to drive this termination.
  - — The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - — When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - — This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA) while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - — If the device driving the SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

Table 14. Serial RapidIO Receiver DC Specifications

Parameter	Symbol	Min	Typical	Max	Units	Notes
Differential input voltage	V_{IN}	200	—	1600	mVp-p	1
Notes: **1.** Measured at receiver.						

2.5.3.4 DC-Level Requirements for SGMII Configurations

Note: Specifications are valid at the recommended operating conditions listed in Table 3

Table 15 describes the SGMII SerDes transmitter AC-coupled DC electrical characteristics. Transmitter DC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX}}$[n]) as shown in Figure 10.

Table 15. SGMII DC Transmitter Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Output high voltage	V_{OH}	—	—	$XV_{DD\_SRDS\text{-}Typ}/2 + \|V_{OD}\|_{-max}/2$	mV	1
Output low voltage	V_{OL}	$XV_{DD\_SRDS\text{-}Typ}/2 - \|V_{OD}\|_{-max}/2$	—	—	mV	1
Output differential voltage ($XV_{DD\text{-}Typ}$ at 1.0 V)	$\|V_{OD}\|$	323	500	725	mV	2,3,4
		296	459	665		2,3,5
		269	417	604		2,3,6
		243	376	545		2,3,7
		215	333	483		2,3,8
		189	292	424		2,3,9
		162	250	362		2,3,10
Output impedance (single-ended)	R_O	40	50	60	Ω	—

Notes:
1. This does not align to DC-coupled SGMII. $XV_{DD\_SRDS2\text{-}Typ}$ = 1.1 V.
2. The $|V_{OD}|$ value shown in the table assumes full multitude by setting srd_smit_lvl as 000 and the following transmit equalization setting in the XMITEQ**AB** (for lanes A and B) or XMITEQ**EF** (for lanes E and F) bit field of Control Register:
   • The MSB (bit 0) of the above bit field is set to zero (selecting the full $V_{DD\text{-}DIFF\text{-}p\text{-}p}$ amplitude which is power up default);
   • The LSB (bit [1–3]) of the above bit field is set based on the equalization settings listed in notes 4 through 10.
3. The $|V_{OD}|$ value shown in the Typ column is based on the condition of $XV_{DD\_SRDS2\text{-}Typ}$ = 1.0 V, no common mode offset variation (V_{OS} =500mV), SerDes transmitter is terminated with 100-Ω differential load between
4. Equalization setting: 1.0x: 0000.
5. Equalization setting: 1.09x: 1000.
6. Equalization setting: 1.2x: 0100.
7. Equalization setting: 1.33x: 1100.
8. Equalization setting: 1.5x: 0010.
9. Equalization setting: 1.71x: 1010.
10. Equalization setting: 2.0x: 0110.
11. $|V_{OD}| = |V_{SR[1–2]\_TXn} - V_{\overline{SR[1–2]\_TXn}}|$. $|V_{OD}|$ is also referred to as output differential peak voltage. $V_{TX\text{-}DIFFp\text{-}p} = 2*|V_{OD}|$.

2.6 AC Timing Characteristics

This section describes the AC timing characteristics for the MSC8254.

2.6.1 DDR SDRAM AC Timing Specifications

This section describes the AC electrical characteristics for the DDR SDRAM interface.

2.6.1.1 DDR SDRAM Input AC Timing Specifications

Table 18 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.8 V.

Table 18. DDR2 SDRAM Input AC Timing Specifications for 1.8 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.20	V
AC input high voltage	V_{IH}	MV_{REF} + 0.20	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.8 ± 5%.				

Table 19 provides the input AC timing specifications for the DDR SDRAM when V_{DDDDR} (typ) = 1.5 V.

Table 19. DDR3 SDRAM Input AC Timing Specifications for 1.5 V Interface

Parameter	Symbol	Min	Max	Unit
AC input low voltage	V_{IL}	—	MV_{REF} – 0.175	V
AC input high voltage	V_{IH}	MV_{REF} + 0.175	—	V
Note: At recommended operating conditions with V_{DDDDR} of 1.5 ± 5%.				

Table 20 provides the input AC timing specifications for the DDR SDRAM interface.

Table 20. DDR SDRAM Input AC Timing Specifications

Parameter	Symbol	Min	Max	Unit	Notes
Controller Skew for MDQS—MDQ/MECC/MDM • 800 MHz data rate • 667 MHz data rate	t_{CISKEW}	 –200 –240	 200 240	 ps ps	1, 2
Tolerated Skew for MDQS—MDQ/MECC/MDM • 800 MHz data rate • 667 MHz data rate	t_{DISKEW}	 –425 –510	 425 510	 ps ps	2, 3

Notes:
1. t_{CISKEW} represents the total amount of skew consumed by the controller between MDQS[n] and any corresponding bit that is captured with MDQS[n]. Subtract this value from the total timing budget.
2. At recommended operating conditions with V_{DDDDR} (1.8 V or 1.5 V) ± 5%
3. The amount of skew that can be tolerated from MDQS to a corresponding MDQ signal is called t_{DISKEW}.This can be determined by the following equation: $t_{DISKEW} = \pm(T \div 4 - abs(t_{CISKEW}))$ where T is the clock period and $abs(t_{CISKEW})$ is the absolute value of t_{CISKEW}.

Figure 11 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

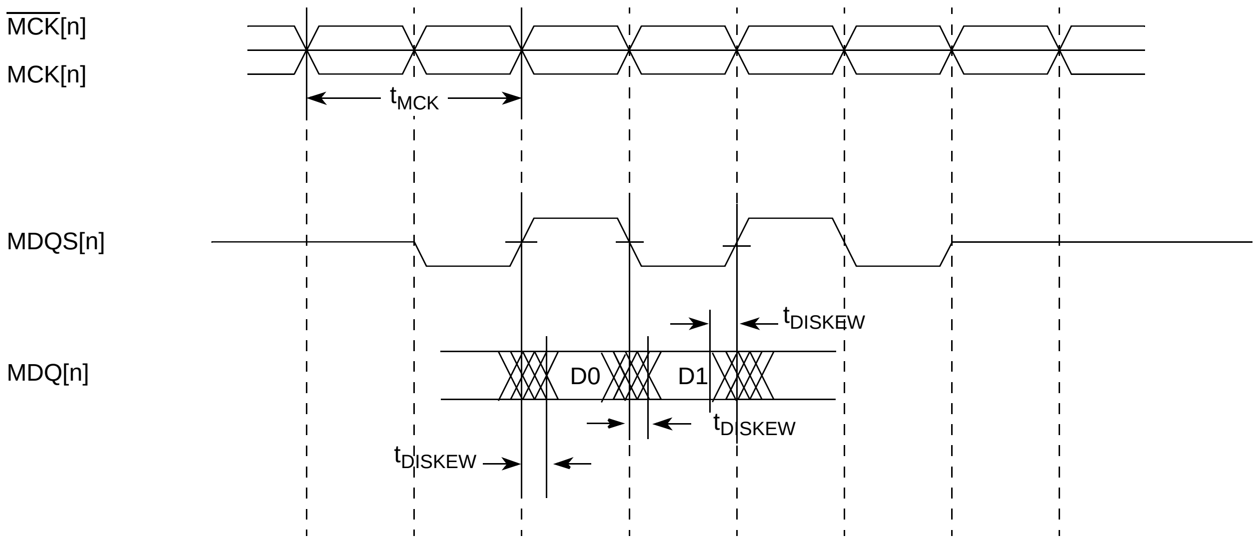


Figure 11. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 21 provides the output AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol [1]	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHAS}	 0.917 1.10	 — —	 ns ns	3
ADDR/CMD output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHAX}	 0.767 1.02	 — —	 ns ns	3
$\overline{\text{MCSn}}$ output setup with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHCS}	 0.917 1.10	 — —	 ns ns	3
$\overline{\text{MCSn}}$ output hold with respect to MCK • 800 MHz data rate • 667 MHz data rate	t_{DDKHCX}	 0.767 1.02	 — —	 ns ns	3
MCK to MDQS Skew • 800 MHz data rate • 667 MHz data rate	t_{DDKHMH}	 –0.4 –0.6	 0.375 0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS • 800 MHz • 667 MHz	t_{DDKHDS}, t_{DDKLDS}	 300 375	 — —	 ps ps	5
MDQ/MECC/MDM output hold with respect to MDQS • 800 MHz • 667 MHz	t_{DDKHDX}, t_{DDKLDX}	 300 375	 — —	 ps ps	5
MDQS preamble	t_{DDKHMP}	$–0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$–0.4 \times t_{MCK}$	$–0.6 \times t_{MCK}$	ns	—

Figure 13 shows the DDR SDRAM output timing diagram.

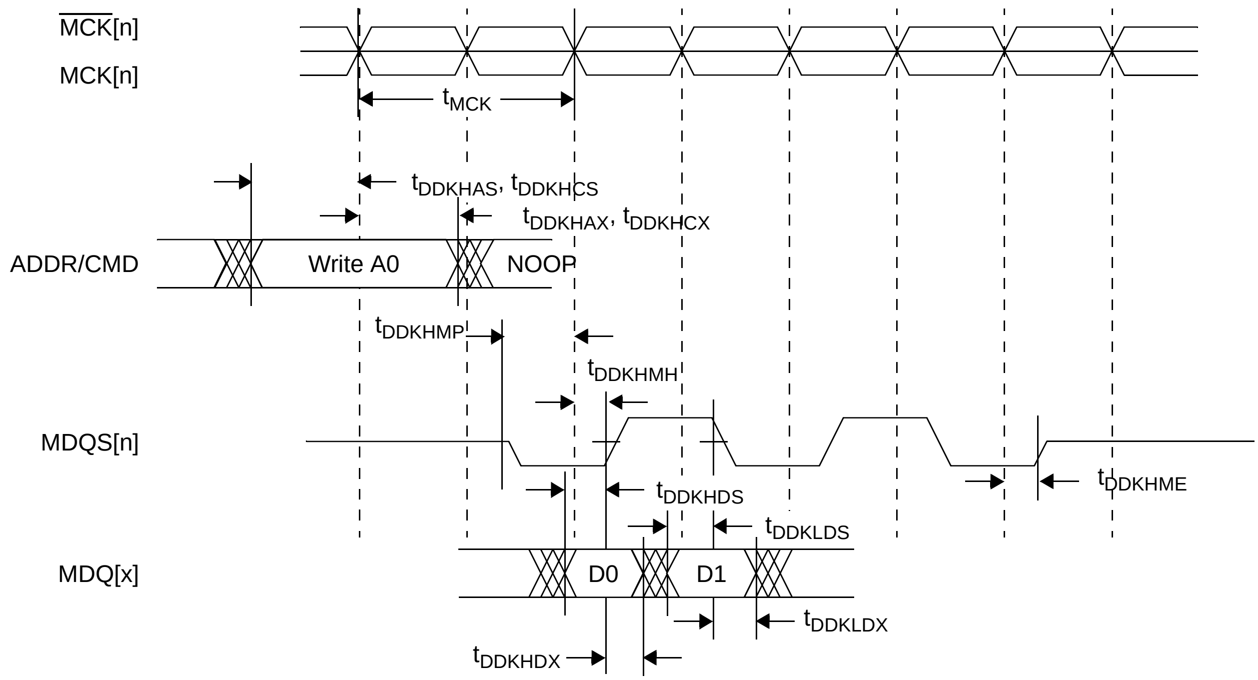


Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.

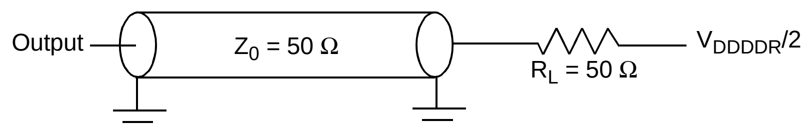


Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.

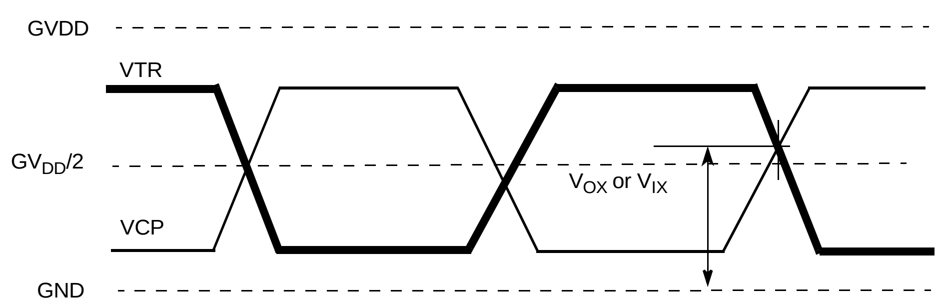


Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

Table 22 provides the DDR2 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 22. DDR2 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.175	0.5 × GVDD + 0.175	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.125	0.5 × GVDD + 0.125	V

Table 23 provides the DDR3 differential specifications for the differential signals MDQS/$\overline{\text{MDQS}}$ and MCK/$\overline{\text{MCK}}$.

Table 23. DDR3 SDRAM Differential Electrical Characteristics

Parameter	Symbol	Min	Max	Unit
Input AC differential cross-point voltage	V_{IXAC}	0.5 × GVDD – 0.150	0.5 × GVDD + 0.150	V
Output AC differential cross-point voltage	V_{OXAC}	0.5 × GVDD – 0.115	0.5 × GVDD + 0.115	V

2.6.2 HSSI AC Timing Specifications

The following subsections define the AC timing requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

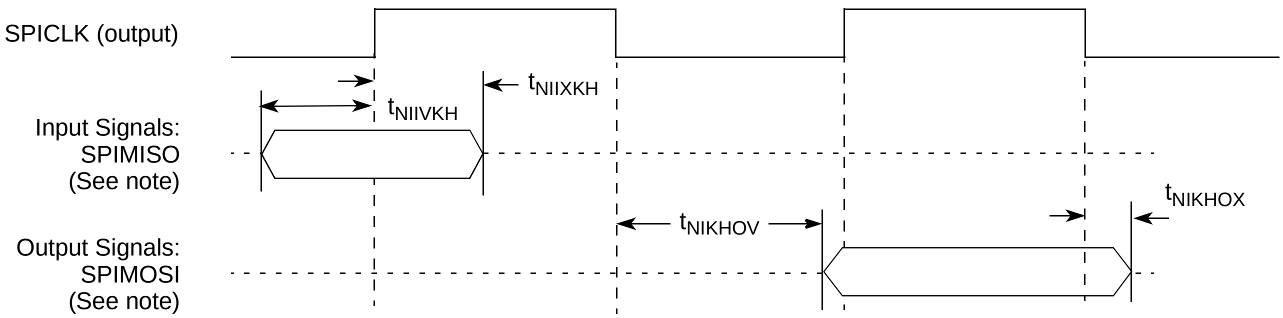
2.6.2.1 AC Requirements for SerDes Reference Clock

Table 24 lists AC requirements for the SerDes reference clocks.

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Table 24. SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ Input Clock Requirements

Parameter	Symbol	Min	Typical	Max	Units	Notes
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ frequency range	t_{CLK_REF}	—	100/125	—	MHz	1
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ clock frequency tolerance	t_{CLK_TOL}	–350	—	350	ppm	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ reference clock duty cycle (measured at 1.6 V)	t_{CLK_DUTY}	40	50	60	%	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ max deterministic peak-peak jitter at 10^{-6} BER	t_{CLK_DJ}	—	—	42	ps	—
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ total reference clock jitter at 10^{-6} BER (peak-to-peak jitter at ref_clk input)	t_{CLK_TJ}	—	—	86	ps	2
SR[1–2]_REF_CLK/$\overline{\text{SR[1–2]\_REF\_CLK}}$ rising/falling edge rate	t_{CLKRR}/t_{CLKFR}	1	—	4	V/ns	3
Differential input high voltage	V_{IH}	200	—	—	mV	4
Differential input low voltage	V_{IL}	—	—	–200	mV	4
Rising edge rate (SR[1–2]_REF_CLK) to falling edge rate (SR[1–2]_REF_CLK) matching	Rise-Fall Matching	—	—	20	%	5, 6



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8254 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8254 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

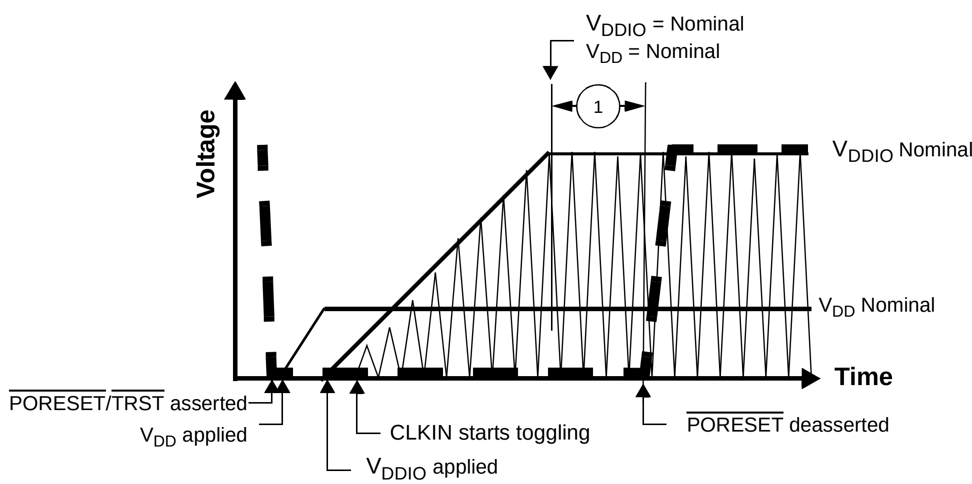


Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the *Reset* chapter in the *MSC8254 Reference Manual*.

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

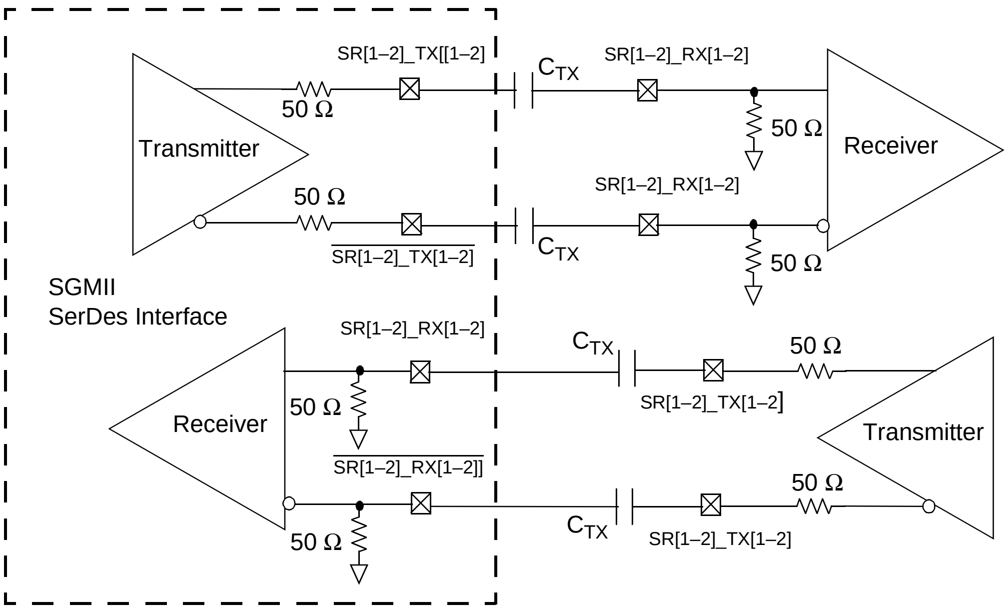


Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8254 DDR ports.

Note: The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin names refer to Table 1.

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS[7–0]}}$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[1–0]}}$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC
MVREF[3]	NC
GVDD1/GVDD2[3]	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the *Clocks* and *General Configuration Registers* chapters in the ***MSC8254 Reference Manual*** for details.
3. For MSC8254 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8254, connecting these pins to GND increases device power consumption.

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

Signal Name	Pin connection
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8254 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8254, connecting these pins to GND increases device power consumption.

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	NC
SR_IMP_CAL_TX	NC
$\overline{\text{SR[1–2]\_REF\_CLK}}$	SXCVSS
SR[1–2]_REF_CLK	SXCVSS
SR[1–2]_RXD[3–0]	SXCVSS
$\overline{\text{SR[1–2]\_RXD[3–0]}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD[3–0]}}$	NC
SR[1–2]_TXD[3–0]	NC
SR[1–2]_PLL_AVDD	In use
SR[1–2]_PLL_AGND	In use
SXPVSS	In use
SXCVSS	In use
SXPVDD	In use
SXCVDD	In use

Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8254 Reference Manual* for details.

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
$\overline{\text{SR[1–2]\_REF\_CLK}}$	In use
SR[1–2]_REF_CLK	In use