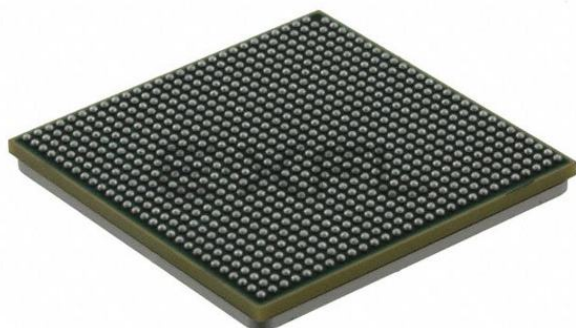




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Understanding [Embedded - DSP \(Digital Signal Processors\)](#)

[Embedded - DSP \(Digital Signal Processors\)](#) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of [Embedded - DSP \(Digital Signal Processors\)](#)

Details

Product Status	Obsolete
Type	SC3850 Quad Core
Interface	Ethernet, I ² C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	800MHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	0°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8254svt800b

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

Note: The information in Table 1 and Table 2 distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Table 1. Signal List by Ball Number

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
A2	M2DQS3	I/O	GVDD2
A3	M2DQS3	I/O	GVDD2
A4	M2ECC0	I/O	GVDD2
A5	M2DQS8	I/O	GVDD2
A6	M2DQS8	I/O	GVDD2
A7	M2A5	O	GVDD2
A8	M2CK1	O	GVDD2
A9	M2CK1	O	GVDD2
A10	M2CS0	O	GVDD2
A11	M2BA0	O	GVDD2
A12	M2CAS	O	GVDD2
A13	M2DQ34	I/O	GVDD2
A14	M2DQS4	I/O	GVDD2
A15	M2DQS4	I/O	GVDD2
A16	M2DQ50	I/O	GVDD2
A17	M2DQS6	I/O	GVDD2
A18	M2DQS6	I/O	GVDD2
A19	M2DQ48	I/O	GVDD2
A20	M2DQ49	I/O	GVDD2
A21	VSS	Ground	N/A
A22	Reserved	NC	—
A23	SXPVDD1	Power	N/A
A24	SXPVSS1	Ground	N/A
A25	Reserved	NC	—
A26	Reserved	NC	—
A27	SXCVDD1	Power	N/A
A28	SXCVSS1	Ground	N/A
B1	M2DQ24	I/O	GVDD2
B2	GVDD2	Power	N/A
B3	M2DQ25	I/O	GVDD2
B4	VSS	Ground	N/A
B5	GVDD2	Power	N/A
B6	M2ECC1	I/O	GVDD2
B7	VSS	Ground	N/A
B8	GVDD2	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
C27	Reserved	NC	—
C28	Reserved	NC	—
D1	GVDD2	Power	N/A
D2	VSS	Ground	N/A
D3	M2DQ29	I/O	GVDD2
D4	GVDD2	Power	N/A
D5	VSS	Ground	N/A
D6	M2ECC5	I/O	GVDD2
D7	GVDD2	Power	N/A
D8	VSS	Ground	N/A
D9	M2A8	O	GVDD2
D10	GVDD2	Power	N/A
D11	VSS	Ground	N/A
D12	M2A0	O	GVDD2
D13	GVDD2	Power	N/A
D14	VSS	Ground	N/A
D15	M2DQ39	I/O	GVDD2
D16	GVDD2	Power	N/A
D17	VSS	Ground	N/A
D18	M2DQ54	I/O	GVDD2
D19	GVDD2	Power	N/A
D20	VSS	Ground	N/A
D21	SXPVSS1	Ground	N/A
D22	SXPVDD1	Power	N/A
D23	SR1_TXD1	O	SXPVDD1
D24	SR1_TXD1	O	SXPVDD1
D25	SXCVSS1	Ground	N/A
D26	SXCVDD1	Power	N/A
D27	SR1_RXD1	I	SXCVDD1
D28	SR1_RXD1	I	SXCVDD1
E1	M2DQ31	I/O	GVDD2
E2	M2DQ30	I/O	GVDD2
E3	M2DQ27	I/O	GVDD2
E4	M2ECC7	I/O	GVDD2
E5	M2ECC6	I/O	GVDD2
E6	M2ECC3	I/O	GVDD2
E7	M2A9	O	GVDD2
E8	M2A6	O	GVDD2
E9	M2A3	O	GVDD2
E10	M2A10	O	GVDD2
E11	M2RAS	O	GVDD2
E12	M2A2	O	GVDD2
E13	M2DQ38	I/O	GVDD2
E14	M2DQS5	I/O	GVDD2
E15	M2DQS5	I/O	GVDD2
E16	M2DQ33	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
E17	M2DQ56	I/O	GVDD2
E18	M2DQ57	I/O	GVDD2
E19	M2DQS7	I/O	GVDD2
E20	Reserved	NC	—
E21	Reserved	NC	—
E22	Reserved	NC	—
E23	SXPVDD1	Power	N/A
E24	SXPVSS1	Ground	N/A
E25	SR1_PLL_AGND ⁹	Ground	SXCVSS1
E26	SR1_PLL_AVDD ⁹	Power	SXCVDD1
E27	SXCVSS1	Ground	N/A
E28	SXCVDD1	Power	N/A
F1	VSS	Ground	N/A
F2	GVDD2	Power	N/A
F3	M2DQ16	I/O	GVDD2
F4	VSS	Ground	N/A
F5	GVDD2	Power	N/A
F6	M2DQ17	I/O	GVDD2
F7	VSS	Ground	N/A
F8	GVDD2	Power	N/A
F9	M2BA2	O	GVDD2
F10	VSS	Ground	N/A
F11	GVDD2	Power	N/A
F12	M2A4	O	GVDD2
F13	VSS	Ground	N/A
F14	GVDD2	Power	N/A
F15	M2DQ42	I/O	GVDD2
F16	VSS	Ground	N/A
F17	GVDD2	Power	N/A
F18	M2DQ58	I/O	GVDD2
F19	M2DQS7	I/O	GVDD2
F20	GVDD2	Power	N/A
F21	SXPVDD1	Power	N/A
F22	SXPVSS1	Ground	N/A
F23	SR1_TXD2/SG1_TX ⁴	O	SXPVDD1
F24	SR1_TXD2/SG1_TX ⁴	O	SXPVDD1
F25	SXCVDD1	Power	N/A
F26	SXCVSS1	Ground	N/A
F27	SR1_RXD2/SG1_RX ⁴	I	SXCVDD1
F28	SR1_RXD2/SG1_RX ⁴	I	SXCVDD1
G1	M2DQS2	I/O	GVDD2
G2	M2DQS2	I/O	GVDD2
G3	M2DQ19	I/O	GVDD2
G4	M2DM2	O	GVDD2
G5	M2DQ21	I/O	GVDD2
G6	M2DQ22	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AB1	M1DQS2	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	M1CK2	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	M1APAR_IN	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA ^{5,8}	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0 ^{5,8}	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1 ^{5,8}	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2 ^{5,8}	I/O	NVDD
AB26	GPIO10/IRQ10/RC10 ^{5,8}	I/O	NVDD
AB27	GPIO5/IRQ5/RC5 ^{5,8}	I/O	NVDD
AB28	GPIO0/IRQ0/RC0 ^{5,8}	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AE9	M1A8	O	GVDD1
AE10	GVDD1	Power	N/A
AE11	VSS	Ground	N/A
AE12	M1A0	O	GVDD1
AE13	GVDD1	Power	N/A
AE14	VSS	Ground	N/A
AE15	M1DQ39	I/O	GVDD1
AE16	GVDD1	Power	N/A
AE17	VSS	Ground	N/A
AE18	M1DQ54	I/O	GVDD1
AE19	GVDD1	Power	N/A
AE20	VSS	Ground	N/A
AE21	GPIO29/UART_TXD ^{5,8}	I/O	NVDD
AE22	TDM1TCK/GE2_RX_CLK ³	I	NVDD
AE23	TDM1RSN/GE2_RX_CTL ³	I/O	NVDD
AE24	VSS	Ground	N/A
AE25	TDM3RCK/GE1_GTX_CLK ³	I/O	NVDD
AE26	TDM3TSN/GE1_RX_CLK ³	I/O	NVDD
AE27	TDM2RSN/GE1_TD2 ³	I/O	NVDD
AE28	TDM2RDT/GE1_TD1 ³	I/O	NVDD
AF1	M1DQ28	I/O	GVDD1
AF2	M1DM3	O	GVDD1
AF3	M1DQ26	I/O	GVDD1
AF4	M1ECC4	I/O	GVDD1
AF5	M1DM8	O	GVDD1
AF6	M1ECC2	I/O	GVDD1
AF7	M1CKE1	O	GVDD1
AF8	M1CK0	O	GVDD1
AF9	M1CK0	O	GVDD1
AF10	M1BA1	O	GVDD1
AF11	M1A1	O	GVDD1
AF12	M1WE	O	GVDD1
AF13	M1DQ37	I/O	GVDD1
AF14	M1DM4	O	GVDD1
AF15	M1DQ36	I/O	GVDD1
AF16	M1DQ32	I/O	GVDD1
AF17	M1DQ55	I/O	GVDD1
AF18	M1DM6	O	GVDD1
AF19	M1DQ53	I/O	GVDD1
AF20	M1DQ52	I/O	GVDD1
AF21	GPIO28/UART_RXD ^{5,8}	I/O	NVDD
AF22	TDM0RSN/GE2_TD2 ³	I/O	NVDD
AF23	TDM0TDT/GE2_TD3 ³	I/O	NVDD
AF24	NVDD	Power	N/A
AF25	TDM2TSN/GE1_TX_CTL ³	I/O	NVDD
AF26	GE1_RX_CTL	I	NVDD

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name ^{1,2}	Pin Type ¹⁰	Power Rail Name
AF27	TDM2TDT/GE1_TX_CLK ³	I/O	NVDD
AF28	TDM3RSN/GE1_RD1 ³	I/O	NVDD
AG1	M1DQ24	I/O	GVDD1
AG2	GVDD1	Power	N/A
AG3	M1DQ25	I/O	GVDD1
AG4	VSS	Ground	N/A
AG5	GVDD1	Power	N/A
AG6	M1ECC1	I/O	GVDD1
AG7	VSS	Ground	N/A
AG8	GVDD1	Power	N/A
AG9	M1A13	O	GVDD1
AG10	VSS	Ground	N/A
AG11	GVDD1	Power	N/A
AG12	$\overline{\text{M1CS1}}$	O	GVDD1
AG13	VSS	Ground	N/A
AG14	GVDD1	Power	N/A
AG15	M1DQ35	I/O	GVDD1
AG16	VSS	Ground	N/A
AG17	GVDD1	Power	N/A
AG18	M1DQ51	I/O	GVDD1
AG19	VSS	Ground	N/A
AG20	GVDD1	Power	N/A
AG21	NVDD	Power	N/A
AG22	TDM1TSN/GE2_TD1 ³	I/O	NVDD
AG23	TDM1RDT/GE2_TX_CLK ³	I/O	NVDD
AG24	TDM0TCK/GE2_GTX_CLK ³	I/O	NVDD
AG25	TDM1TDT/GE2_TD0 ³	I/O	NVDD
AG26	VSS	Ground	N/A
AG27	NVDD	Power	N/A
AG28	TDM3RDT/GE1_RD0 ³	I/O	NVDD
AH1	Reserved.	NC	—
AH2	M1DQS3	I/O	GVDD1
AH3	M1DQS3	I/O	GVDD1
AH4	M1ECC0	I/O	GVDD1
AH5	$\overline{\text{M1DQS8}}$	I/O	GVDD1
AH6	M1DQS8	I/O	GVDD1
AH7	M1A5	O	GVDD1
AH8	$\overline{\text{M1CK1}}$	O	GVDD1
AH9	M1CK1	O	GVDD1
AH10	$\overline{\text{M1CS0}}$	O	GVDD1
AH11	M1BA0	O	GVDD1
AH12	$\overline{\text{M1CAS}}$	O	GVDD1
AH13	M1DQ34	I/O	GVDD1
AH14	M1DQS4	I/O	GVDD1
AH15	M1DQS4	I/O	GVDD1
AH16	M1DQ50	I/O	GVDD1

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8254 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8254.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–3	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage ³		V_{DDPLL0}	–0.3 to 1.1	V
		V_{DDPLL1}	–0.3 to 1.1	V
		V_{DDPLL2}	–0.3 to 1.1	V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	–0.3 to 1.98 –0.3 to 1.65	V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to $0.51 \times V_{DDDDR}$	V
Input DDR voltage		V_{INDDR}	–0.3 to $V_{DDDDR} + 0.3$	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to $V_{DDIO} + 0.3$	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDEXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDEXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage ³		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to $V_{DDEXC} + 0.3$	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C
Notes: - Functional operating conditions are given in Table 3. - Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage. - PLL supply voltage is specified at input of the filter and not at pin of the MSC8254 (see Figure 37 and Figure 38)				

2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.5\text{ V}$.

Table 7. DDR3 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	$0.49 \times V_{DDDDR}$	$0.51 \times V_{DDDDR}$	V	2,3,4
Input high voltage	V_{IH}	$MV_{REF} + 0.100$	V_{DDDDR}	V	5
Input low voltage	V_{IL}	GND	$MV_{REF} - 0.100$	V	5
I/O leakage current	I_{OZ}	-50	50	μA	6
Notes: 1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} at all times. The DRAM and memory controller can use the same or different sources. 2. MV_{REF} is expected to be equal to $0.5 \times V_{DDDDR}$, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed $\pm 1\%$ of the DC value. 3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of $MV_{REF} - 0.4$ and a maximum value of $MV_{REF} + 0.04\text{ V}$. V_{TT} should track variations in the DC-level of MV_{REF}. 4. The voltage regulator for MV_{REF} must be able to supply up to 250 μA. 5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ signals are available in the IBIS models. 6. Output leakage is measured with all outputs are disabled, $0\text{ V} \leq V_{OUT} \leq V_{DDDDR}$.					

2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

Note: At recommended operating conditions (see Table 3) with $V_{DDDDR} = 1.8\text{ V}$ for DDR2 memory or $V_{DDDDR} = 1.5\text{ V}$ for DDR3 memory.

Table 8. DDR2/DDR3 SDRAM Capacitance

Parameter	Symbol	Min	Max	Unit
I/O capacitance: DQ, DQS, $\overline{DQS}$	C_{IO}	6	8	pF
Delta I/O capacitance: DQ, DQS, $\overline{DQS}$	C_{DIO}	—	0.5	pF
Note: Guaranteed by FAB process and micro-construction.				

2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for MV_{REF} .

Note: Values when used at recommended operating conditions (see Table 3).

Table 9. Current Draw Characteristics for MV_{REF}

Parameter / Condition	Symbol	Min	Max	Unit
Current draw for MV_{REFn}	I_{MVREFn}	—	300	μA
• DDR2 SDRAM			250	μA
• DDR3 SDRAM				

2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8254 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, “HSSI AC Timing Specifications.”

2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{SR[1-2]_{TX}}$) or a receiver input (SR[1–2]_RX and $\overline{SR[1-2]_{RX}}$). Each signal swings between A volts and B volts where $A > B$.

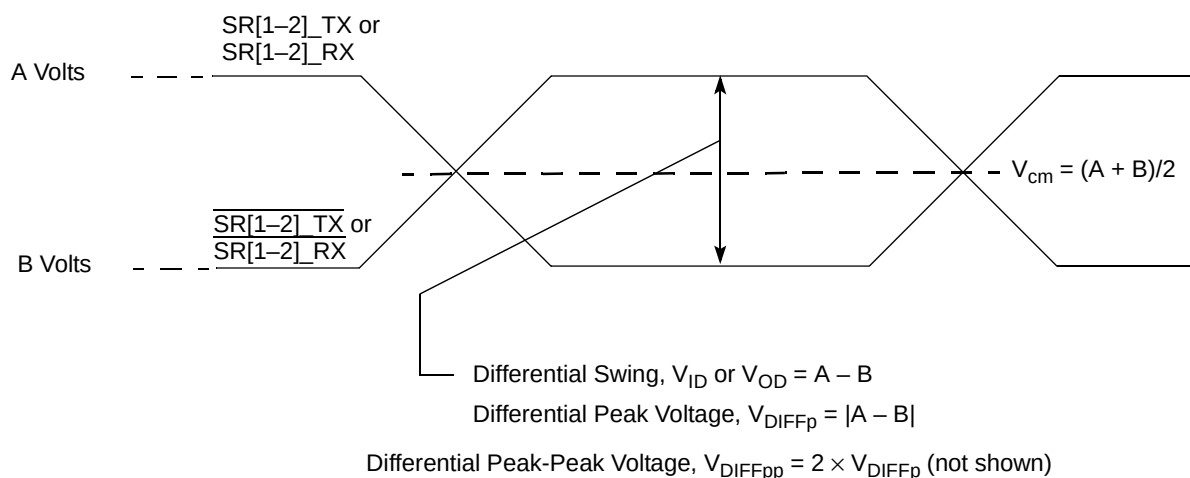


Figure 4. Differential Voltage Definitions for Transmitter or Receiver

2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 17 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- TDM
- GPIO
- UART
- TIMER
- EE
- I²C
- Interrupts ($\overline{\text{IRQn}}$, $\overline{\text{NMI_OUT}}$, $\overline{\text{INT_OUT}}$)
- Clock and resets ($\overline{\text{CLKIN}}$, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)
- DMA External Request
- JTAG signals

Table 17. 2.5 V I/O DC Electrical Characteristics

Characteristic	Symbol	Min	Max	Unit	Notes
Input high voltage	V_{IH}	1.7	—	V	1
Input low voltage	V_{IL}	—	0.7	V	1
Input high current ($V_{IN} = V_{DDIO}$)	I_{IN}	—	30	μA	2
Output high voltage ($V_{DDIO} = \text{min}$, $I_{OH} = -1.0 \text{ mA}$)	V_{OH}	2.0	$V_{DDIO} + 0.3$	V	1
Output low voltage ($V_{DDIO} = \text{min}$, $I_{OL} = 1.0 \text{ mA}$)	V_{OL}	$\text{GND} - 0.3$	0.40	V	1
Notes: 1. The min V_{IL} and max V_{IH} values are based on the respective min and max V_{IN} values listed in Table 3. 2. The symbol V_{IN} represents the input voltage of the supply. It is referenced in Table 3.					

Figure 11 shows the DDR2 and DDR3 SDRAM interface input timing diagram.

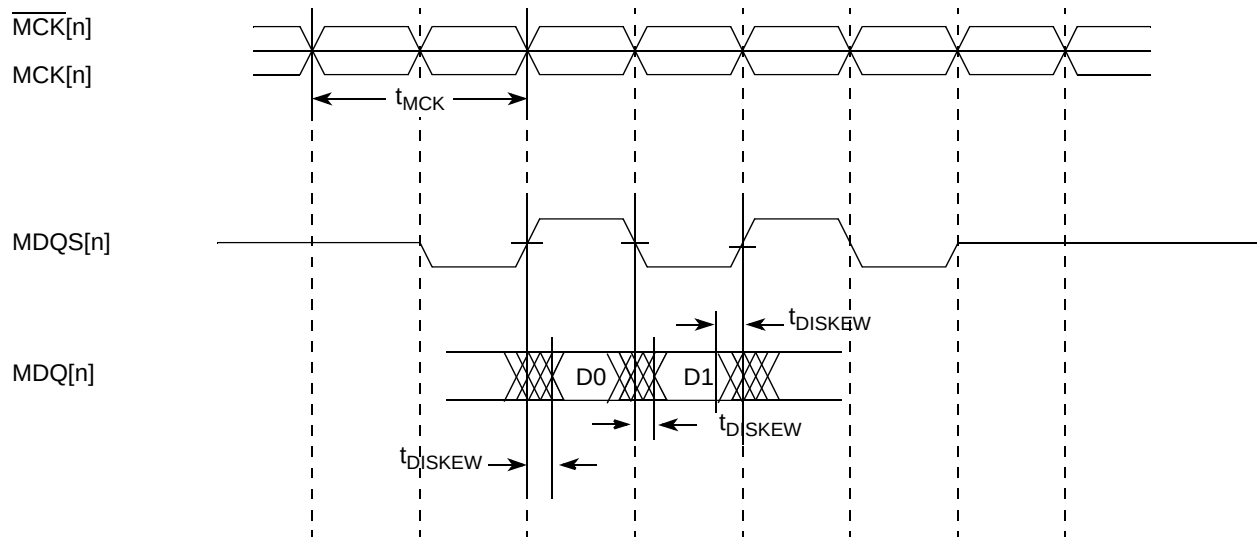


Figure 11. DDR2 and DDR3 SDRAM Interface Input Timing Diagram

2.6.1.2 DDR SDRAM Output AC Timing Specifications

Table 21 provides the output AC timing specifications for the DDR SDRAM interface.

Table 21. DDR SDRAM Output AC Timing Specifications

Parameter	Symbol ¹	Min	Max	Unit	Notes
MCK[n] cycle time	t_{MCK}	2.5	5	ns	2
ADDR/CMD output setup with respect to MCK	t_{DDKHAS}	0.917 1.10	— —	ns ns	3
ADDR/CMD output hold with respect to MCK	t_{DDKHAX}	0.767 1.02	— —	ns ns	3
MCSn output setup with respect to MCK	t_{DDKHCS}	0.917 1.10	— —	ns ns	3
MCSn output hold with respect to MCK	t_{DDKHGX}	0.767 1.02	— —	ns ns	3
MCK to MDQS Skew	t_{DDKMHM}	−0.4 −0.6	0.375 0.6	ns	4
MDQ/MECC/MDM output setup with respect to MDQS	t_{DDKHDS} , t_{DDKLDS}	300 375	— —	ps ps	5
MDQ/MECC/MDM output hold with respect to MDQS	t_{DDKHDX} , t_{DDKLDX}	300 375	— —	ps ps	5
MDQS preamble	t_{DDKHMP}	$−0.9 \times t_{MCK}$	—	ns	—
MDQS postamble	t_{DDKHME}	$−0.4 \times t_{MCK}$	$−0.6 \times t_{MCK}$	ns	—

Figure 13 shows the DDR SDRAM output timing diagram.

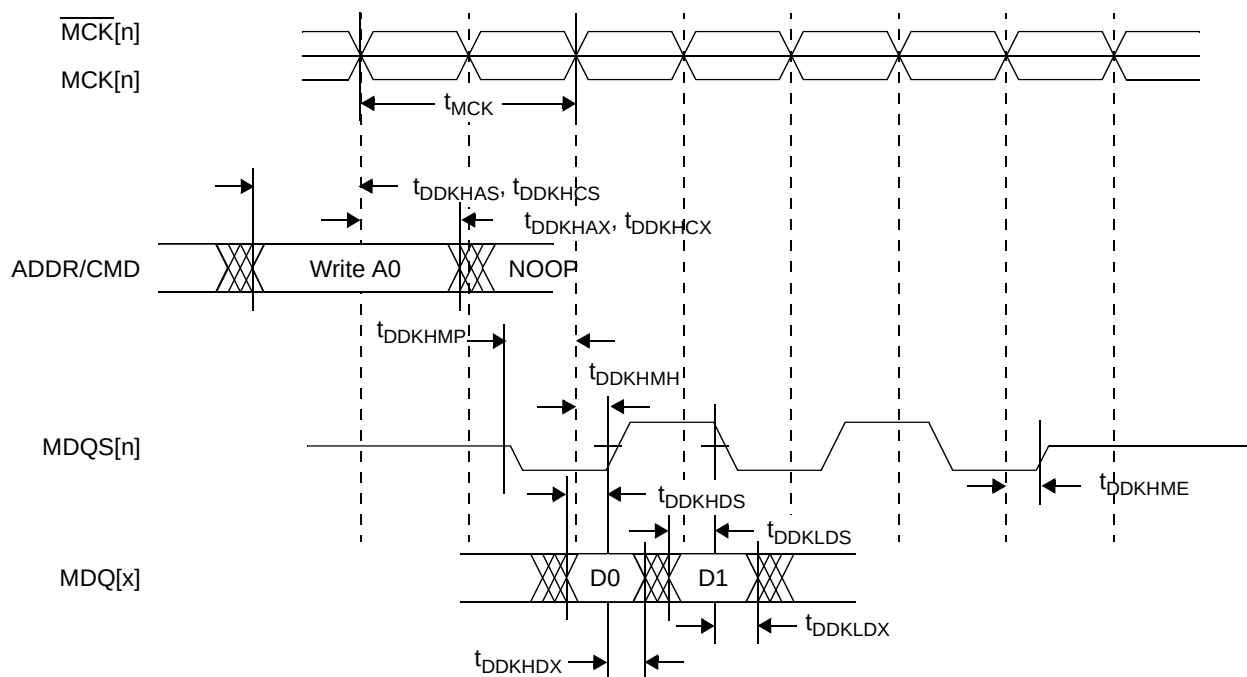


Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.

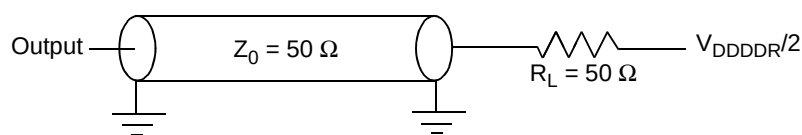


Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.

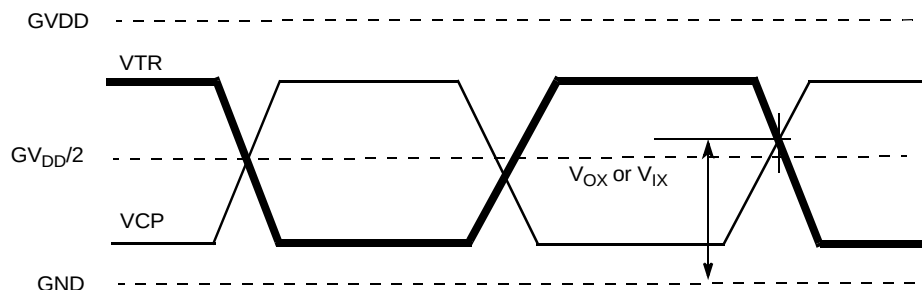


Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: V_{TR} specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).

2.6.3 TDM Timing

Table 31 provides the input and output AC timing specifications for the TDM interface.

Table 31. TDM AC Timing Specifications for 62.5 MHz¹

Parameter	Symbol ²	Min	Max	Unit
TDMxRCK/TDMxTCK	t_{DM}	16.0	—	ns
TDMxRCK/TDMxTCK high pulse width	t_{DM_HIGH}	7.0	—	ns
TDMxRCK/TDMxTCK low pulse width	t_{DM_LOW}	7.0	—	ns
TDM all input setup time	t_{DMIVKH}	3.6	—	ns
TDMxRD hold time	$t_{DMRDIXKH}$	1.9	—	ns
TDMxTFS/TDMxRFS input hold time	$t_{DMFSIXKH}$	1.9	—	ns
TDMxTCK High to TDMxTD output active	t_{DM_OUTAC}	2.5	—	ns
TDMxTCK High to TDMxTD output valid	$t_{DMTKHOV}$	—	9.8	ns
TDMxTD hold time	$t_{DMTKHOX}$	2.5	—	ns
TDMxTCK High to TDMxTD output high impedance	t_{DM_OUTH}	—	9.8	ns
TDMxTFS/TDMxRFS output valid	$t_{DMFSKHOV}$	—	9.25	ns
TDMxTFS/TDMxRFS output hold time	$t_{DMFSKHOX}$	2.0	—	ns

Notes:

1. The symbols used for timing specifications follow the pattern $t_{(\text{first two letters of functional block})(\text{signal})(\text{state})(\text{reference})(\text{state})}$ for inputs and $t_{(\text{first two letters of functional block})(\text{reference})(\text{state})(\text{signal})(\text{state})}$ for outputs. For example, t_{HIKHOX} symbolizes the output internal timing (HI) for the time t_{serial} memory clock reference (K) goes from the high state (H) until outputs (O) are invalid (X).
2. Output values are based on 30 pF capacitive load.
3. Inputs are referenced to the sampling that the TDM is programmed to use. Outputs are referenced to the programming edge they are programmed to use. Use of the rising edge or falling edge as a reference is programmable. T_{DMxTCK} and T_{DMxRCK} are shown using the rising edge.
4. All values are based on a maximum TDM interface frequency of 62.5 MHz.

Figure 20 shows the TDM receive signal timing.

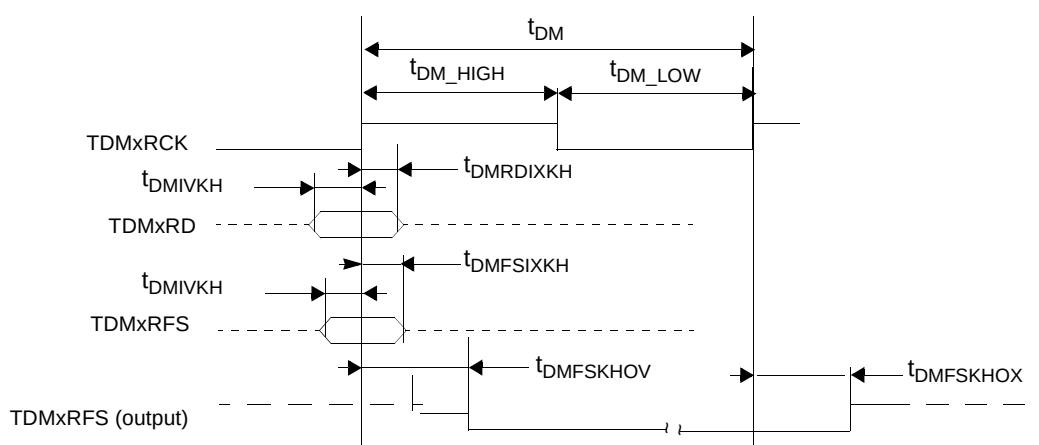


Figure 20. TDM Receive Signals

2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

Table 34. RGMII at 1 Gbps² with On-Board Delay³ AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter) ⁴	t_{SKEWT}	-0.5	—	0.5	ns
Data to clock input skew (at receiver) ⁴	t_{SKEWR}	1	—	2.6	ns
Notes: 1. At recommended operating conditions with V_{DDIO} of $2.5\text{ V} \pm 5\%$. 2. RGMII at 100 Mbps support is guaranteed by design. 3. Program GCR4 as 0x00000000. 4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.					

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

Table 35. RGMII at 1 Gbps² with No On-Board Delay³ AC Timing Specifications

Parameter/Condition	Symbol	Min	Typ	Max	Unit
Data to clock output skew (at transmitter) ⁴	t_{SKEWT}	-2.6	—	-1.0	ns
Data to clock input skew (at receiver) ⁴	t_{SKEWR}	-0.5	—	0.5	ns
Notes: 1. At recommended operating conditions with V_{DDIO} of $2.5\text{ V} \pm 5\%$. 2. RGMII at 100 Mbps support is guaranteed by design. 3. GCR4 should be programmed as 0x000CC330. 4. This implies that PC board design requires clocks to be routed with no additional trace delay					

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

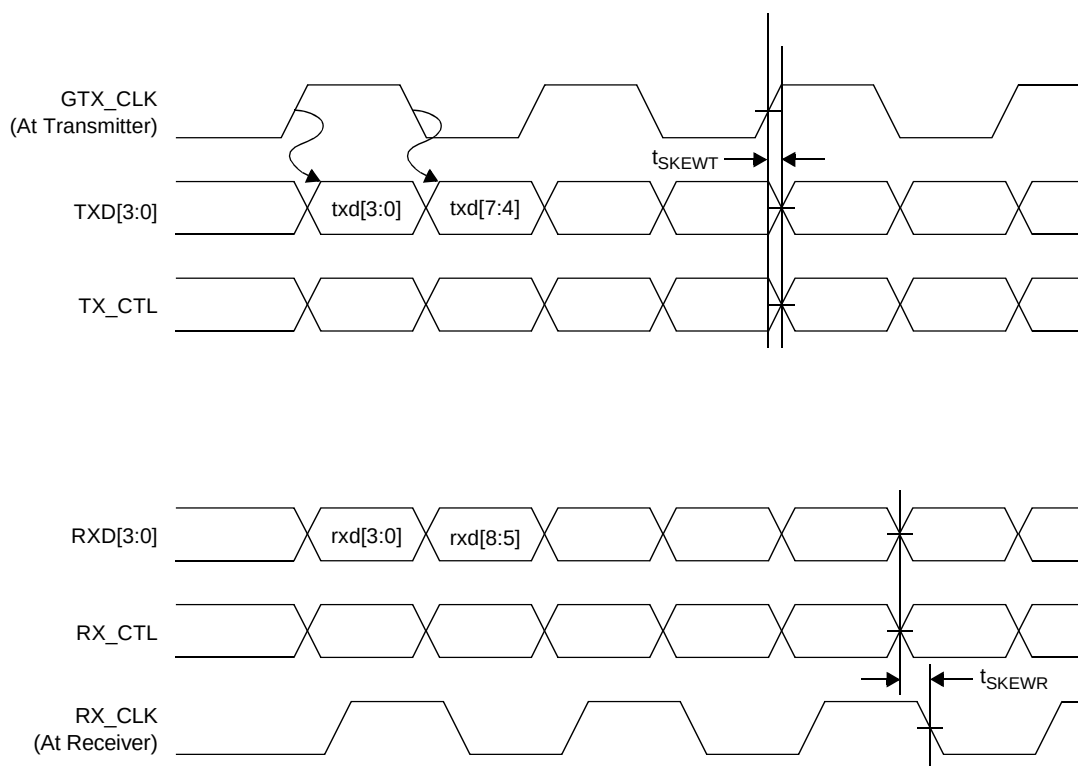
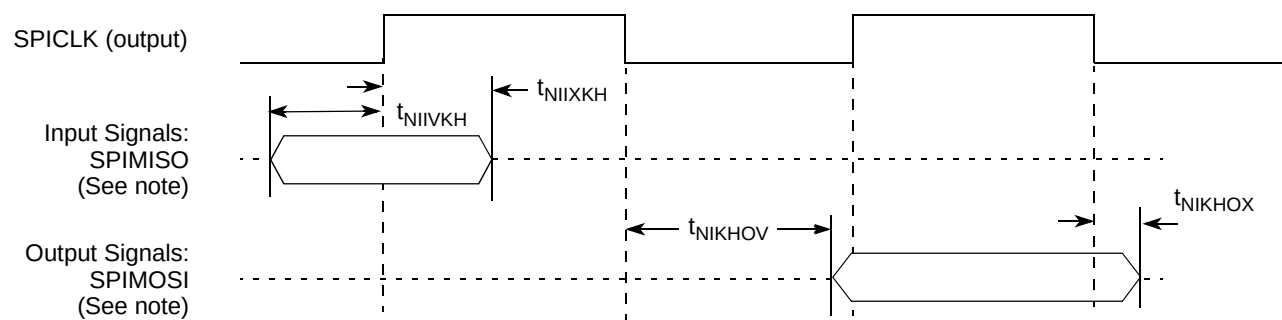


Figure 25. RGMII AC Timing and Multiplexing



Note: measured with $SPMODE[CI] = 0$, $SPMODE[CP] = 0$

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

2.6.7 Asynchronous Signal Timing

Table 35 lists the asynchronous signal timing specifications.

Table 37. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle
Output	t_{OUT}	Asynchronous	Application dependent
Note: Input value relevant for EE0, $\overline{IRQ}[15-0]$, and $\overline{NMI}$ only.			

The following interfaces use the specified asynchronous signals:

- **GPIO.** Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8254 device, that is, when the expected input value is read from the GPIO data register.

- **EE port.** Signals EE0, EE1.
- **Boot function.** Signal STOP_BS.
- **I²C interface.** Signals I2C_SCL and I2C_SDA.
- **Interrupt inputs.** Signals $\overline{IRQ}[15-0]$ and $\overline{NMI}$.
- **Interrupt outputs.** Signals $\overline{INT_OUT}$ and $\overline{NMI_OUT}$ (minimum pulse width is 32 ns).

2.6.8 JTAG Signals

Table 38 lists the JTAG timing specifications shown in Figure 29 through Figure 32.

Table 38. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at $V_M = V_{DDIO}/2$	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
TRST assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 29 shows the test clock input timing diagram

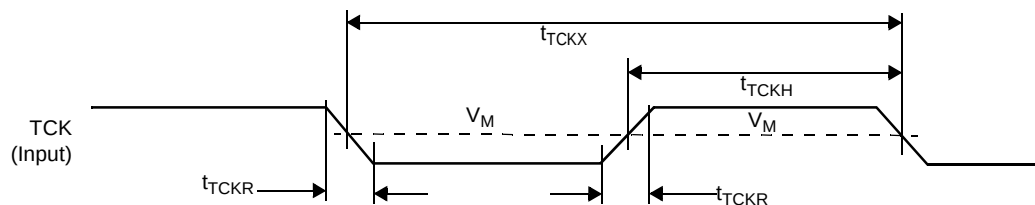


Figure 29. Test Clock Input Timing

Figure 30 shows the boundary scan (JTAG) timing diagram.

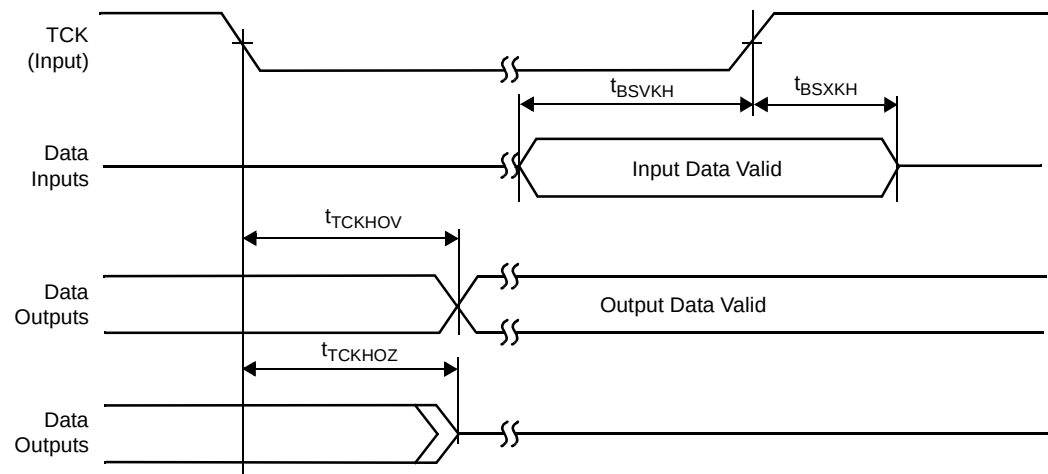


Figure 30. Boundary Scan (JTAG) Timing

Figure 31 shows the test access port timing diagram

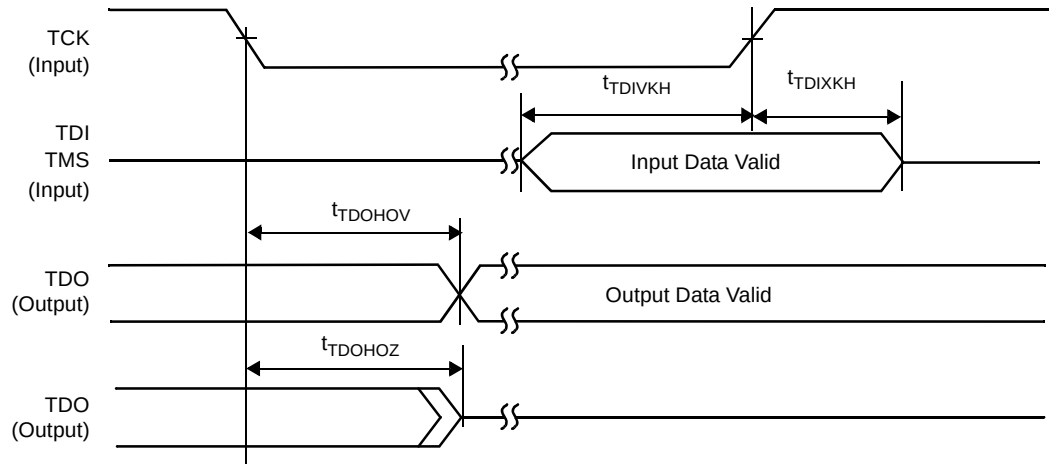


Figure 31. Test Access Port Timing

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.



Figure 32. $\overline{\text{TRST}}$ Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8254 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8254 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

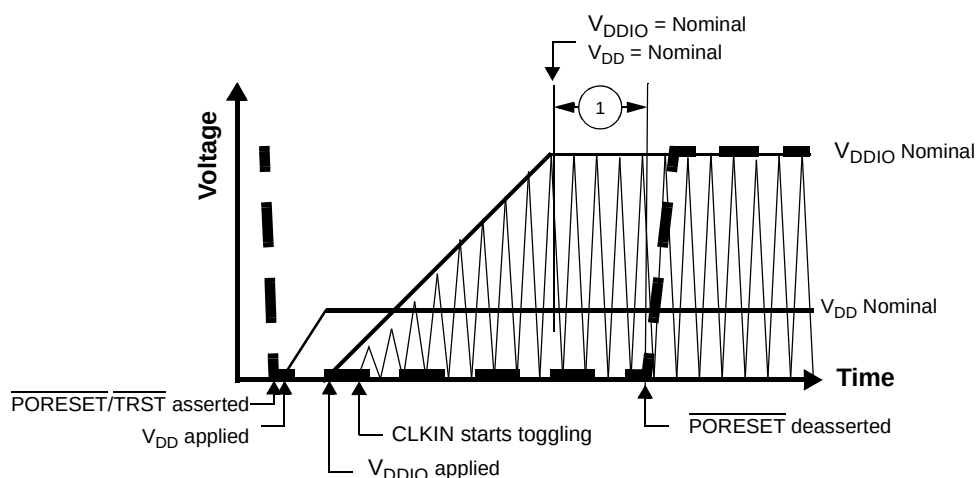


Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the *Reset* chapter in the *MSC8254 Reference Manual*.

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

$$R_{term} = R_{im} - R_{buf}$$

where R_{im} = trace characteristic impedance

R_{buf} = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see AN3556 *MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

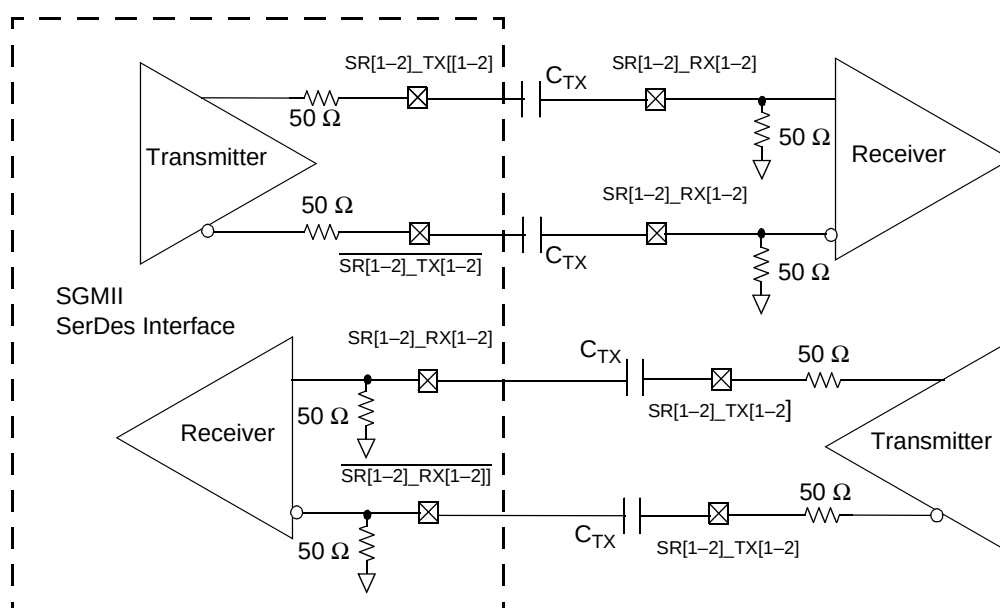


Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

Signal Name	Pin connection
MAPAR_OUT	NC
MAPAR_IN	NC
Notes: 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2. 2. For MSC8254 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8254, connecting these pins to GND increases device power consumption.	

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	NC
SR_IMP_CAL_TX	NC
$\overline{\text{SR[1-2]_REF_CLK}}$	SXCVSS
SR[1-2]_REF_CLK	SXCVSS
SR[1-2]_RXD[3-0]	SXCVSS
$\overline{\text{SR[1-2]_RXD[3-0]}}$	SXCVSS
$\overline{\text{SR[1-2]_TXD[3-0]}}$	NC
SR[1-2]_TXD[3-0]	NC
SR[1-2]_PLL_AVDD	In use
SR[1-2]_PLL_AGND	In use
SXPVSS	In use
SXCVSS	In use
SXPVDD	In use
SXCVDD	In use
Note: All lanes in the HSSI SerDes should be powered down. Refer to the <i>MSC8254 Reference Manual</i> for details.	

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
$\overline{\text{SR[1-2]_REF_CLK}}$	In use
SR[1-2]_REF_CLK	In use