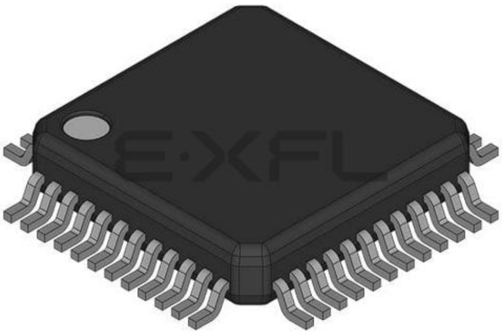


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	39
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag128clf

- System Clock Sources
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Frequency-locked-loop (FLL) controlled by internal or external reference; trimmable internal reference allows 0.2% resolution and 2% deviation (1% across 0 to 70 ºC)
- Peripherals
  - ADC — 24 analog inputs with 12 bits resolution; output formatted in 12-, 10- or 8-bit right-justified format; single or continuous conversion (automatic return to idle after single conversion); interrupt or DMA request when conversion complete; operation in low-power modes for lower noise operation; asynchronous clock source for lower noise operation; selectable asynchronous hardware conversion triggers from RTC, PDB, or iEvent; dual samples based on hardware triggers during ping-pong mode; on-chip temperature sensor
  - PDB — 16-bit of resolution with prescaler; seven possible trigger events input; positive transition of trigger event signal initiates the counter; support continuous trigger or single shot, bypass mode; supports two triggered delay outputs or ORed together; pulsed output could be used for HSCMP windowing signal
  - iEvent — User programmable combinational boolean output using the four selected iEvent input channels for use as interrupt requests, DMA transfer requests, or hardware triggers
  - FTM — Two 6-channel flexible timer/PWM modules with DMA request option; deadtime insertion is available for each complementary channel pair; channels operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs); 16-bit free-running counter; the load of the FTM registers which have write buffer can be synchronized; write protection for critical registers; backwards compatible with TPM
  - TPM — 16-bit free-running or modulo up/down count operation; two channels, each channel may be input capture, output compare, or edge-aligned PWM; one interrupt per channel plus terminal count interrupt
  - CRC — High speed hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial; error detection for all single, double, odd, and most multi-bit errors; programmable initial seed value
  - HSCMP — Two analog comparators with selectable interrupt on rising edge, falling edge, or either edges of comparator output; the positive and negative inputs of the comparator are both driven from 4-to-1 muxes; programmable voltage reference from two internal DACs; support DMA transfer
  - IIC — Compatible with IIC bus standard and SMBus version 2 features; up to 100 kbps with maximum bus loading; multi-master operation; software programmable for one of 64 different serial clock frequencies; programmable slave address and glitch input filter; interrupt driven byte-by-byte data transfer; arbitration lost interrupt with automatic mode switching from master to slave; calling address identification interrupt; bus busy detection; broadcast and 10-bit address extension; address matching causes wake-up when MCU is in Stop3 mode; DMA support
  - SCI — Two serial communications interface modules with optional 13-bit break; full-duplex, standard non-return-to-zero (NRZ) format; double-buffered transmitter and receiver with separate enables; 13-bit baud rate selection with /32 fractional divide; interrupt-driven or polled operation; hardware parity generation and checking; programmable 8-bit or 9-bit character length; receiver wakeup by idle-line or address-mark; address match feature in receiver to reduce address-mark wakeup ISR overhead; 1/16 bit-time noise detection; DMA transmission for both transmit and receive
  - SPI — Two serial peripheral interfaces with full-duplex or single-wire bidirectional option; double-buffered transmitter and receiver; master or slave mode operation; selectable MSB-first or LSB-first shifting; 8-bit or 16-bit data modes; programmable transmit bit rate; receive data buffer hardware match feature; DMA transmission for transmit and receive
- Input/Output
  - Up to 69 GPIOs and one Input-only pin
  - Interrupt or DMA request with selectable polarity on all input pins
  - Programmable glitch filter, hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
  - Independent pin value register to read logic level on digital pin
  - Up to 16 rapid general purpose I/O (RGPIO) pins connected to the processor’s local 32-bit platform bus with set, clear, and faster toggle functionality

Table of Contents

List of Tables

List of Figures

1 MCF51AG128 Family Configurations

1.1 Device Comparison

The following table compares the various device derivatives available within the MCF51AG128 series MCUs.

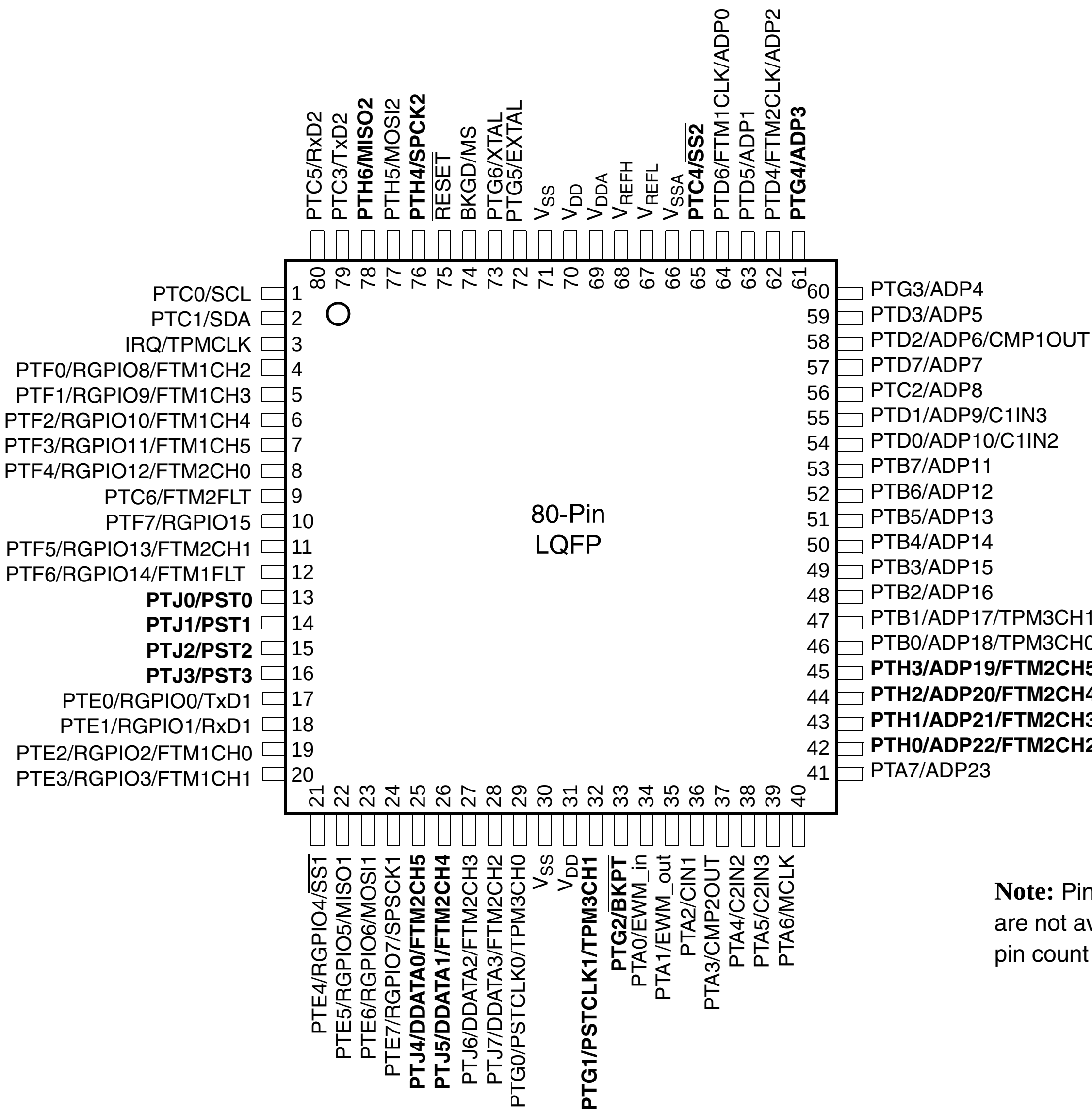
Table 1. MCF51AG128 Series Device Comparison

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
Flash memory size (KB)	128			96		
RAM size (KB)	16					
ColdFire V1 core with BDM (background debug module)	Yes					
HSCMP (analog comparator)	2	2	1	2	2	1
ADC (analog-to-digital converter) channels (12-bit)	24	19	12	24	19	12
CRC (cyclic redundancy check)	Yes					
DAC	2	2	1	2	2	1
DMA controller	4-ch					
iEvent (intelligent Event module)	Yes					
EWM (External Watchdog Monitor)	Yes					
WDOG (Watchdog timer)	Yes					
RTC	Yes					
DBG (debug module)	Yes					
IIC (inter-integrated circuit)	1	1	No	1	1	No
IRQ (interrupt request input)	Yes					
INTC (interrupt controller)	Yes					
LVD (low-voltage detector)	Yes					
ICS (internal clock source)	Yes					
OSC (crystal oscillator)	Yes					
Port I/O[1]	69	53	39	69	53	39
RGPIO (rapid general-purpose I/O)	16	16	15	16	16	15
SCI (serial communications interface)	2					
SPI1 (serial peripheral interface)	Yes					
SPI2 (serial peripheral interface)	Yes	No	No	Yes	No	No
FTM1 (flexible timer module) channels	6[2]					
FTM2 channels	6[2]					

1.4 Pin Assignments

This section describes the pin assignments for the available packages.

Figure 2 shows the pinout of the 80-pin LQFP.



Note: Pin names in **bold** are not available in lower pin count packages.

Figure 2. 80-Pin LQFP

Table 3 shows the package pin assignments.

Table 3. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest		
80	64	48	Port Pin	Alt 1	Alt 2
1	1	—	PTC0	SCL	
2	2	—	PTC1	SDA	
3	3	1	IRQ	TPMCLK[1]	
4	4	2	PTF0	RGPIO8	FTM1CH2
5	5	3	PTF1	RGPIO9	FTM1CH3
6	6	4	PTF2	RGPIO10	FTM1CH4
7	7	5	PTF3	RGPIO11	FTM1CH5
8	8	6	PTF4	RGPIO12	FTM2CH0
9	9	7	PTC6	FTM2FLT	
10	10	8	PTF7	RGPIO15	
11	11	9	PTF5	RGPIO13	FTM2CH1
12	12	10	PTF6	RGPIO14	FTM1FLT
13	—	—	PTJ0	PST0	
14	—	—	PTJ1	PST1	
15	—	—	PTJ2	PST2	
16	—	—	PTJ3	PST3	
17	13	11	PTE0	RGPIO0	TxD1
18	14	12	PTE1	RGPIO1	RxD1
19	15	13	PTE2	RGPIO2	FTM1CH0
20	16	—	PTE3	RGPIO3	FTM1CH1
21	17	14	PTE4	RGPIO4	$\overline{SS1}$
22	18	15	PTE5	RGPIO5	MISO1
23	19	16	PTE6	RGPIO6	MOSI1
24	20	17	PTE7	RGPIO7	SPSCK1
25	—	—	PTJ4	DDATA0	FTM2CH5
26	—	—	PTJ5	DDATA1	FTM2CH4
27	21	18	PTJ6	DDATA2	FTM2CH3
28	22	19	PTJ7	DDATA3	FTM2CH2
29	23	20	PTG0	PSTCLK0	TPM3CH0
30	24	21	V_{SS}		
31	25	22	V_{DD}		
32	—	—	PTG1	PSTCLK1	TPM3CH1
33	—	—	PTG2	$\overline{BKPT}$	
34	26	23	PTA0	EWM_in	
35	27	24	PTA1	EWM_out	
36	28	—	PTA2	CIN1	
37	29	25	PTA3	CMP2OUT	
38	30	—	PTA4	C2IN2	
39	31	—	PTA5	C2IN3	
40	32	—	PTA6	MCLK	

[1] TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AG128 series MCUs, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2 Junction to Ambient Natural Convection
3 1s — Single layer board, one signal layer
4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \qquad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \qquad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \qquad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—

Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
14	 C P C	Stop3 mode supply current –40 °C 25 °C 105 °C	$S3I_{DD}$	5	 1.2 1.7 43.3	 3 3 60	µA
	C P C	–40 °C 25 °C 105 °C		3	1.04 1.6 45.5	3 3 60	µA
15	 C P C	Stop4 mode supply current –40 °C 25 °C 105 °C	$S4I_{DD}$	5	 106 109 155	 130 130 170	µA
	C P C	–40 °C 25 °C 105 °C		3	95 98 142	130 130 170	µA
16	C	RTC adder to stop2 or stop3[5], 25 °C	$S23I_{DDRTC}$	5	300	—	nA
				3	300	—	nA
17	C	Adder to stop3 for oscillator enabled[6] (ERCLKEN = 1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5	—	µA

1 Typicals are measured at 25 °C.
2 Values given here are preliminary estimates prior to completing characterization.
3 Code run from flash, FEI mode, and does not include any dc loads on port pins. Bus CLK= (CPU CLK/2)
4 GPIO filters are working on LPO clock.
5 Most customers are expected to use auto-wakeup from stop2 or stop3 instead of the higher current wait mode.
6 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

Figure 9. Run Current at Different Conditions

2.7 High Speed Comparator (HSCMP) Electricals

Table 11. HSCMP Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current, high speed mode (EN = 1, PMODE = 1)	I_{DDAHS}	—	200	—	µA
3	T	Supply current, low speed mode (EN = 1, PMODE = 0)	I_{DDALS}	—	20	—	µA
4	—	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
5	D	Analog input offset voltage	V_{AIO}	—	5	40	mV
6	D	Analog Comparator hysteresis	V_H	3.0	9.0	20.0	mV
7	D	Propagation delay, high speed mode (EN = 1, PMODE = 1)	t_{DHS}	—	70	120	ns
8	D	Propagation delay, low speed mode (EN = 1, PMODE = 0)	t_{DLS}	—	400	600	ns
9	D	Analog Comparator initialization delay	t_{AINIT}	—	400	—	ns

2.8 Digital to Analog (DAC) Characteristics

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DDA}	2.7	—	5.5	V
2	D	Supply current (enabled)	I_{DDAC}	—	—	20	µA
3	D	Supply current (stand-by)	I_{DDACS}	—	—	150	nA
4	D	DAC reference input voltage	V_{in1},V_{in2}	V_{SSA}	—	V_{DDA}	V
5	D	DAC setup delay	t_{PRGST}	—	1000	—	nS
6	D	DAC step size	V_{step}	$3V_{in}/128$	$V_{in}/32$	$5V_{in}/128$	V
7	D	DAC output voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.9 ADC Characteristics

Table 12. 5V 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
			Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	—
2	D	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	—

Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
16	D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	—
17	D	Temp Sensor Slope	–40 °C — 25 °C	m	—	3.266	—	mV/°C	—
			25 °C — 85 °C		—	3.638	—		

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

[3] Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

[4] Based on input pad leakage current. Refer to pad electricals.

2.10 External Oscillator (XOSC) Characteristics

Table 14. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	 32 1 1 1	 — — — —	 38.4 16 16 8	 kHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		 10 1	—	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[3]	 $t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	 — — — —	 1500 2000 3 7	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode [2] FBE mode[2] FBELP mode	f_{extal}	 0.03125 0 0	 — — —	 50.33 50.33 50.33	MHz

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

Table 15. ICS Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
10	D	FLL acquisition time [3]	$t_{fll\_acquire}$	—	—	1	ms
11	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	%f_{dco}
12	D	Loss of external clock minimum freq. (RANGE = 0) • ext. clock freq: above (3/5)f_{int}, never reset • ext. clock freq: between (2/5)f_{int} and (3/5)f_{int}, maybe reset (phase dependency) • ext. clock freq: below (2/5)f_{int}, always reset	f_{loc_low}	(3/5) x f_{int}	—	—	kHz
13	D	Loss of external clock minimum freq. (RANGE = 1) • ext. clock freq: above (16/5)f_{int}, never reset • ext. clock freq: between (15/5)f_{int} and (16/5)f_{int}, maybe reset (phase dependency) • ext. clock freq: below (15/5)f_{int}, always reset	f_{loc_high}	(16/5) x f_{int}	—	—	kHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry by V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

2.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.12.1 Control Timing

Table 16. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency ($t_{cyc} = 1/f_{Bus}$)	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width[2] ($t_{cyc} = 1/f_{Self\_reset}$)	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	100 1.5 x t_{cyc}	—	—	ns
8		Port rise and fall time (load = 30 pF for SPI, rest 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	— —	11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

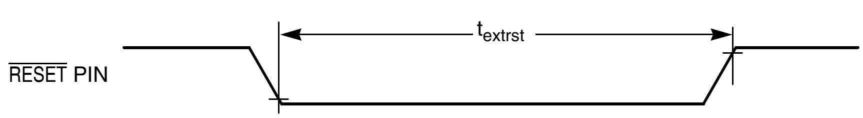


Figure 11. Reset Timing

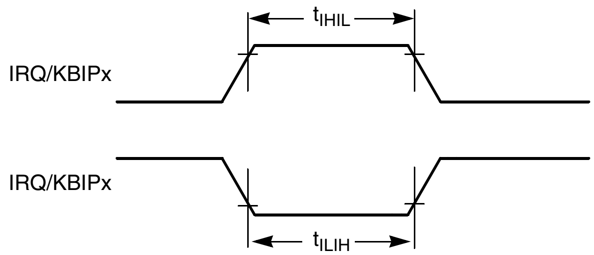


Figure 12. IRQ/KBIPx Timing

2.12.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 17. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

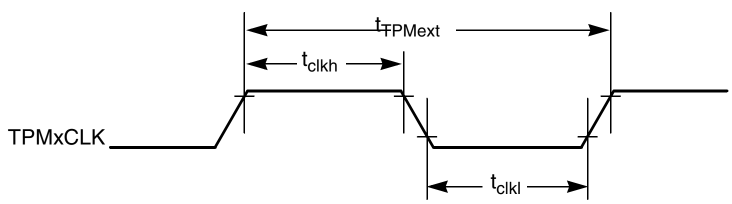


Figure 13. Timer External Clock

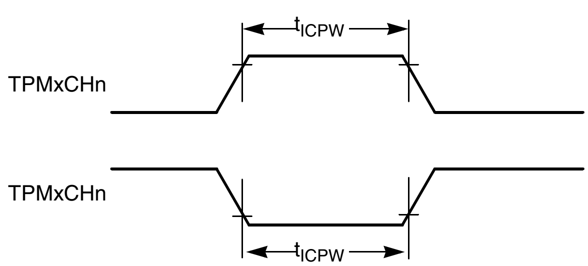
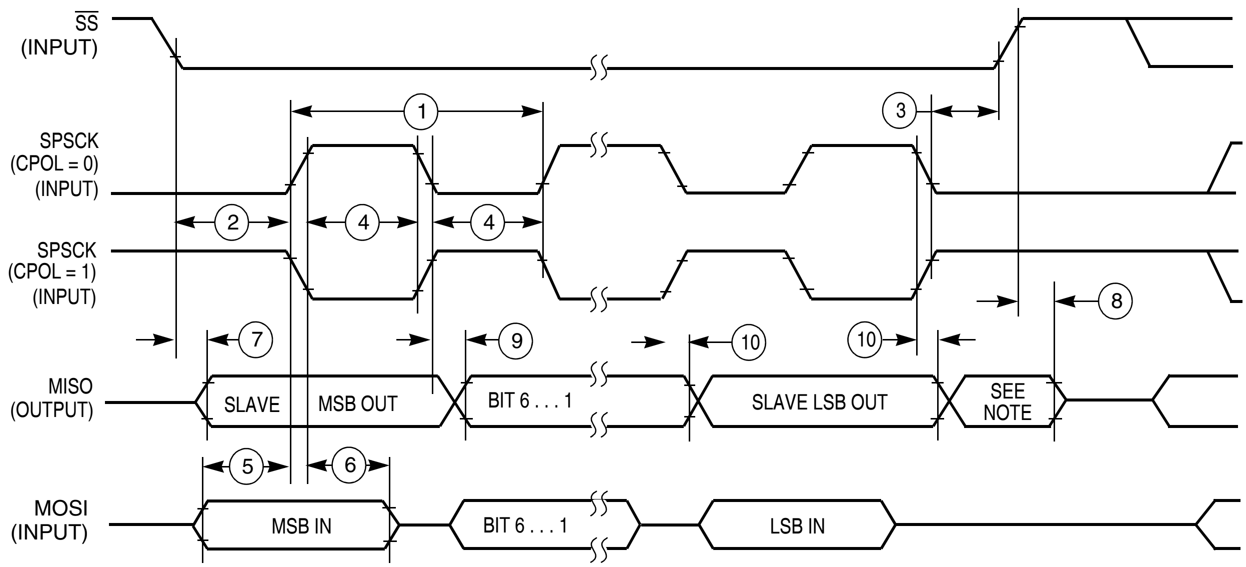


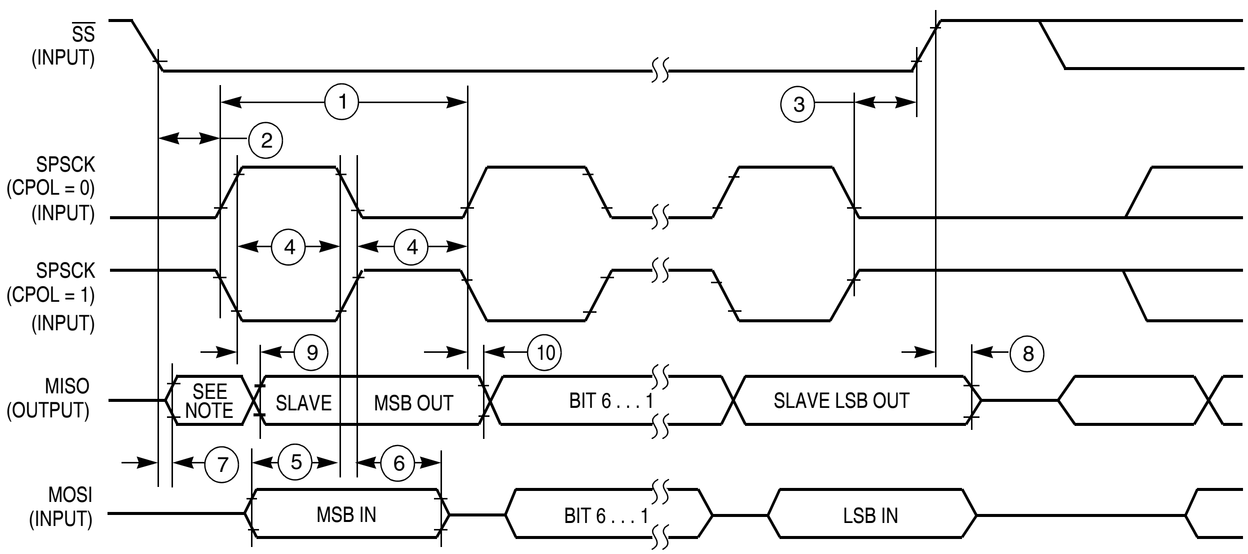
Figure 14. Timer Input Capture Pulse



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see *MCF51AG128 Reference Manual*.

Table 19. Flash Characteristics

Num	C	Characteristic	Symbol	Min	Typical[1]	Max	Unit
1	—	Supply voltage for program/erase	$V_{prog/erase}$	2.7		5.5	V
2	—	Supply voltage for read operation	V_{Read}	2.7		5.5	V
3	—	Internal FCLK frequency[2]	f_{FCLK}	150		200	kHz
4	—	Internal FCLK period (1/FCLK)	t_{Fcyc}	5		6.67	μs
5	—	Byte program time (random location)[2]	t_{prog}		9		t_{Fcyc}
6	—	Byte program time (burst mode)[2]	t_{Burst}		4		t_{Fcyc}
7	—	Page erase time[3]	t_{Page}		4000		t_{Fcyc}
8	—	Mass erase time[2]	t_{Mass}		20,000		t_{Fcyc}
9	C	Program/erase endurance[4] T_L to T_H = –40 °C to 105 °C T = 25 °C		 10,000 —	 — 100,000	 — —	cycles
10	C	Data retention[5]	t_{D_ret}	15	100	—	years

[1] Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

[2] The frequency of this clock is controlled by a software setting.

[3] These values are hardware state machine controlled. User code does not need to count cycles. This information supplied for calculating approximate time to program and erase.

[4] **Typical endurance for flash** was evaluated for this product family on the HC9S12Dx64. For additional information on how Freescale Semiconductor defines typical endurance, please refer to Engineering Bulletin EB619/D, *Typical Endurance for Nonvolatile Memory*.

[5] **Typical data retention** values are based on intrinsic capability of the technology measured at high temperature and de-rated to 25 °C using the Arrhenius equation. For additional information on how Freescale Semiconductor defines typical data retention, please refer to Engineering Bulletin EB618/D, *Typical Data Retention for Nonvolatile Memory.*

2.14 EMC Performance

Electromagnetic compatibility (EMC) performance is highly dependant on the environment in which the MCU resides. Board design and layout, circuit topology choices, location and characteristics of external components as well as MCU software operation all play a significant role in EMC performance. The system designer should consult Freescale applications notes such as AN2321, AN1050, AN1263, AN2764, and AN1259 for advice and guidance specifically targeted at optimizing EMC performance.

2.14.1 Radiated Emissions

Microcontroller radiated RF emissions are measured from 150 kHz to 1 GHz using the TEM/GTEM Cell method in accordance with the IEC 61967-2 and SAE J1752/3 standards. The measurement is performed with the microcontroller installed on a custom EMC evaluation board while running specialized EMC test software. The radiated emissions from the microcontroller are measured in a TEM cell in two package orientations (North and East). For more detailed information concerning the evaluation results, conditions and setup, please refer to the EMC Evaluation Report for this device.

3 Ordering Information

This section contains ordering information for MCF51AG128 devices.

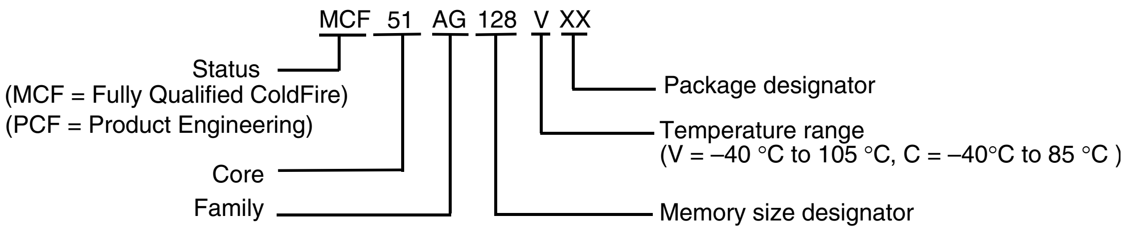


Table 20. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51AG128VLK	MCF51AG128 ColdFire Microcontroller	128 / 16	80 LQFP	–40°C to 105°C
MCF51AG128VLH	MCF51AG128 ColdFire Microcontroller	128 / 16	64 LQFP	–40°C to 105°C
MCF51AG128VQH	MCF51AG128 ColdFire Microcontroller	128 / 16	64 QFP	–40°C to 105°C
MCF51AG128VLF	MCF51AG128 ColdFire Microcontroller	128 / 16	48 LQFP	–40°C to 105°C
MCF51AG96VLK	MCF51AG96 ColdFire Microcontroller	96 / 16	80 LQFP	–40°C to 105°C
MCF51AG96VLH	MCF51AG96 ColdFire Microcontroller	96 / 16	64 LQFP	–40°C to 105°C
MCF51AG96VQH	MCF51AG96 ColdFire Microcontroller	96 / 16	64 QFP	–40°C to 105°C
MCF51AG96VLF	MCF51AG96 ColdFire Microcontroller	96 / 16	48 LQFP	–40°C to 105°C

4 Package Information

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
64	Quad Flat Package	QFP	QH	840B	98ASB42844B
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

THIS PAGE INTENTIONALLY BLANK