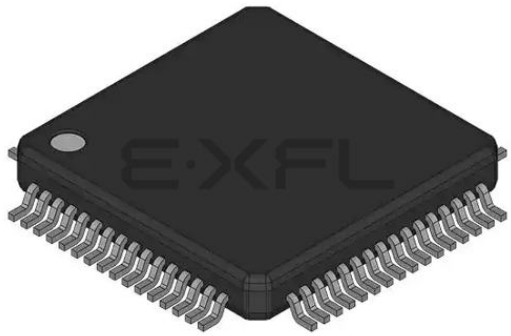

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 19x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag128clh

- System Clock Sources
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Frequency-locked-loop (FLL) controlled by internal or external reference; trimmable internal reference allows 0.2% resolution and 2% deviation (1% across 0 to 70 ºC)
- Peripherals
  - ADC — 24 analog inputs with 12 bits resolution; output formatted in 12-, 10- or 8-bit right-justified format; single or continuous conversion (automatic return to idle after single conversion); interrupt or DMA request when conversion complete; operation in low-power modes for lower noise operation; asynchronous clock source for lower noise operation; selectable asynchronous hardware conversion triggers from RTC, PDB, or iEvent; dual samples based on hardware triggers during ping-pong mode; on-chip temperature sensor
  - PDB — 16-bit of resolution with prescaler; seven possible trigger events input; positive transition of trigger event signal initiates the counter; support continuous trigger or single shot, bypass mode; supports two triggered delay outputs or ORed together; pulsed output could be used for HSCMP windowing signal
  - iEvent — User programmable combinational boolean output using the four selected iEvent input channels for use as interrupt requests, DMA transfer requests, or hardware triggers
  - FTM — Two 6-channel flexible timer/PWM modules with DMA request option; deadtime insertion is available for each complementary channel pair; channels operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs); 16-bit free-running counter; the load of the FTM registers which have write buffer can be synchronized; write protection for critical registers; backwards compatible with TPM
  - TPM — 16-bit free-running or modulo up/down count operation; two channels, each channel may be input capture, output compare, or edge-aligned PWM; one interrupt per channel plus terminal count interrupt
  - CRC — High speed hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial; error detection for all single, double, odd, and most multi-bit errors; programmable initial seed value
  - HSCMP — Two analog comparators with selectable interrupt on rising edge, falling edge, or either edges of comparator output; the positive and negative inputs of the comparator are both driven from 4-to-1 muxes; programmable voltage reference from two internal DACs; support DMA transfer
  - IIC — Compatible with IIC bus standard and SMBus version 2 features; up to 100 kbps with maximum bus loading; multi-master operation; software programmable for one of 64 different serial clock frequencies; programmable slave address and glitch input filter; interrupt driven byte-by-byte data transfer; arbitration lost interrupt with automatic mode switching from master to slave; calling address identification interrupt; bus busy detection; broadcast and 10-bit address extension; address matching causes wake-up when MCU is in Stop3 mode; DMA support
  - SCI — Two serial communications interface modules with optional 13-bit break; full-duplex, standard non-return-to-zero (NRZ) format; double-buffered transmitter and receiver with separate enables; 13-bit baud rate selection with /32 fractional divide; interrupt-driven or polled operation; hardware parity generation and checking; programmable 8-bit or 9-bit character length; receiver wakeup by idle-line or address-mark; address match feature in receiver to reduce address-mark wakeup ISR overhead; 1/16 bit-time noise detection; DMA transmission for both transmit and receive
  - SPI — Two serial peripheral interfaces with full-duplex or single-wire bidirectional option; double-buffered transmitter and receiver; master or slave mode operation; selectable MSB-first or LSB-first shifting; 8-bit or 16-bit data modes; programmable transmit bit rate; receive data buffer hardware match feature; DMA transmission for transmit and receive
- Input/Output
  - Up to 69 GPIOs and one Input-only pin
  - Interrupt or DMA request with selectable polarity on all input pins
  - Programmable glitch filter, hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
  - Independent pin value register to read logic level on digital pin
  - Up to 16 rapid general purpose I/O (RGPIO) pins connected to the processor’s local 32-bit platform bus with set, clear, and faster toggle functionality

Table 1. MCF51AG128 Series Device Comparison (continued)

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
TPM3 (timer pulse-width modulator) channels	2					
Debug Visibility Bus	Yes	No	No	Yes	No	No

[1] Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

[2] Some pins of FTMx might not be bonded on small package, therefore these channels could be used as soft timer only.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AG128 series pins and modules.

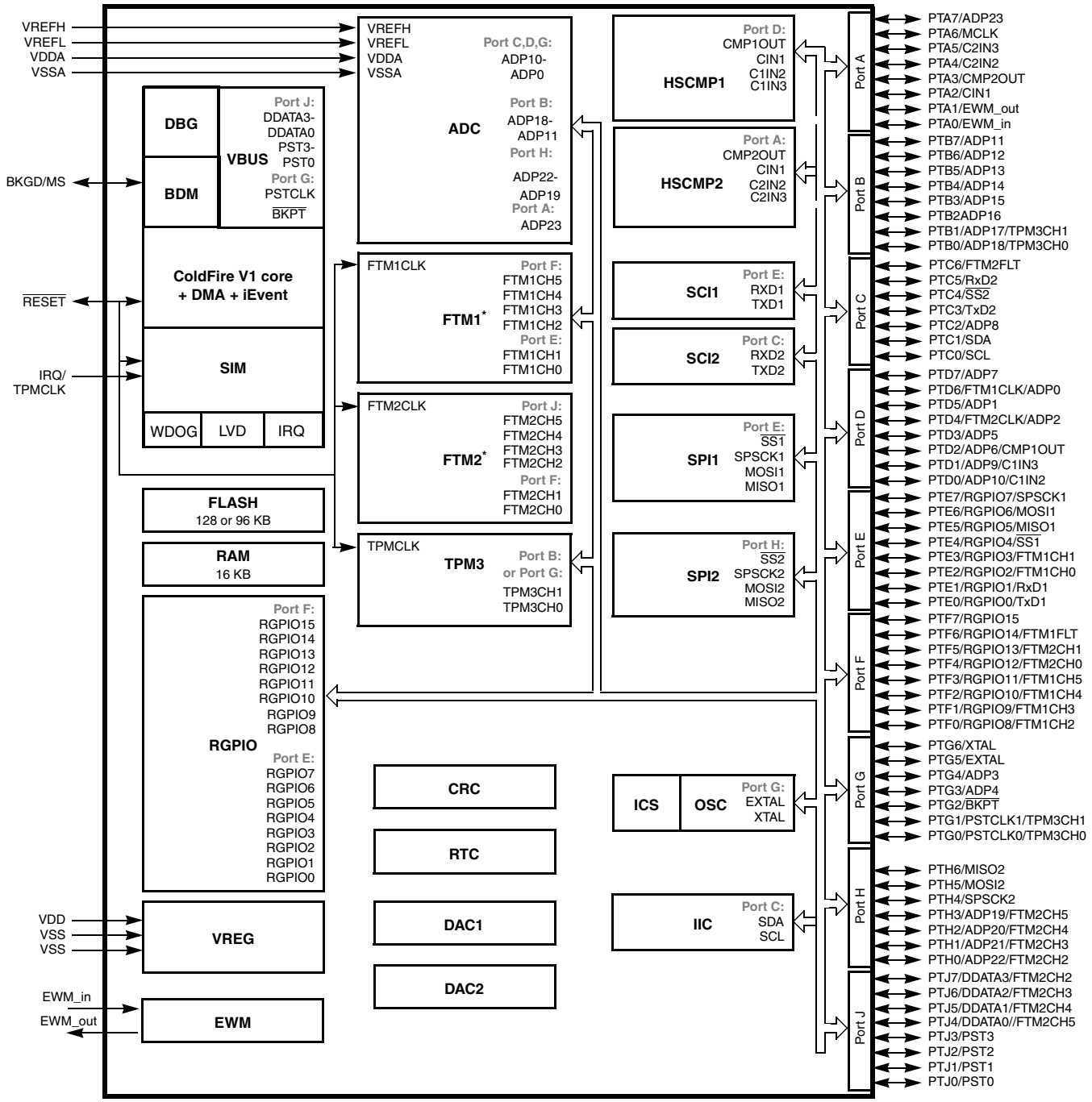


Figure 1. MCF51AG128 Series MCUs Block Diagram

Table 2. MCF51AG128 Series Functional Units (continued)

Functional Unit	Function
WDOG (Watchdog timer)	keeps a watch on the system functioning and resets it in case of its failure
RTC (Real Time Counter)	Provides a constant time-base with optional interrupt

Figure 4 shows the pinout of the 48-pin LQFP.

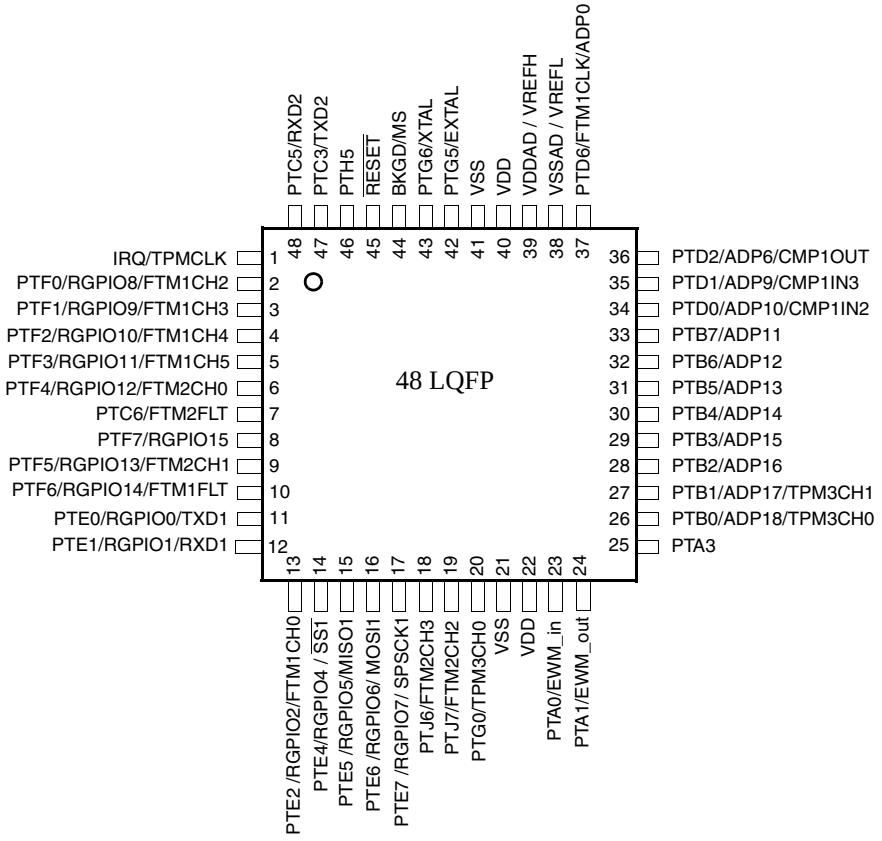


Figure 4. 48-Pin LQFP

Table 5. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 6. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to 105	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s	θ_{JA}	56	°C/W
	2s2p		45	
64-pin QFP				
	1s		54	
	2s2p		41	
64-pin LQFP				
	1s		67	
	2s2p		49	
48-pin LQFP				
	1s		69	
	2s2p		51	

Table 9. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
6	P	Input high voltage; all digital inputs	V_{IH}	$0.65 \times V_{DD}$	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	
8	D	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[3] Internal pullup resistorsPTC0 and PTC1	R_{PU}	20 10	45 22	65 32	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
17	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
18	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
19	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
20	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
21	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
22	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV
23	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
24	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	 0 0	 — —	 2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		 0 0	 — —	 25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

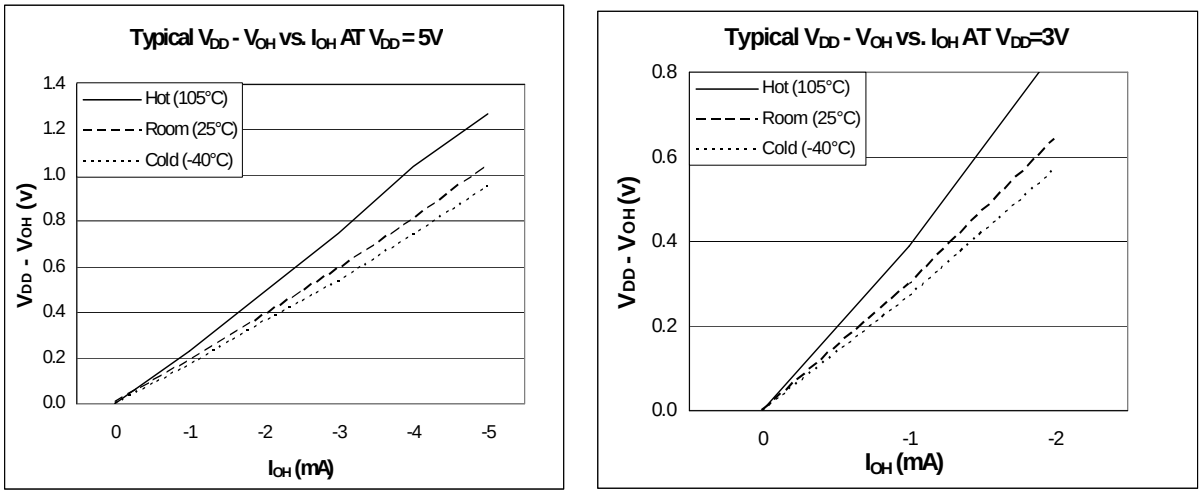


Figure 5. Typical I_{OH} vs. $V_{DD} – V_{OH}$ (Low Drive,PTxDSn = 0)

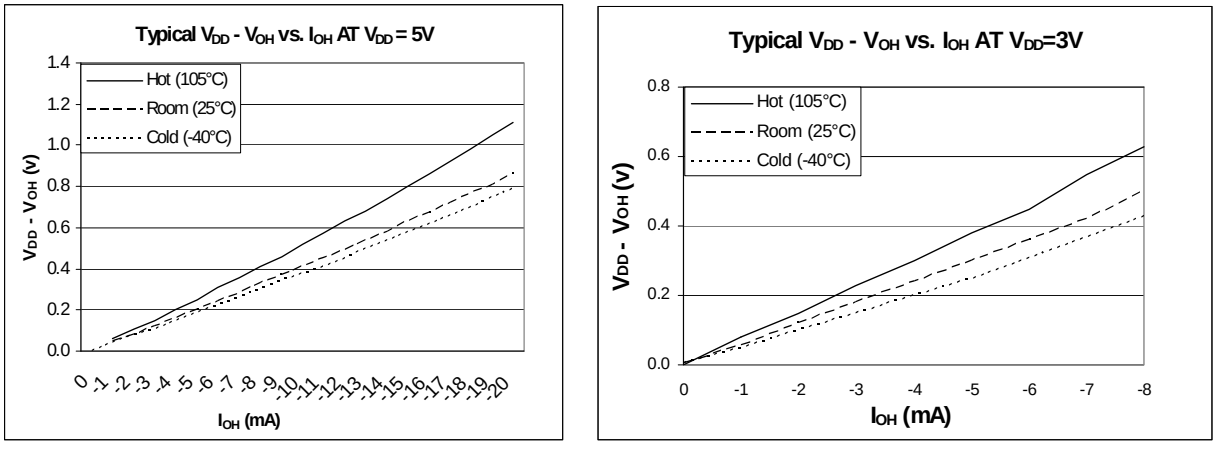


Figure 6. Typical I_{OH} vs. $V_{DD} – V_{OH}$ (High Drive, PTxDSn = 1)

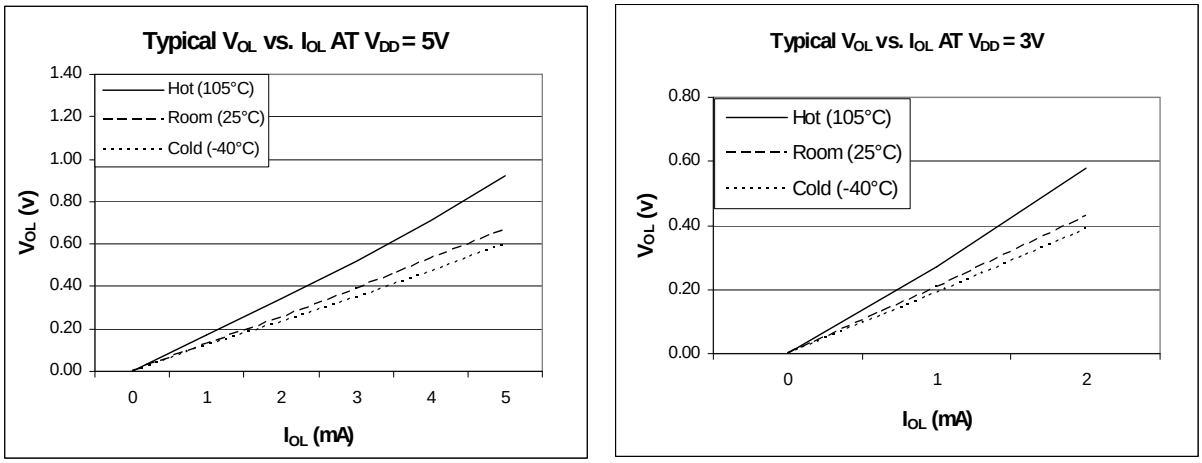


Figure 7. Typical I_{OL} vs. V_{OL} (Low Drive, PTxDSn = 0)

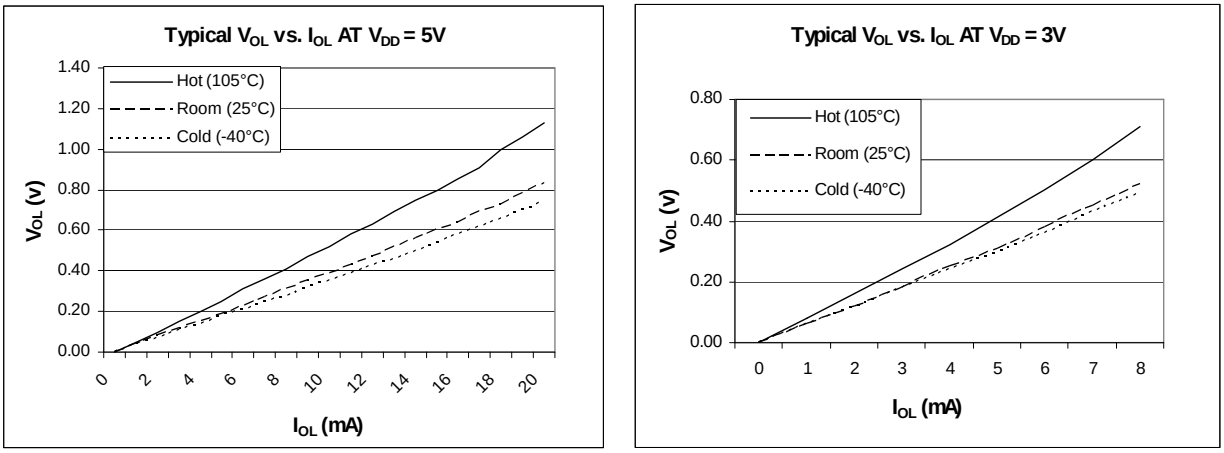


Figure 8. Typical I_{OL} vs. V_{OL} (High Drive, PTxDSn = 1)

Table 12. 5V 12-bit ADC Operating Conditions (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
3	D	Ref Voltage High	—	V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	—
4	D	Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSA}	V_{SSA}	V	—
5	D	Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
6	C	Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
7	C	Input Resistance	—	R_{ADIN}	—	3	5	kΩ	—
8	C	Analog Source Resistance	12 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	C		10 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		 — —	 — —	 5 10		
	C		8 bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	D		Low Power (ADLPC = 1)		0.4	—	4.0		—

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

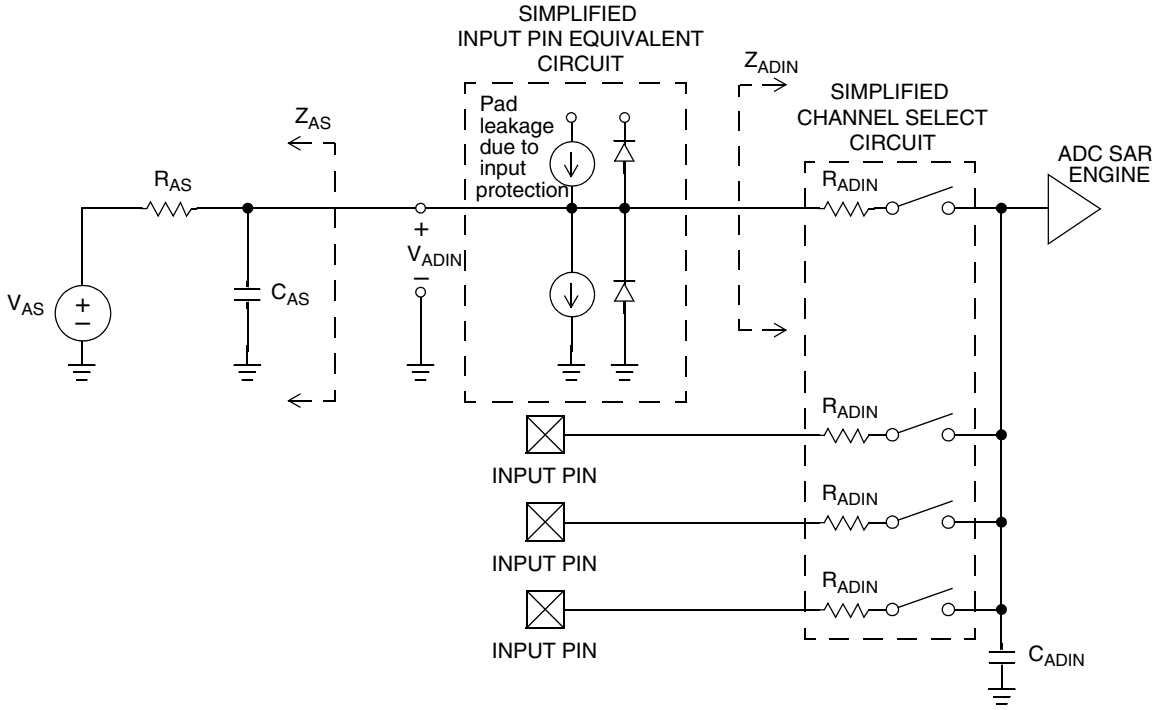


Figure 10. ADC Input Impedance Equivalency Diagram

Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	181	—	μA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	334	—	μA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	385	—	μA	—
4	D	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.717	1	mA	—
5	T	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.065	1	μA	—

Table 13. 5 V 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC = 1)		1.25	2	3.3		
7	P	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long Sample (ADLSMP = 1)		—	40	—		
8	T	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long Sample (ADLSMP = 1)		—	23.5	—		
9	T	Total Unadjusted Error	12 bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	P		10 bit mode		—	±1	±2.5		
	T		8 bit mode		—	±0.5	±1.0		
10	T	Differential Non-Linearity	12 bit mode	DNL	—	±1.75	—	LSB[2]	—
	P		10 bit mode[3]		—	±0.5	±1.0		
	T		8 bit mode[5]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12 bit mode	INL	—	±1.5	—	LSB[2]	—
	P		10 bit mode		—	±0.5	±1.0		
	T		8 bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12 bit mode	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	P		10 bit mode		—	±0.5	±1.5		
	T		8 bit mode		—	±0.5	±0.5		
13	T	Full-Scale Error	12 bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10 bit mode		—	±0.5	±1		
	T		8 bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12 bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10 bit mode		—	—	±0.5		
			8 bit mode		—	—	±0.5		
15	D	Input Leakage Error	12 bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10 bit mode		—	±0.2	±2.5		
			8 bit mode		—	±0.1	±1		

Table 15. ICS Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
10	D	FLL acquisition time [3]	$t_{fll\_acquire}$	—	—	1	ms
11	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
12	D	Loss of external clock minimum freq. (RANGE = 0) • ext. clock freq: above $(3/5)f_{int}$, never reset • ext. clock freq: between $(2/5)f_{int}$ and $(3/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(2/5)f_{int}$, always reset	f_{loc_low}	$(3/5) \times f_{int}$	—	—	kHz
13	D	Loss of external clock minimum freq. (RANGE = 1) • ext. clock freq: above $(16/5)f_{int}$, never reset • ext. clock freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(15/5)f_{int}$, always reset	f_{loc_high}	$(16/5) \times f_{int}$	—	—	kHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry by V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

3 Ordering Information

This section contains ordering information for MCF51AG128 devices.

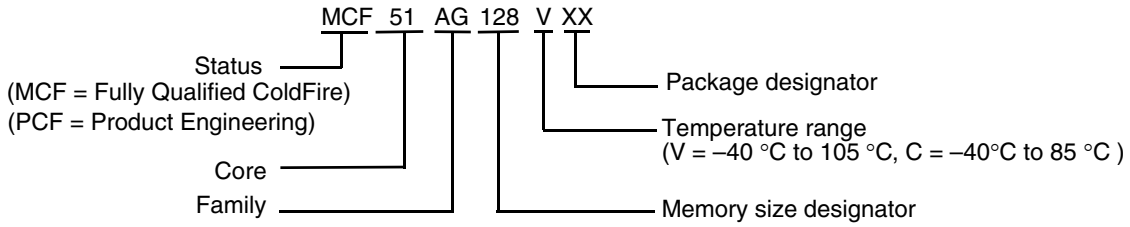


Table 20. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51AG128VLK	MCF51AG128 ColdFire Microcontroller	128 / 16	80 LQFP	–40°C to 105°C
MCF51AG128VLH	MCF51AG128 ColdFire Microcontroller	128 / 16	64 LQFP	–40°C to 105°C
MCF51AG128VQH	MCF51AG128 ColdFire Microcontroller	128 / 16	64 QFP	–40°C to 105°C
MCF51AG128VLF	MCF51AG128 ColdFire Microcontroller	128 / 16	48 LQFP	–40°C to 105°C
MCF51AG96VLK	MCF51AG96 ColdFire Microcontroller	96 / 16	80 LQFP	–40°C to 105°C
MCF51AG96VLH	MCF51AG96 ColdFire Microcontroller	96 / 16	64 LQFP	–40°C to 105°C
MCF51AG96VQH	MCF51AG96 ColdFire Microcontroller	96 / 16	64 QFP	–40°C to 105°C
MCF51AG96VLF	MCF51AG96 ColdFire Microcontroller	96 / 16	48 LQFP	–40°C to 105°C

4 Package Information

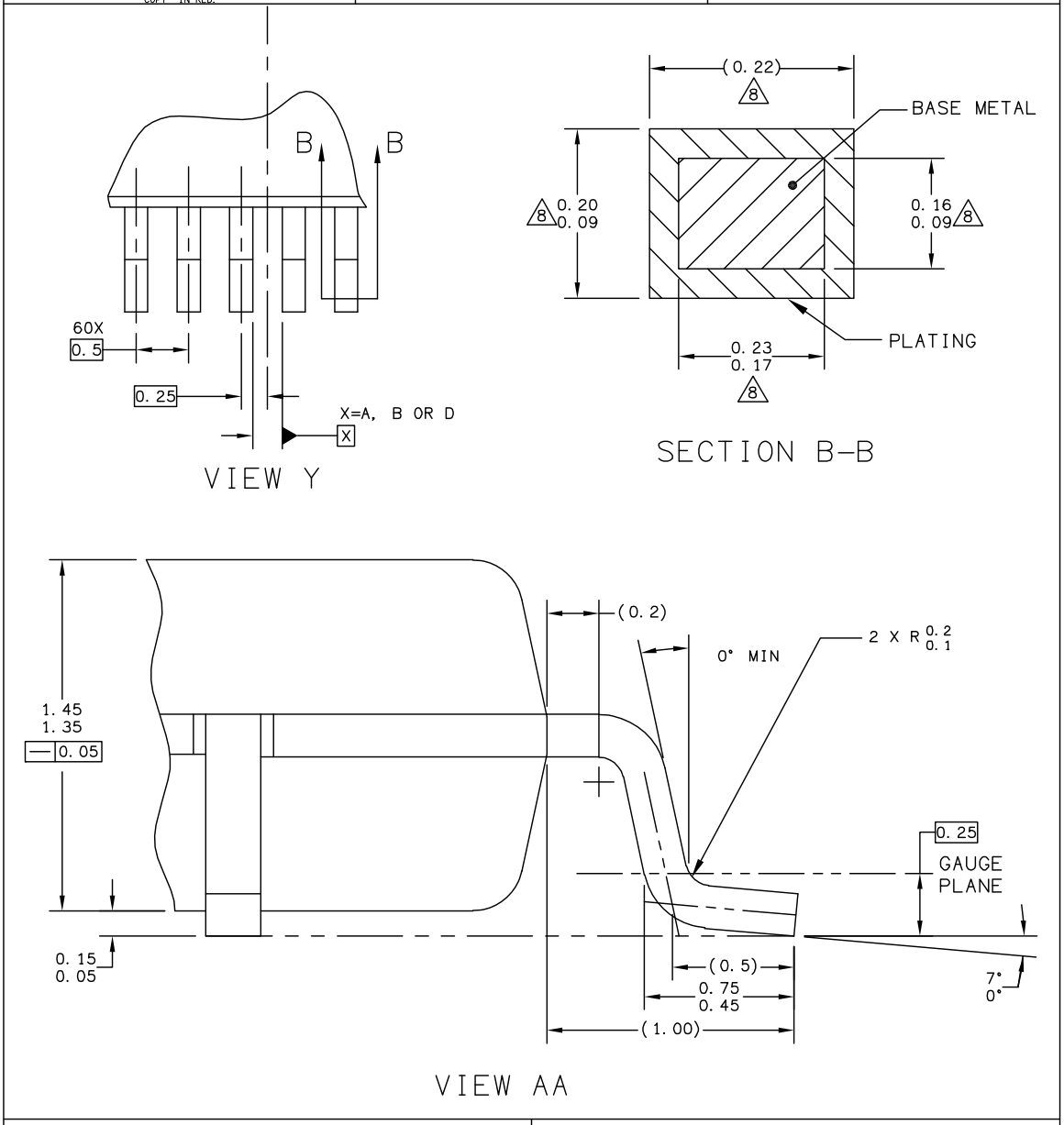
Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
64	Quad Flat Package	QFP	QH	840B	98ASB42844B
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

5 Mechanical Outline Drawings

5.1 80-pin LQFP Package

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E



TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02	
	STANDARD: JEDEC MS-026 BCD	
	PACKAGE CODE: 8426	SHEET: 2

5.4 48-pin LQFP Package

6 Revision History

Table 22. Revision History

Rev. No.	Date	Description
1	11/2008	Initial Draft Release.
2	4/2009	Internal Release.
3	5/2009	Alpha Customer Release.
4	12/2009	• Added 48-pin LQFP information; • Updated Section 2.5/17 and 2.6/21. • Provided the supply current in Section 2.7/23, and setup delay in Section 2.8/23.
5	6/2010	• Updated Table 10. • Added Figure 9. • Corrected pin names of PTG6 and PTG5 in 48-pin LQFP. • Standardized Generation 2008 Watchdog to Watchdog. • In Table 9, updated Output high/low voltage — Low Drive (PTxDSn = 0) 3 V, I_{Load} value.

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Document Number: MCF51AG128
Rev. 5
6/2010

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