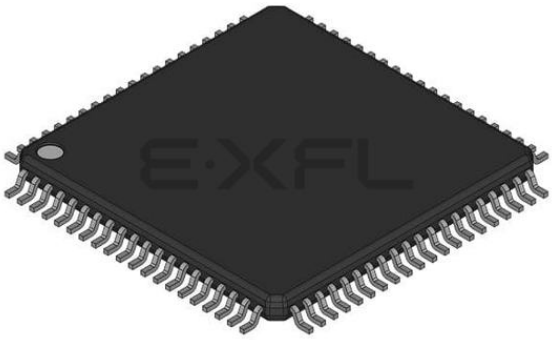

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	69
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag128vlk

- System Clock Sources
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Frequency-locked-loop (FLL) controlled by internal or external reference; trimmable internal reference allows 0.2% resolution and 2% deviation (1% across 0 to 70 ºC)
- Peripherals
  - ADC — 24 analog inputs with 12 bits resolution; output formatted in 12-, 10- or 8-bit right-justified format; single or continuous conversion (automatic return to idle after single conversion); interrupt or DMA request when conversion complete; operation in low-power modes for lower noise operation; asynchronous clock source for lower noise operation; selectable asynchronous hardware conversion triggers from RTC, PDB, or iEvent; dual samples based on hardware triggers during ping-pong mode; on-chip temperature sensor
  - PDB — 16-bit of resolution with prescaler; seven possible trigger events input; positive transition of trigger event signal initiates the counter; support continuous trigger or single shot, bypass mode; supports two triggered delay outputs or ORed together; pulsed output could be used for HSCMP windowing signal
  - iEvent — User programmable combinational boolean output using the four selected iEvent input channels for use as interrupt requests, DMA transfer requests, or hardware triggers
  - FTM — Two 6-channel flexible timer/PWM modules with DMA request option; deadtime insertion is available for each complementary channel pair; channels operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs); 16-bit free-running counter; the load of the FTM registers which have write buffer can be synchronized; write protection for critical registers; backwards compatible with TPM
  - TPM — 16-bit free-running or modulo up/down count operation; two channels, each channel may be input capture, output compare, or edge-aligned PWM; one interrupt per channel plus terminal count interrupt
  - CRC — High speed hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial; error detection for all single, double, odd, and most multi-bit errors; programmable initial seed value
  - HSCMP — Two analog comparators with selectable interrupt on rising edge, falling edge, or either edges of comparator output; the positive and negative inputs of the comparator are both driven from 4-to-1 muxes; programmable voltage reference from two internal DACs; support DMA transfer
  - IIC — Compatible with IIC bus standard and SMBus version 2 features; up to 100 kbps with maximum bus loading; multi-master operation; software programmable for one of 64 different serial clock frequencies; programmable slave address and glitch input filter; interrupt driven byte-by-byte data transfer; arbitration lost interrupt with automatic mode switching from master to slave; calling address identification interrupt; bus busy detection; broadcast and 10-bit address extension; address matching causes wake-up when MCU is in Stop3 mode; DMA support
  - SCI — Two serial communications interface modules with optional 13-bit break; full-duplex, standard non-return-to-zero (NRZ) format; double-buffered transmitter and receiver with separate enables; 13-bit baud rate selection with /32 fractional divide; interrupt-driven or polled operation; hardware parity generation and checking; programmable 8-bit or 9-bit character length; receiver wakeup by idle-line or address-mark; address match feature in receiver to reduce address-mark wakeup ISR overhead; 1/16 bit-time noise detection; DMA transmission for both transmit and receive
  - SPI — Two serial peripheral interfaces with full-duplex or single-wire bidirectional option; double-buffered transmitter and receiver; master or slave mode operation; selectable MSB-first or LSB-first shifting; 8-bit or 16-bit data modes; programmable transmit bit rate; receive data buffer hardware match feature; DMA transmission for transmit and receive
- Input/Output
  - Up to 69 GPIOs and one Input-only pin
  - Interrupt or DMA request with selectable polarity on all input pins
  - Programmable glitch filter, hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
  - Independent pin value register to read logic level on digital pin
  - Up to 16 rapid general purpose I/O (RGPIO) pins connected to the processor’s local 32-bit platform bus with set, clear, and faster toggle functionality

1 MCF51AG128 Family Configurations

1.1 Device Comparison

The following table compares the various device derivatives available within the MCF51AG128 series MCUs.

Table 1. MCF51AG128 Series Device Comparison

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
Flash memory size (KB)	128			96		
RAM size (KB)	16					
ColdFire V1 core with BDM (background debug module)	Yes					
HSCMP (analog comparator)	2	2	1	2	2	1
ADC (analog-to-digital converter) channels (12-bit)	24	19	12	24	19	12
CRC (cyclic redundancy check)	Yes					
DAC	2	2	1	2	2	1
DMA controller	4-ch					
iEvent (intelligent Event module)	Yes					
EWM (External Watchdog Monitor)	Yes					
WDOG (Watchdog timer)	Yes					
RTC	Yes					
DBG (debug module)	Yes					
IIC (inter-integrated circuit)	1	1	No	1	1	No
IRQ (interrupt request input)	Yes					
INTC (interrupt controller)	Yes					
LVD (low-voltage detector)	Yes					
ICS (internal clock source)	Yes					
OSC (crystal oscillator)	Yes					
Port I/O[1]	69	53	39	69	53	39
RGPIO (rapid general-purpose I/O)	16	16	15	16	16	15
SCI (serial communications interface)	2					
SPI1 (serial peripheral interface)	Yes					
SPI2 (serial peripheral interface)	Yes	No	No	Yes	No	No
FTM1 (flexible timer module) channels	6[2]					
FTM2 channels	6[2]					

Table 1. MCF51AG128 Series Device Comparison (continued)

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
TPM3 (timer pulse-width modulator) channels	2					
Debug Visibility Bus	Yes	No	No	Yes	No	No

[1] Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

[2] Some pins of FTMx might not be bonded on small package, therefore these channels could be used as soft timer only.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AG128 series pins and modules.

Table 3. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest		
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**
41	33	—	PTA7	ADP23	
42	—	—	PTH0	ADP22	FTM2CH2
43	—	—	PTH1	ADP21	FTM2CH3
44	—	—	PTH2	ADP20	FTM2CH4
45	—	—	PTH3	ADP19	FTM2CH5
46	34	26	PTB0	ADP18	TPM3CH0
47	35	27	PTB1	ADP17	TPM3CH1
48	36	28	PTB2	ADP16	
49	37	29	PTB3	ADP15	
50	38	30	PTB4	ADP14	
51	39	31	PTB5	ADP13	
52	40	32	PTB6	ADP12	
53	41	33	PTB7	ADP11	
54	42	34	PTD0	ADP10	C1IN2
55	43	35	PTD1	ADP9	C1IN3
56	44	—	PTC2	ADP8	
57	45	—	PTD7	ADP7	
58	46	36	PTD2	ADP6	CMP1OUT
59	47	—	PTD3	ADP5	
60	48	—	PTG3	ADP4	
61	—	—	PTG4	ADP3	
62	49	—	PTD4	FTM2CLK	ADP2
63	50	—	PTD5	ADP1	
64	51	37	PTD6	FTM1CLK	ADP0
65	—	—	PTC4	$\overline{SS2}$	
66	52	38	V_{SSA}		
67	53	38	V_{REFL}		
68	54	39	V_{REFH}		
69	55	39	V_{DDA}		
70	56	40	V_{DD}		
71	57	41	V_{SS}		
72	58	42	PTG5	EXTAL	
73	59	43	PTG6	XTAL	
74	60	44	BKGD	MS	
75	61	45	$\overline{RESET}$		
76	—	—	PTH4	SPSCK2	
77	62	46	PTH5	MOSI2	
78	—	—	PTH6	MISO2	
79	63	47	PTC3	TxD2	
80	64	48	PTC5	RxD2	

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—

Table 7. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	±500	—	V
3	Latch-up Current at T_A = 85°C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –5 mA 3 V, I_{Load} = –1.5 mA 5V, I_{Load} = –3 mA, PTC0 and PTC1 3V, I_{Load} = –1.5 mA, PTC0 and PTC1	V_{OH}	 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.4 V_{DD} – 0.4	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –20 mA 3 V, I_{Load} = –8 mA 5V, I_{Load} = –12 mA, PTC0 and PTC1 3V, I_{Load} = –8 mA, PTC0 and PTC1		 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.4 V_{DD} – 0.4	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 1.5 mA 5V, I_{Load} = 3 mA, PTC0 and PTC1 3V, I_{Load} = 1.5 mA, PTC0 and PTC1	V_{OL}	 — — — —	 — — — —	 1.5 0.8 0.4 0.4	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 20 mA 3 V, I_{Load} = 8 mA 5V, I_{Load} = 12 mA, PTC0 and PTC1 3V, I_{Load} = 8 mA, PTC0 and PTC1		 — — — —	 — — — —	 1.5 0.8 0.4 0.4	
4	C	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	C	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	 — —	 — —	 100 60	mA

Table 9. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
6	P	Input high voltage; all digital inputs	V_{IH}	$0.65 \times V_{DD}$	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	
8	D	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[3] Internal pullup resistorsPTC0 and PTC1	R_{PU}	20 10	45 22	65 32	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
17	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
18	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
19	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
20	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
21	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
22	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV
23	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
24	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	 0 0	 — —	 2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		 0 0	 — —	 25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

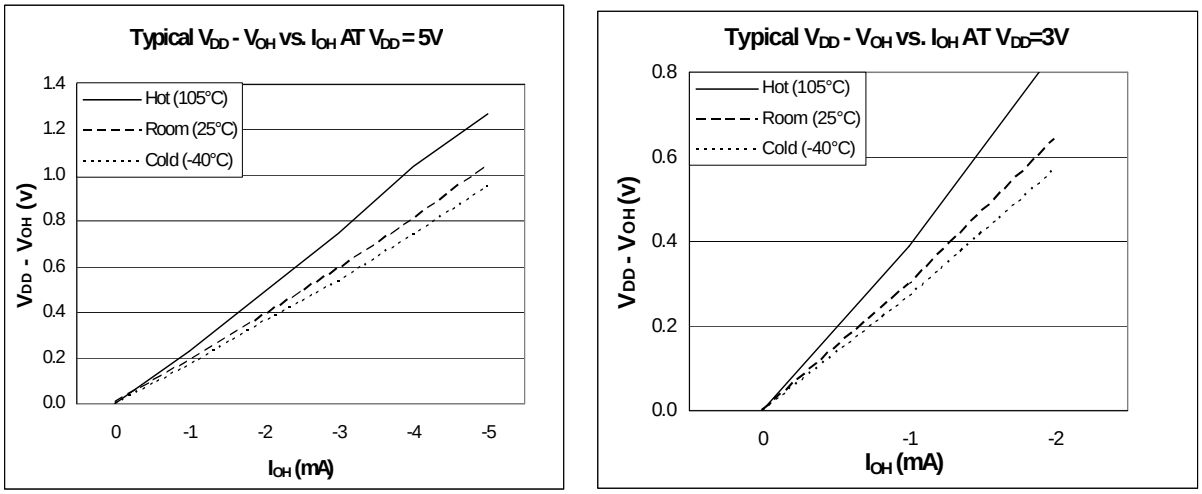


Figure 5. Typical I_{OH} vs. $V_{DD} – V_{OH}$ (Low Drive,PTxDSn = 0)

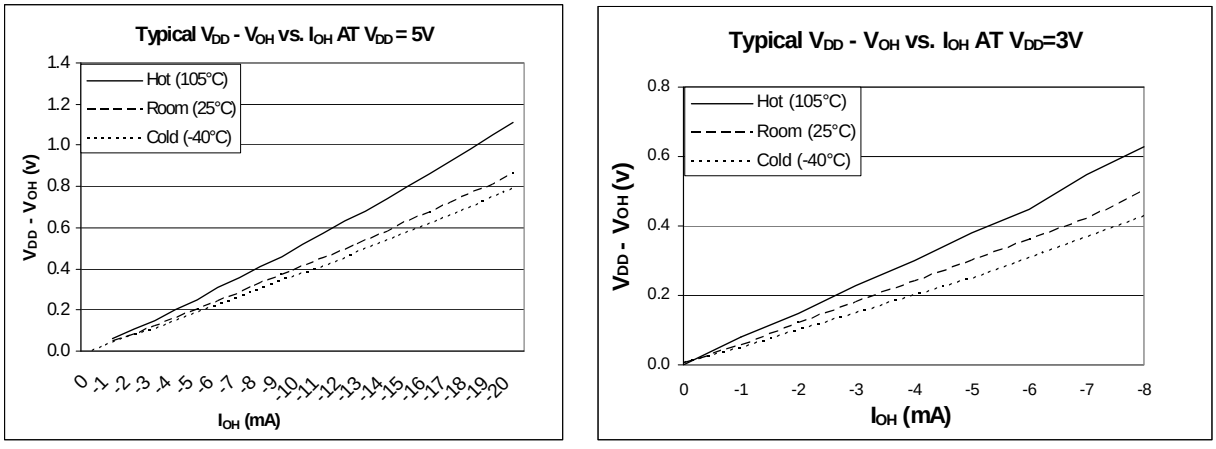


Figure 6. Typical I_{OH} vs. $V_{DD} – V_{OH}$ (High Drive, PTxDSn = 1)

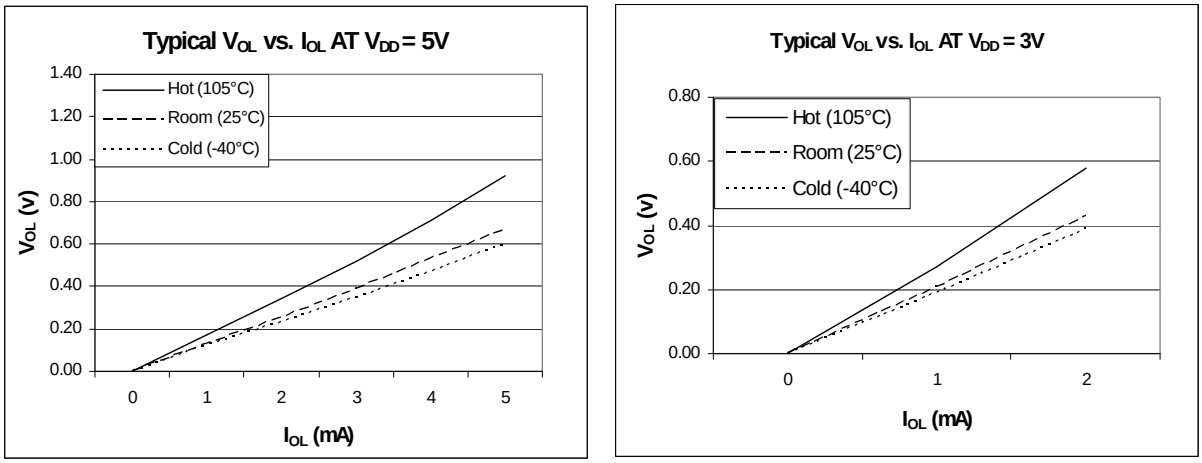


Figure 7. Typical I_{OL} vs. V_{OL} (Low Drive, PTxDSn = 0)

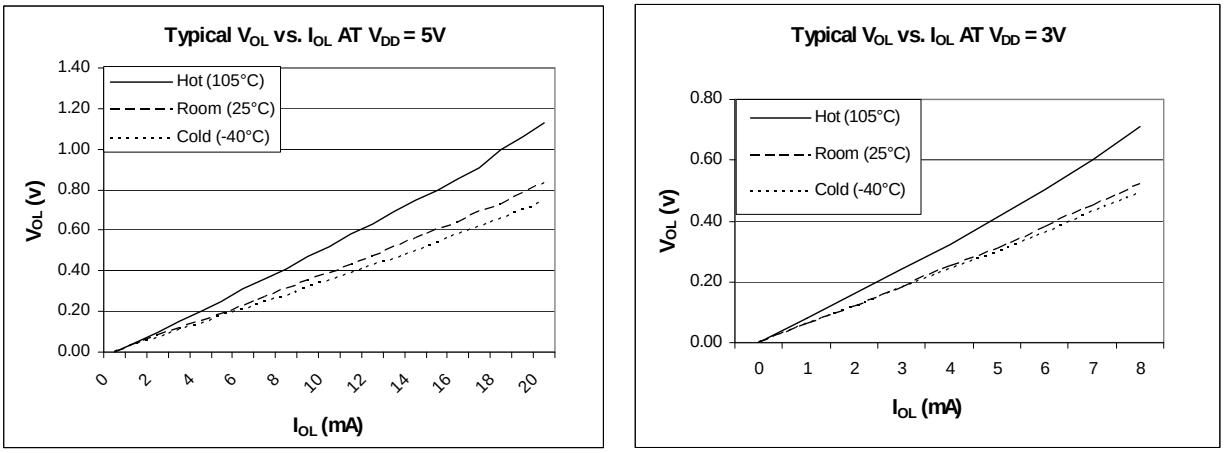


Figure 8. Typical I_{OL} vs. V_{OL} (High Drive, PTxDSn = 1)

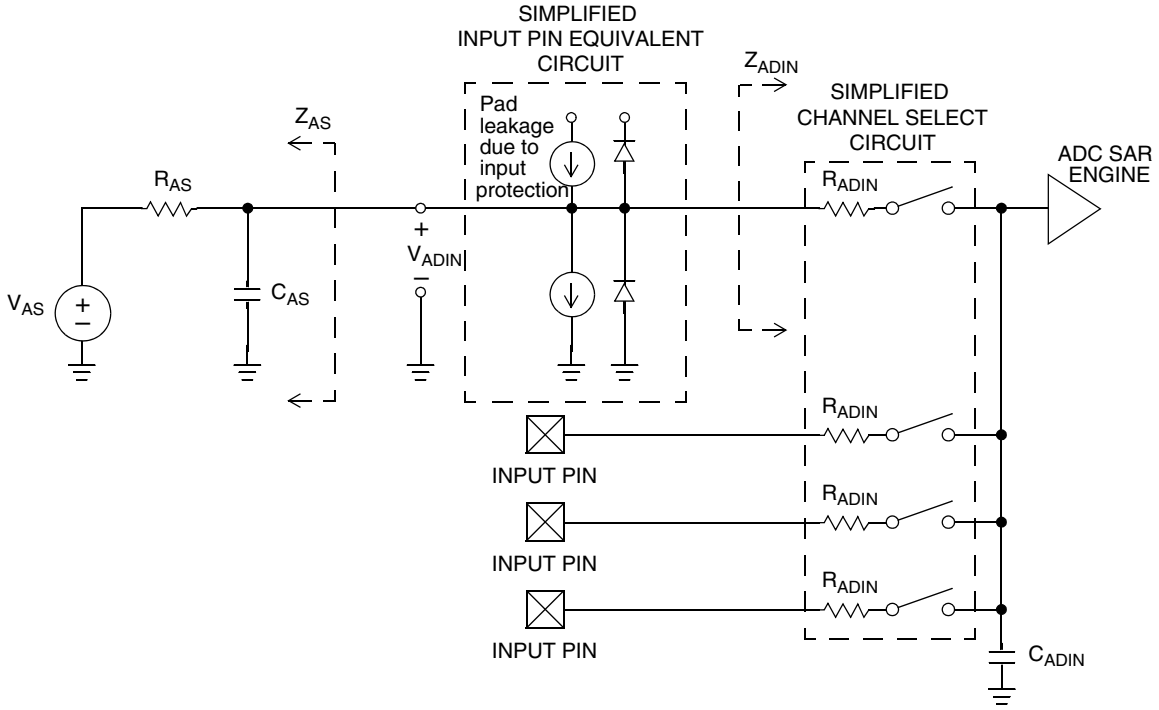


Figure 10. ADC Input Impedance Equivalency Diagram

Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	T	Supply Current ADLPC = 1 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	181	—	μA	—
2	T	Supply Current ADLPC = 1 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	334	—	μA	—
3	T	Supply Current ADLPC = 0 ADLSMP = 1 ADCO = 1	—	I_{DDAD}	—	385	—	μA	—
4	D	Supply Current ADLPC = 0 ADLSMP = 0 ADCO = 1	—	I_{DDAD}	—	0.717	1	mA	—
5	T	Supply Current	Stop, Reset, Module Off	I_{DDAD}	—	0.065	1	μA	—

Table 13. 5 V 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
16	D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	—
17	D	Temp Sensor Slope	–40 °C — 25 °C	m	—	3.266	—	mV/°C	—
			25 °C — 85 °C		—	3.638	—		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.10 External Oscillator (XOSC) Characteristics

Table 14. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

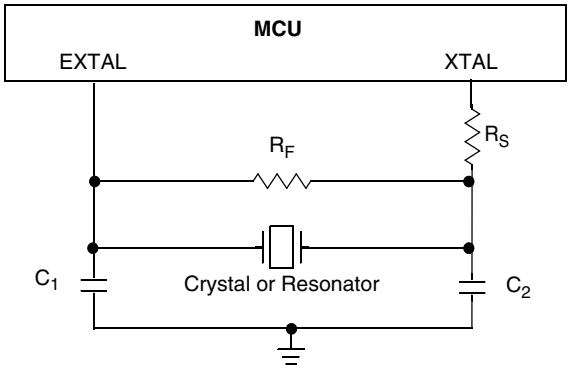
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 16 16 8	 kHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		10 1	—	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[3]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 1500 2000 3 7	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode [2] FBE mode[2] FBELP mode	f_{extal}	 0.03125 0 0	 — — —	 50.33 50.33 50.33	MHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal



2.11 ICS Specifications

Table 15. ICS Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range - untrimmed [2]	Low range (DRS = 00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	C		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS = 01)		—	33.69	—	
	P		High range (DRS = 10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over full voltage and temperature range		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 –70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$

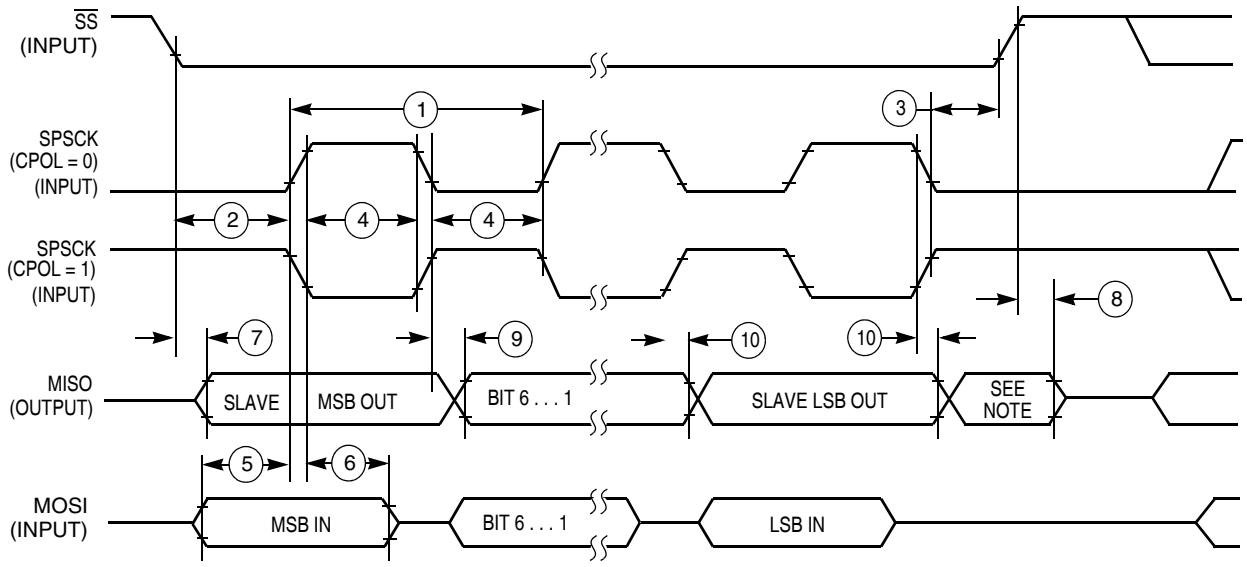
2.12.3 SPI Characteristics

Table 18 and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 18. SPI Timing Characteristics

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	30 30	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	10 10	— —	ns ns
7	D	Slave access time	t_a	—	—	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	—	t_{cyc}
9	D	Data valid time (maximum delay after SPCLK edge to Data output) Master Slave	t_V[1]	 — —	 25 70	 ns ns
10	D	Data hold time (minimum delay after SPCLK edge to Data output) Master Slave	t_{HO}[1]	 10 10	 — —	 ns ns

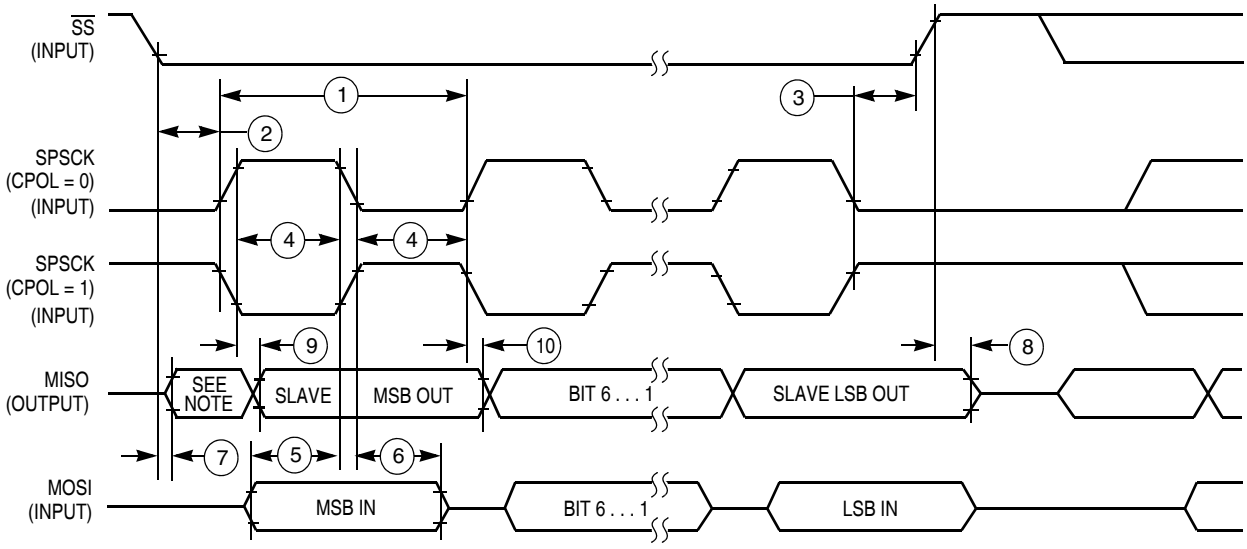
[1] SPI Output Load = 30 pf



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

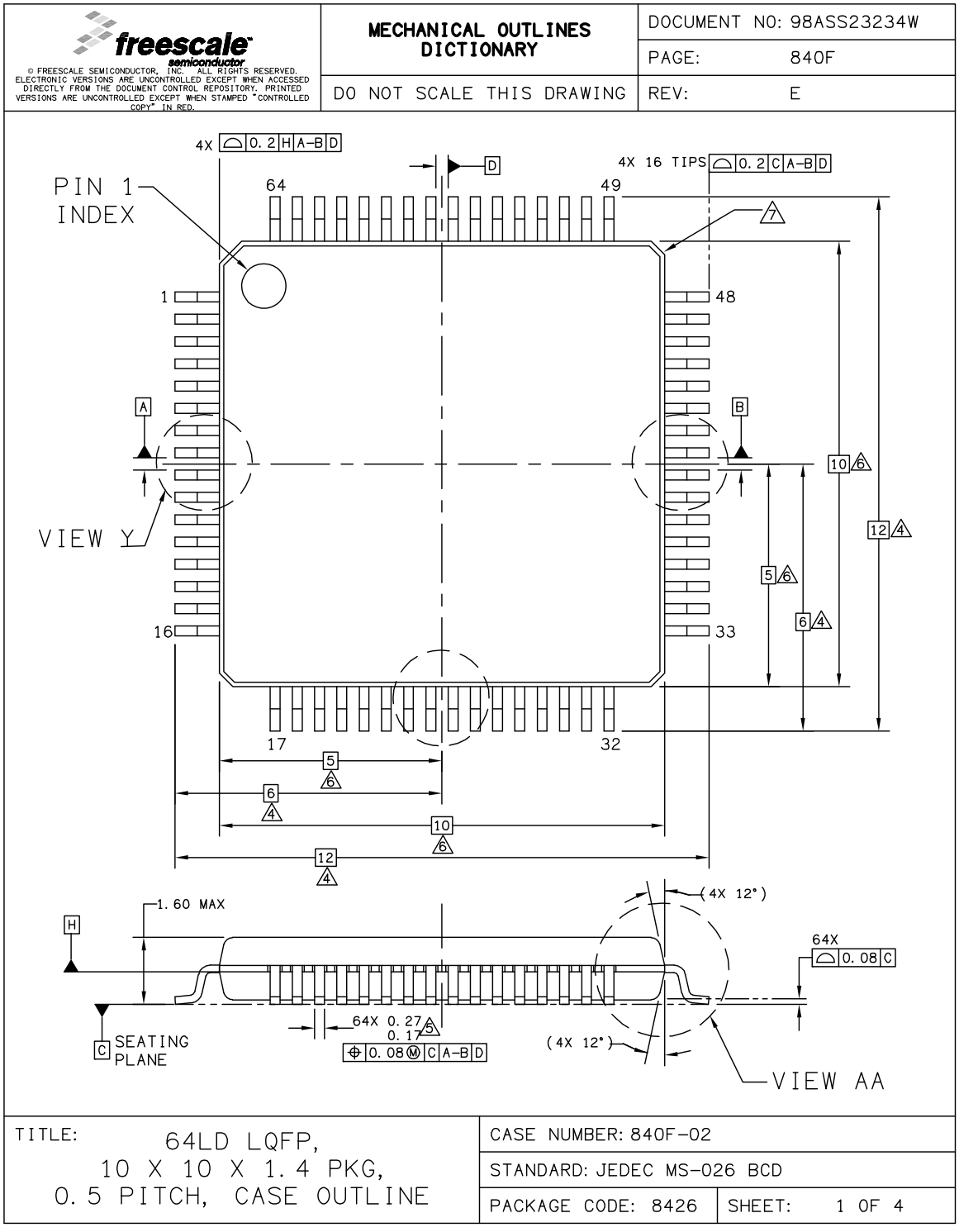
Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

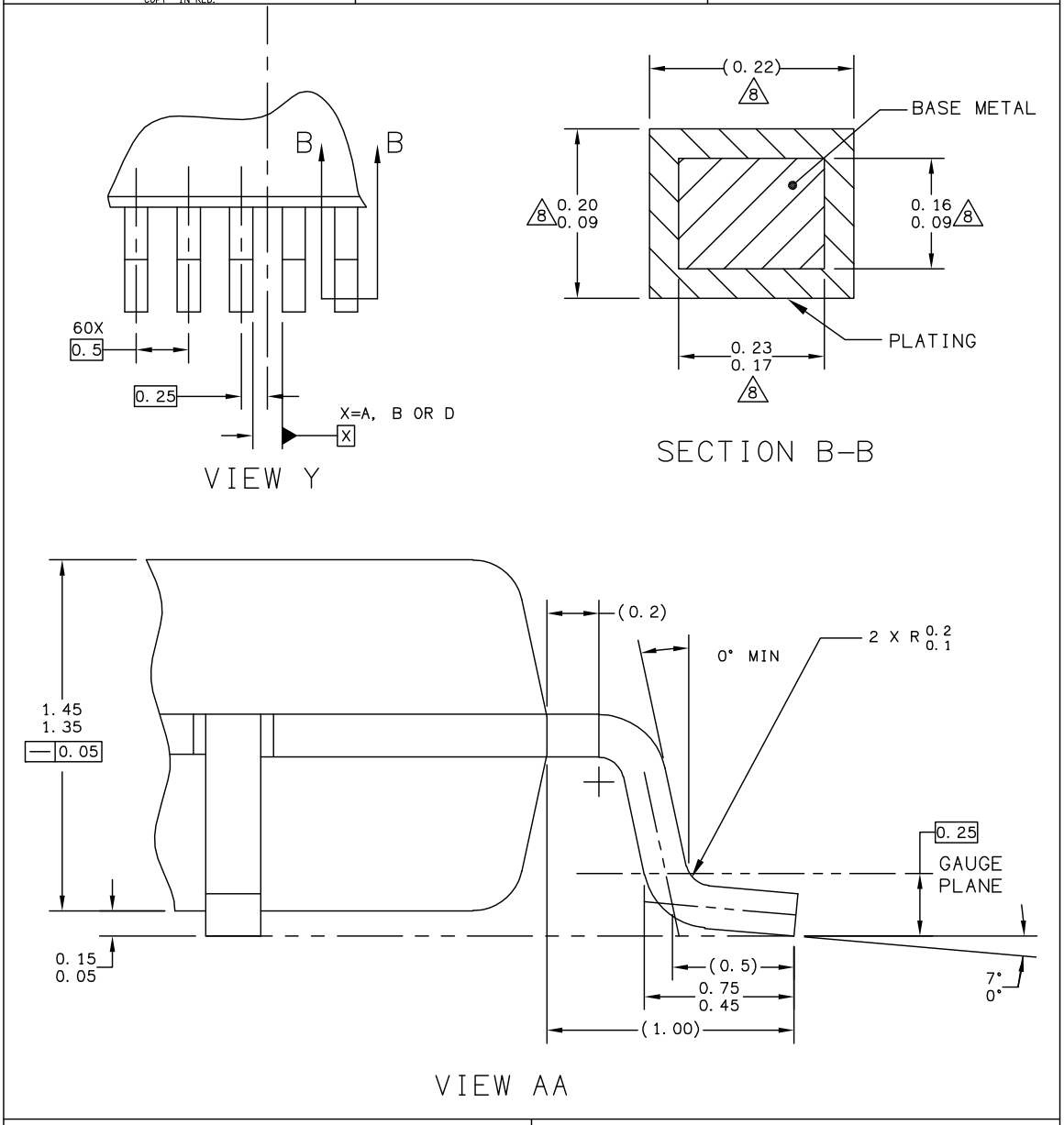
This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see *MCF51AG128 Reference Manual*.

5.2 64-pin LQFP Package

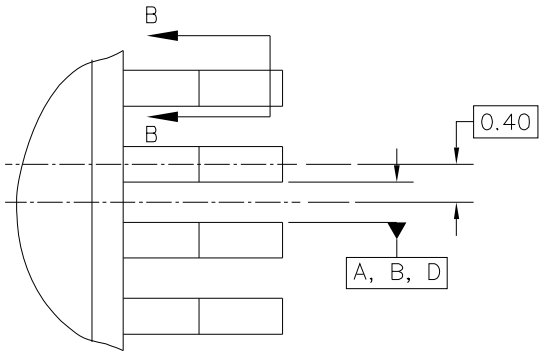


freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

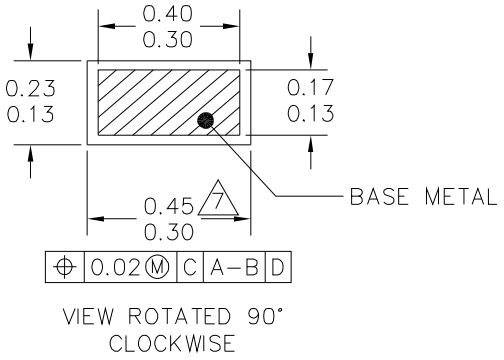


TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02	
	STANDARD: JEDEC MS-026 BCD	
	PACKAGE CODE: 8426	SHEET: 2

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
	PAGE: 840B
DO NOT SCALE THIS DRAWING	REV: B

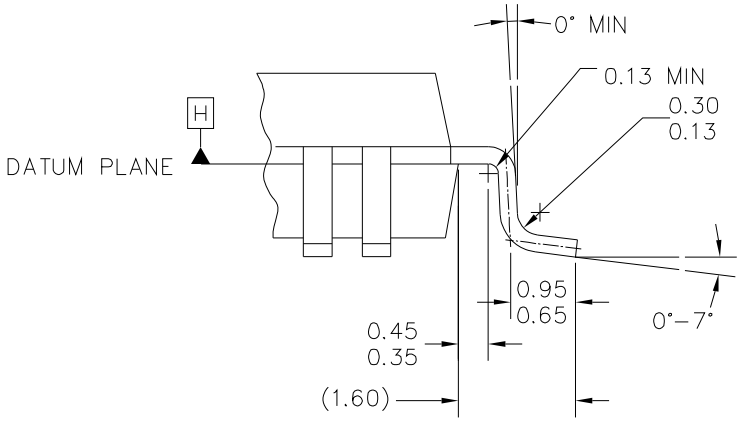


DETAIL "A"



VIEW ROTATED 90° CLOCKWISE

SECTION B–B



DETAIL "C"

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 2 OF 4

freescale semiconductor 	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A−B AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

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