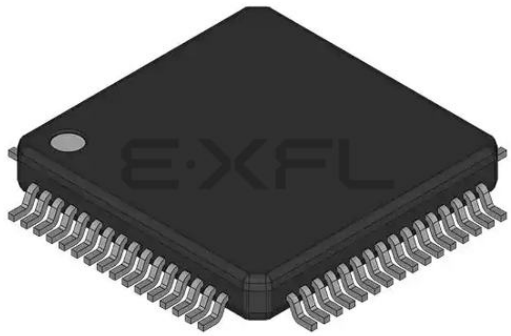

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	53
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 19x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag128vqh

- System Clock Sources
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Frequency-locked-loop (FLL) controlled by internal or external reference; trimmable internal reference allows 0.2% resolution and 2% deviation (1% across 0 to 70 ºC)
- Peripherals
  - ADC — 24 analog inputs with 12 bits resolution; output formatted in 12-, 10- or 8-bit right-justified format; single or continuous conversion (automatic return to idle after single conversion); interrupt or DMA request when conversion complete; operation in low-power modes for lower noise operation; asynchronous clock source for lower noise operation; selectable asynchronous hardware conversion triggers from RTC, PDB, or iEvent; dual samples based on hardware triggers during ping-pong mode; on-chip temperature sensor
  - PDB — 16-bit of resolution with prescaler; seven possible trigger events input; positive transition of trigger event signal initiates the counter; support continuous trigger or single shot, bypass mode; supports two triggered delay outputs or ORed together; pulsed output could be used for HSCMP windowing signal
  - iEvent — User programmable combinational boolean output using the four selected iEvent input channels for use as interrupt requests, DMA transfer requests, or hardware triggers
  - FTM — Two 6-channel flexible timer/PWM modules with DMA request option; deadtime insertion is available for each complementary channel pair; channels operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs); 16-bit free-running counter; the load of the FTM registers which have write buffer can be synchronized; write protection for critical registers; backwards compatible with TPM
  - TPM — 16-bit free-running or modulo up/down count operation; two channels, each channel may be input capture, output compare, or edge-aligned PWM; one interrupt per channel plus terminal count interrupt
  - CRC — High speed hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial; error detection for all single, double, odd, and most multi-bit errors; programmable initial seed value
  - HSCMP — Two analog comparators with selectable interrupt on rising edge, falling edge, or either edges of comparator output; the positive and negative inputs of the comparator are both driven from 4-to-1 muxes; programmable voltage reference from two internal DACs; support DMA transfer
  - IIC — Compatible with IIC bus standard and SMBus version 2 features; up to 100 kbps with maximum bus loading; multi-master operation; software programmable for one of 64 different serial clock frequencies; programmable slave address and glitch input filter; interrupt driven byte-by-byte data transfer; arbitration lost interrupt with automatic mode switching from master to slave; calling address identification interrupt; bus busy detection; broadcast and 10-bit address extension; address matching causes wake-up when MCU is in Stop3 mode; DMA support
  - SCI — Two serial communications interface modules with optional 13-bit break; full-duplex, standard non-return-to-zero (NRZ) format; double-buffered transmitter and receiver with separate enables; 13-bit baud rate selection with /32 fractional divide; interrupt-driven or polled operation; hardware parity generation and checking; programmable 8-bit or 9-bit character length; receiver wakeup by idle-line or address-mark; address match feature in receiver to reduce address-mark wakeup ISR overhead; 1/16 bit-time noise detection; DMA transmission for both transmit and receive
  - SPI — Two serial peripheral interfaces with full-duplex or single-wire bidirectional option; double-buffered transmitter and receiver; master or slave mode operation; selectable MSB-first or LSB-first shifting; 8-bit or 16-bit data modes; programmable transmit bit rate; receive data buffer hardware match feature; DMA transmission for transmit and receive
- Input/Output
  - Up to 69 GPIOs and one Input-only pin
  - Interrupt or DMA request with selectable polarity on all input pins
  - Programmable glitch filter, hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
  - Independent pin value register to read logic level on digital pin
  - Up to 16 rapid general purpose I/O (RGPIO) pins connected to the processor’s local 32-bit platform bus with set, clear, and faster toggle functionality

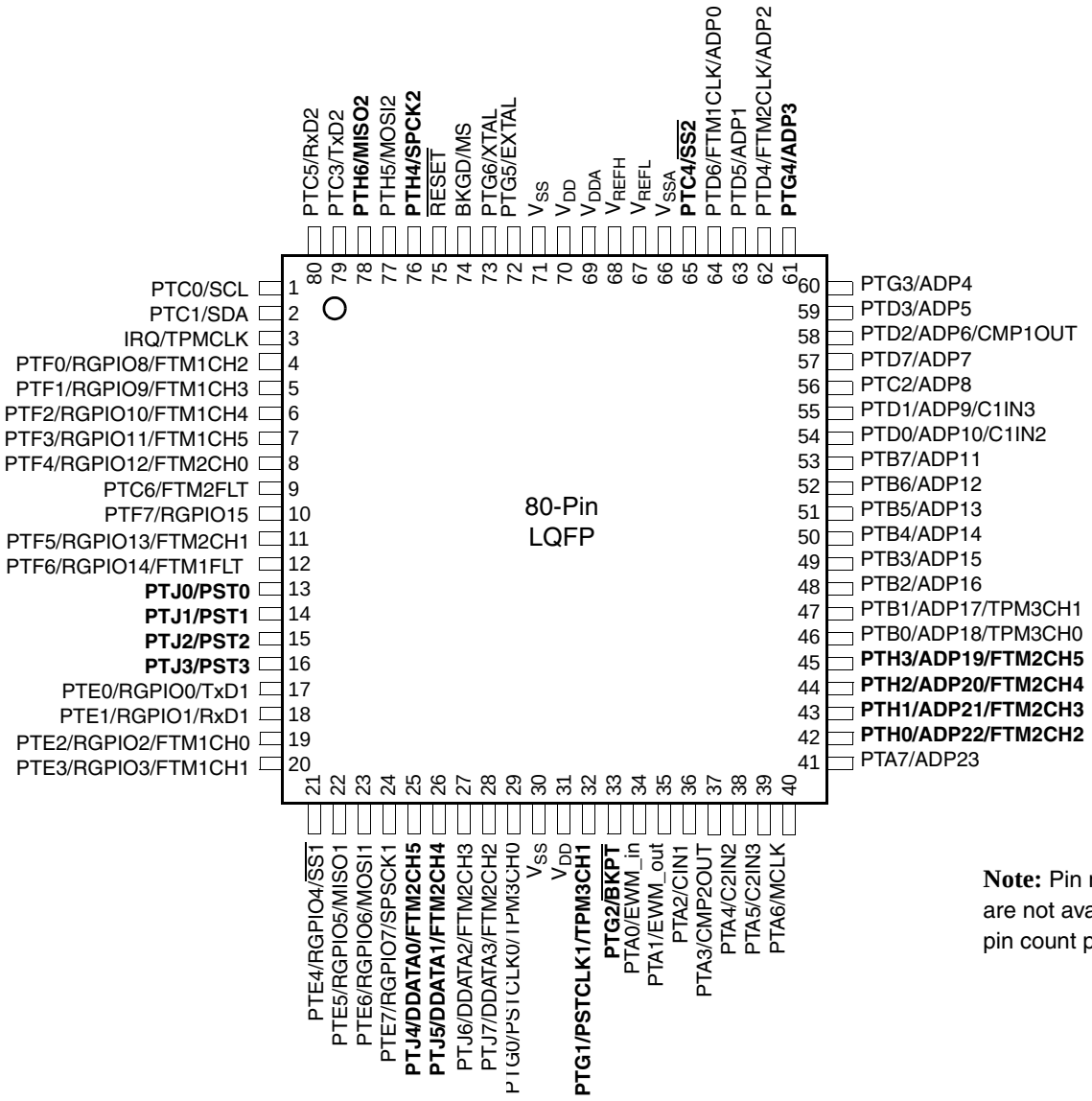
Table 2. MCF51AG128 Series Functional Units (continued)

Functional Unit	Function
WDOG (Watchdog timer)	keeps a watch on the system functioning and resets it in case of its failure
RTC (Real Time Counter)	Provides a constant time-base with optional interrupt

1.4 Pin Assignments

This section describes the pin assignments for the available packages.

Figure 2 shows the pinout of the 80-pin LQFP.



Note: Pin names in **bold** are not available in lower pin count packages.

Figure 2. 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

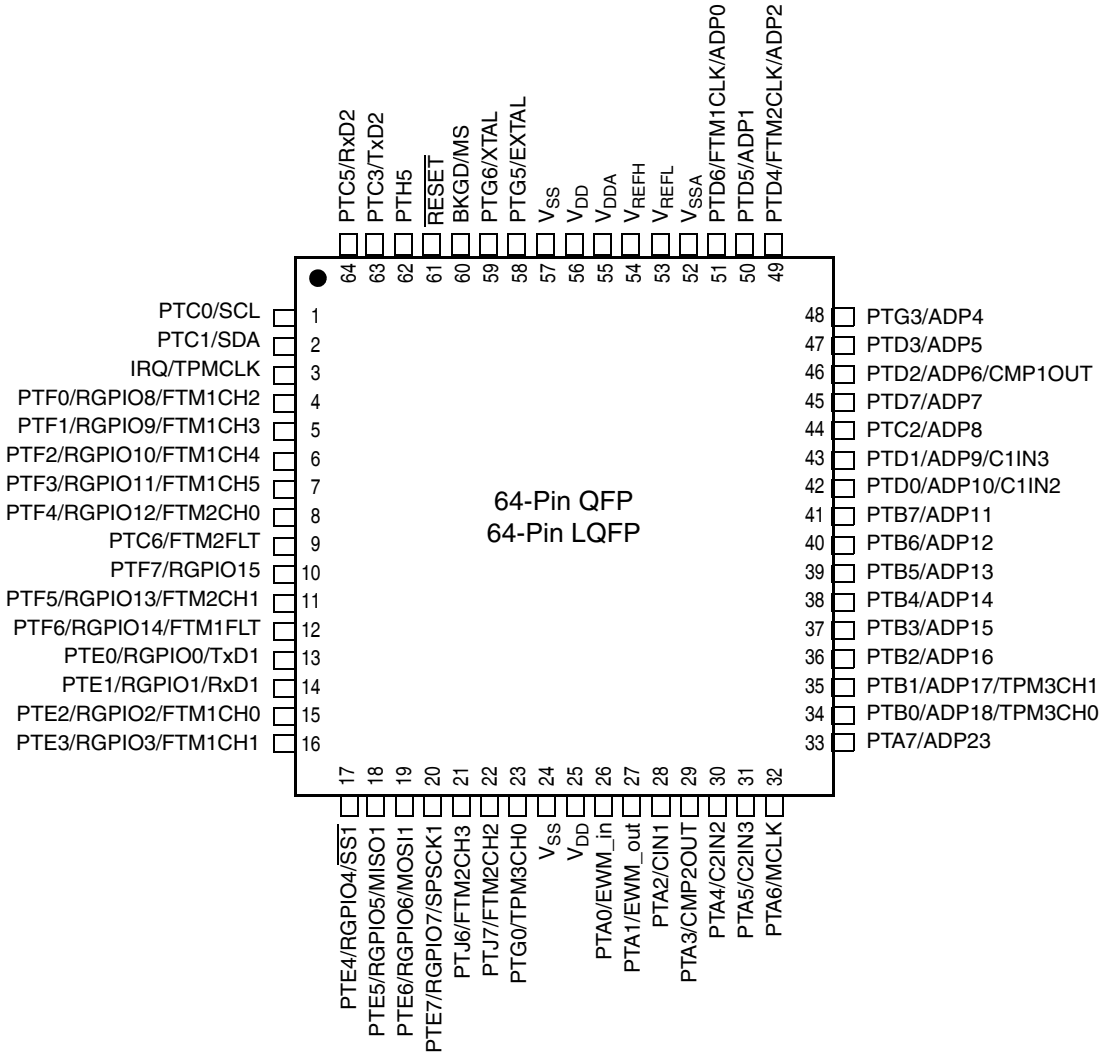


Figure 3. 64-Pin QFP and LQFP

Figure 4 shows the pinout of the 48-pin LQFP.

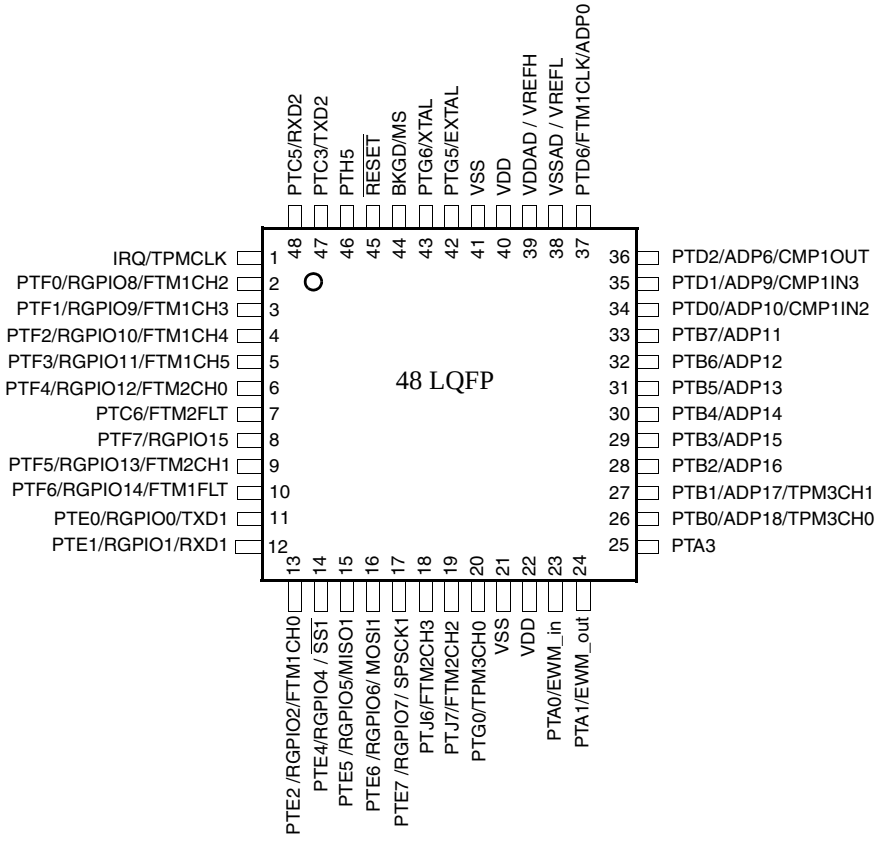


Figure 4. 48-Pin LQFP

Table 3. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest		
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**
41	33	—	PTA7	ADP23	
42	—	—	PTH0	ADP22	FTM2CH2
43	—	—	PTH1	ADP21	FTM2CH3
44	—	—	PTH2	ADP20	FTM2CH4
45	—	—	PTH3	ADP19	FTM2CH5
46	34	26	PTB0	ADP18	TPM3CH0
47	35	27	PTB1	ADP17	TPM3CH1
48	36	28	PTB2	ADP16	
49	37	29	PTB3	ADP15	
50	38	30	PTB4	ADP14	
51	39	31	PTB5	ADP13	
52	40	32	PTB6	ADP12	
53	41	33	PTB7	ADP11	
54	42	34	PTD0	ADP10	C1IN2
55	43	35	PTD1	ADP9	C1IN3
56	44	—	PTC2	ADP8	
57	45	—	PTD7	ADP7	
58	46	36	PTD2	ADP6	CMP1OUT
59	47	—	PTD3	ADP5	
60	48	—	PTG3	ADP4	
61	—	—	PTG4	ADP3	
62	49	—	PTD4	FTM2CLK	ADP2
63	50	—	PTD5	ADP1	
64	51	37	PTD6	FTM1CLK	ADP0
65	—	—	PTC4	$\overline{SS2}$	
66	52	38	V_{SSA}		
67	53	38	V_{REFL}		
68	54	39	V_{REFH}		
69	55	39	V_{DDA}		
70	56	40	V_{DD}		
71	57	41	V_{SS}		
72	58	42	PTG5	EXTAL	
73	59	43	PTG6	XTAL	
74	60	44	BKGD	MS	
75	61	45	$\overline{RESET}$		
76	—	—	PTH4	SPSCK2	
77	62	46	PTH5	MOSI2	
78	—	—	PTH6	MISO2	
79	63	47	PTC3	TxD2	
80	64	48	PTC5	RxD2	

[1] TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AG128 series MCUs, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 5. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 6. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to 105	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s	θ_{JA}	56	°C/W
	2s2p		45	
64-pin QFP				
	1s		54	
	2s2p		41	
64-pin LQFP				
	1s		67	
	2s2p		49	
48-pin LQFP				
	1s		69	
	2s2p		51	

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at 4 MHz CPU clock (All Peripheral Clocks are ON)	RI_{DD}	5	5.8	7	mA
				3	5.7	7	
2	C	Run supply current[3] measured at 16 MHz CPU clock (All Peripheral Clocks are ON)		5	21	25	mA
				3	20.9	25	
3	C	Run supply current[3] measured at 32 MHz CPU clock (All Peripheral Clocks are ON)		5	39.2	50	mA
				3	39.1	50	
4	P	Run supply current[3] measured at 50MHz CPU clock (All Peripheral Clocks are ON)		5	57.9	70	mA
				3	57.8	70	
5	C	Run supply current[3] measured at 4 MHz CPU clock (All Peripheral Clocks are OFF[4])	RI_{DD}	5	4.7	6	mA
				3	4.6	6	
6	C	Run supply current[3] measured at 16 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	16.1	20	mA
				3	15.9	20	
7	C	Run supply current[3] measured at 32 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	29	35	mA
				3	28.9	35	
8	C	Run supply current[3] measured at 50 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	44.1	50	mA
				3	44.0	50	
9	C	Wait supply current[3] measured at 4 MHz CPU clock	WI_{DD}	5	3.2	5	mA
				3	3.2	5	
10	C	Wait supply current[3] measured at 16 MHz CPU clock		5	10.1	13	mA
				3	10	13	
11	C	Wait supply current[3] measured at 32 MHz CPU clock		5	19	25	mA
				3	18.8	25	
12	C	Wait supply current[3] measured at 50 MHz CPU clock		5	29.2	40	mA
				3	29	40	
13	C P C	Stop2 mode supply current –40 °C 25 °C 105 °C	$S2I_{DD}$	5	 1.17 1.35 28.6	 3 3 40	µA
	C P C	–40 °C 25 °C 105 °C		3	1.0 1.34 26.8	3 3 40	µA

Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
14		Stop3 mode supply current	$S3I_{DD}$				
	C	–40 °C		5	1.2	3	μA
	P	25 °C			1.7	3	
	C	105 °C			43.3	60	
	C	–40 °C		3	1.04	3	μA
	P	25 °C			1.6	3	
	C	105 °C			45.5	60	
15		Stop4 mode supply current	$S4I_{DD}$				
	C	–40 °C		5	106	130	μA
	P	25 °C			109	130	
	C	105 °C			155	170	
	C	–40 °C		3	95	130	μA
	P	25 °C			98	130	
	C	105 °C			142	170	
16	C	RTC adder to stop2 or stop3[5], 25 °C	$S23I_{DDRTC}$	5	300	—	nA
				3	300	—	nA
17	C	Adder to stop3 for oscillator enabled[6] (ERCLKEN = 1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5	—	μA

1 Typicals are measured at 25 °C.

2 Values given here are preliminary estimates prior to completing characterization.

3 Code run from flash, FEI mode, and does not include any dc loads on port pins. Bus CLK= (CPU CLK/2)

4 GPIO filters are working on LPO clock.

5 Most customers are expected to use auto-wakeup from stop2 or stop3 instead of the higher current wait mode.

6 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

Figure 9. Run Current at Different Conditions

2.7 High Speed Comparator (HSCMP) Electricals

Table 11. HSCMP Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current, high speed mode (EN = 1, PMODE = 1)	I_{DDAHS}	—	200	—	μA
3	T	Supply current, low speed mode (EN = 1, PMODE = 0)	I_{DDALS}	—	20	—	μA
4	—	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
5	D	Analog input offset voltage	V_{AIO}	—	5	40	mV
6	D	Analog Comparator hysteresis	V_H	3.0	9.0	20.0	mV
7	D	Propagation delay, high speed mode (EN = 1, PMODE = 1)	t_{DHS}	—	70	120	ns
8	D	Propagation delay, low speed mode (EN = 1, PMODE = 0)	t_{DLS}	—	400	600	ns
9	D	Analog Comparator initialization delay	t_{AINIT}	—	400	—	ns

2.8 Digital to Analog (DAC) Characteristics

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DDA}	2.7	—	5.5	V
2	D	Supply current (enabled)	I_{DDAC}	—	—	20	μA
3	D	Supply current (stand-by)	I_{DDACS}	—	—	150	nA
4	D	DAC reference input voltage	V_{in1}, V_{in2}	V_{SSA}	—	V_{DDA}	V
5	D	DAC setup delay	t_{PRGST}	—	1000	—	nS
6	D	DAC step size	V_{step}	$3V_{in}/128$	$V_{in}/32$	$5V_{in}/128$	V
7	D	DAC output voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.9 ADC Characteristics

Table 12. 5V 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
			Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	—
2	D	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	—

Table 13. 5 V 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC = 1)		1.25	2	3.3		
7	P	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long Sample (ADLSMP = 1)		—	40	—		
8	T	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long Sample (ADLSMP = 1)		—	23.5	—		
9	T	Total Unadjusted Error	12 bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	P		10 bit mode		—	±1	±2.5		
	T		8 bit mode		—	±0.5	±1.0		
10	T	Differential Non-Linearity	12 bit mode	DNL	—	±1.75	—	LSB[2]	—
	P		10 bit mode[3]		—	±0.5	±1.0		
	T		8 bit mode[5]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12 bit mode	INL	—	±1.5	—	LSB[2]	—
	P		10 bit mode		—	±0.5	±1.0		
	T		8 bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12 bit mode	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	P		10 bit mode		—	±0.5	±1.5		
	T		8 bit mode		—	±0.5	±0.5		
13	T	Full-Scale Error	12 bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10 bit mode		—	±0.5	±1		
	T		8 bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12 bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10 bit mode		—	—	±0.5		
			8 bit mode		—	—	±0.5		
15	D	Input Leakage Error	12 bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10 bit mode		—	±0.2	±2.5		
			8 bit mode		—	±0.1	±1		

Table 15. ICS Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
10	D	FLL acquisition time [3]	$t_{fll\_acquire}$	—	—	1	ms
11	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
12	D	Loss of external clock minimum freq. (RANGE = 0) • ext. clock freq: above $(3/5)f_{int}$, never reset • ext. clock freq: between $(2/5)f_{int}$ and $(3/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(2/5)f_{int}$, always reset	f_{loc_low}	$(3/5) \times f_{int}$	—	—	kHz
13	D	Loss of external clock minimum freq. (RANGE = 1) • ext. clock freq: above $(16/5)f_{int}$, never reset • ext. clock freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(15/5)f_{int}$, always reset	f_{loc_high}	$(16/5) \times f_{int}$	—	—	kHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry by V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

2.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.12.1 Control Timing

Table 16. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width[2] (t_{cyc} = 1/f_{Self_reset})	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
8		Port rise and fall time (load = 30 pF for SPI, rest 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	 — —	 11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

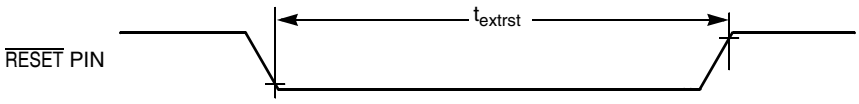


Figure 11. Reset Timing

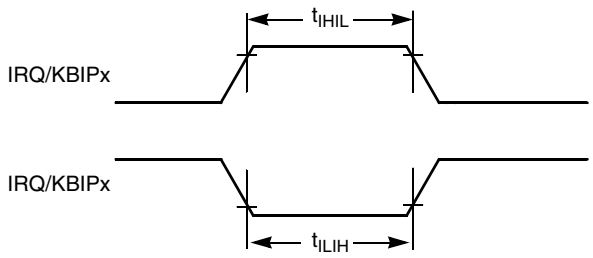


Figure 12. IRQ/KBIPx Timing

2.12.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 17. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

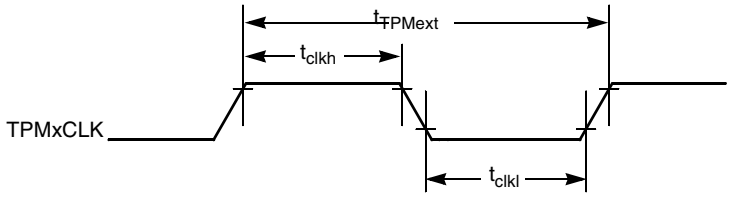


Figure 13. Timer External Clock

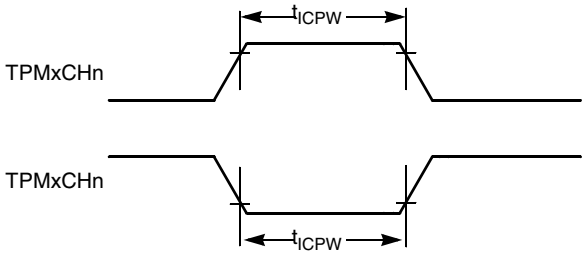


Figure 14. Timer Input Capture Pulse

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		PAGE: 840F
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NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
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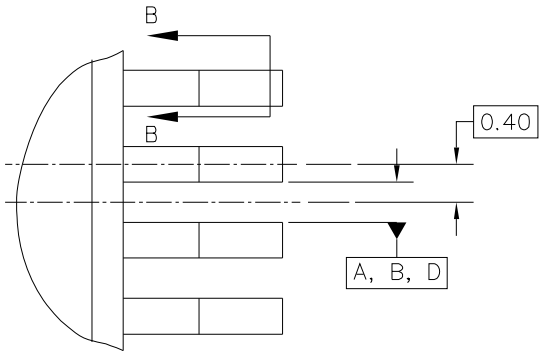
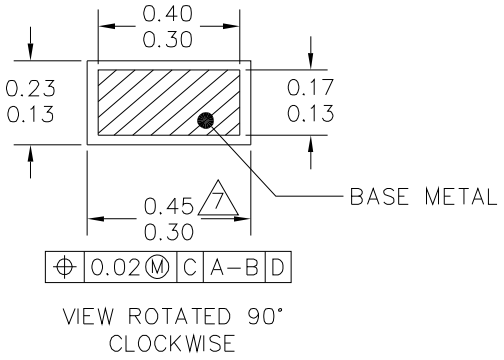
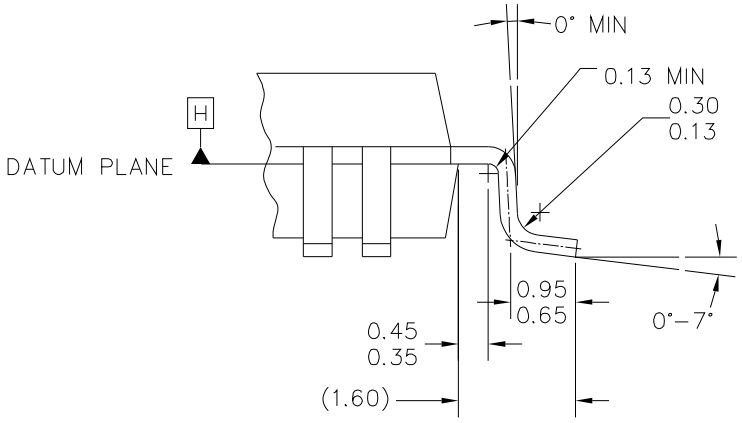


DETAIL "A"



VIEW ROTATED 90° CLOCKWISE

SECTION B–B



DETAIL "C"

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	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 2 OF 4

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		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A−B AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

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