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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	53
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 19x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-LQFP
Supplier Device Package	64-LQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mcf51ag96clh

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1 MCF51AG128 Family Configurations

1.1 Device Comparison

The following table compares the various device derivatives available within the MCF51AG128 series MCUs.

Table 1. MCF51AG128 Series Device Comparison

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
Flash memory size (KB)	128			96		
RAM size (KB)	16					
ColdFire V1 core with BDM (background debug module)	Yes					
HSCMP (analog comparator)	2	2	1	2	2	1
ADC (analog-to-digital converter) channels (12-bit)	24	19	12	24	19	12
CRC (cyclic redundancy check)	Yes					
DAC	2	2	1	2	2	1
DMA controller	4-ch					
iEvent (intelligent Event module)	Yes					
EWM (External Watchdog Monitor)	Yes					
WDOG (Watchdog timer)	Yes					
RTC	Yes					
DBG (debug module)	Yes					
IIC (inter-integrated circuit)	1	1	No	1	1	No
IRQ (interrupt request input)	Yes					
INTC (interrupt controller)	Yes					
LVD (low-voltage detector)	Yes					
ICS (internal clock source)	Yes					
OSC (crystal oscillator)	Yes					
Port I/O[1]	69	53	39	69	53	39
RGPIO (rapid general-purpose I/O)	16	16	15	16	16	15
SCI (serial communications interface)	2					
SPI1 (serial peripheral interface)	Yes					
SPI2 (serial peripheral interface)	Yes	No	No	Yes	No	No
FTM1 (flexible timer module) channels	6[2]					
FTM2 channels	6[2]					

Table 1. MCF51AG128 Series Device Comparison (continued)

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
TPM3 (timer pulse-width modulator) channels	2					
Debug Visibility Bus	Yes	No	No	Yes	No	No

[1] Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

[2] Some pins of FTMx might not be bonded on small package, therefore these channels could be used as soft timer only.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AG128 series pins and modules.

1.3 Features

Table 2 describes the functional units of the MCF51AG128 series.

Table 2. MCF51AG128 Series Functional Units

Functional Unit	Function
CF1Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants, and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provide a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
HSCMP1, HSCMP2 (analog comparators)	Compare two analog inputs
DAC1, DAC2 (digital-to-analog converter)	Provide programmable voltage reference for HSCMPx
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
ICS (internal clock source)	Provides clocking options for the device, including a frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the FLL
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1, SPI2 (8/16-bit serial peripheral interfaces)	Provide 8/16-bit 4-pin synchronous serial interface
DMA	Provides the means to directly transfer data between system memory and I/O peripherals
iEvent	Highly programmable module for creating combinational boolean outputs for use as interrupt requests, DMA transfer requests, or hardware triggers
EWM (External Watchdog Monitor)	Additional watchdog system to help reset external circuits

Table 2. MCF51AG128 Series Functional Units (continued)

Functional Unit	Function
WDOG (Watchdog timer)	keeps a watch on the system functioning and resets it in case of its failure
RTC (Real Time Counter)	Provides a constant time-base with optional interrupt

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

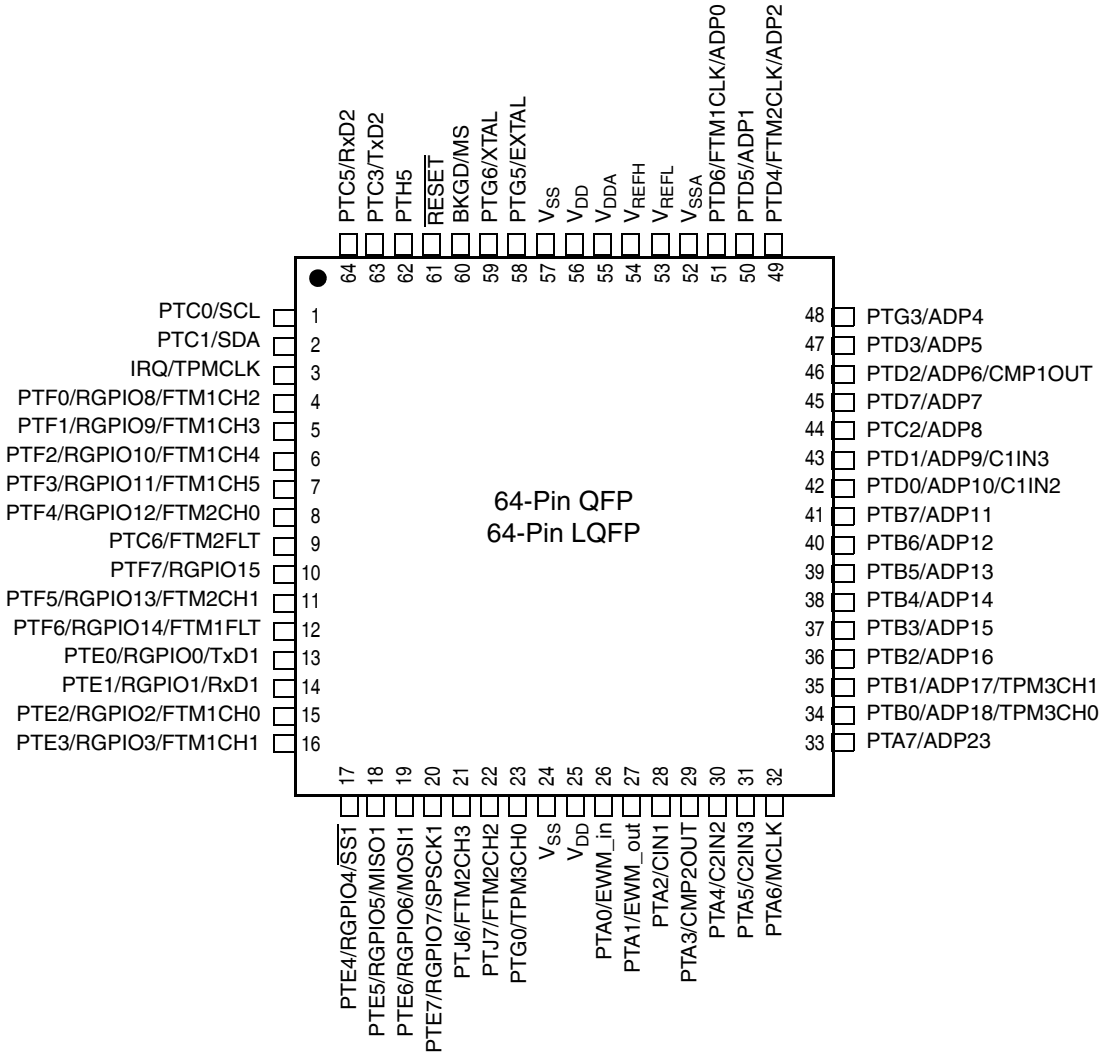


Figure 3. 64-Pin QFP and LQFP

Table 3 shows the package pin assignments.

Table 3. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest		
80	64	48	Port Pin	Alt 1	Alt 2
1	1	—	PTC0	SCL	
2	2	—	PTC1	SDA	
3	3	1	IRQ	TPMCLK[1]	
4	4	2	PTF0	RGPIO8	FTM1CH2
5	5	3	PTF1	RGPIO9	FTM1CH3
6	6	4	PTF2	RGPIO10	FTM1CH4
7	7	5	PTF3	RGPIO11	FTM1CH5
8	8	6	PTF4	RGPIO12	FTM2CH0
9	9	7	PTC6	FTM2FLT	
10	10	8	PTF7	RGPIO15	
11	11	9	PTF5	RGPIO13	FTM2CH1
12	12	10	PTF6	RGPIO14	FTM1FLT
13	—	—	PTJ0	PST0	
14	—	—	PTJ1	PST1	
15	—	—	PTJ2	PST2	
16	—	—	PTJ3	PST3	
17	13	11	PTE0	RGPIO0	TxD1
18	14	12	PTE1	RGPIO1	RxD1
19	15	13	PTE2	RGPIO2	FTM1CH0
20	16	—	PTE3	RGPIO3	FTM1CH1
21	17	14	PTE4	RGPIO4	$\overline{SS1}$
22	18	15	PTE5	RGPIO5	MISO1
23	19	16	PTE6	RGPIO6	MOSI1
24	20	17	PTE7	RGPIO7	SPSCK1
25	—	—	PTJ4	DDATA0	FTM2CH5
26	—	—	PTJ5	DDATA1	FTM2CH4
27	21	18	PTJ6	DDATA2	FTM2CH3
28	22	19	PTJ7	DDATA3	FTM2CH2
29	23	20	PTG0	PSTCLK0	TPM3CH0
30	24	21	V_{SS}		
31	25	22	V_{DD}		
32	—	—	PTG1	PSTCLK1	TPM3CH1
33	—	—	PTG2	$\overline{BKPT}$	
34	26	23	PTA0	EWM_in	
35	27	24	PTA1	EWM_out	
36	28	—	PTA2	CIN1	
37	29	25	PTA3	CMP2OUT	
38	30	—	PTA4	C2IN2	
39	31	—	PTA5	C2IN3	
40	32	—	PTA6	MCLK	

Table 5. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 6. Thermal Characteristics

Rating		Symbol	Value	Unit
Operating temperature range (packaged)		T_A	–40 to 105	°C
Maximum junction temperature		T_J	150	°C
Thermal resistance [1,2,3,4]				
80-pin LQFP				
	1s	θ_{JA}	56	°C/W
	2s2p		45	
64-pin QFP				
	1s		54	
	2s2p		41	
64-pin LQFP				
	1s		67	
	2s2p		49	
48-pin LQFP				
	1s		69	
	2s2p		51	

Table 9. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
6	P	Input high voltage; all digital inputs	V_{IH}	0.65 × V_{DD}	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	0.35 × V_{DD}	
8	D	Input hysteresis; all digital inputs	V_{hys}	0.06 × V_{DD}	—	—	mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[3] Internal pullup resistorsPTC0 and PTC1	R_{PU}	20 10	45 22	65 32	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	 3.9 4.0	 4.0 4.1	 4.1 4.2	V
17	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	 2.48 2.54	 2.56 2.62	 2.64 2.70	V
18	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	 4.5 4.6	 4.6 4.7	 4.7 4.8	V
19	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	 4.2 4.3	 4.3 4.4	 4.4 4.5	V
20	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	 2.84 2.90	 2.92 2.98	 3.00 3.06	V
21	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	 2.66 2.72	 2.74 2.80	 2.82 2.88	V
22	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	 — —	 100 60	 — —	mV
23	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
24	D	DC injection current[5 6 7 8] (single pin limit) V_{IN} > V_{DD} V_{IN} < V_{SS}	I_{IC}	 0 0	 — —	 2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) V_{IN} > V_{DD} V_{IN} < V_{SS}		 0 0	 — —	 25 –5	mA

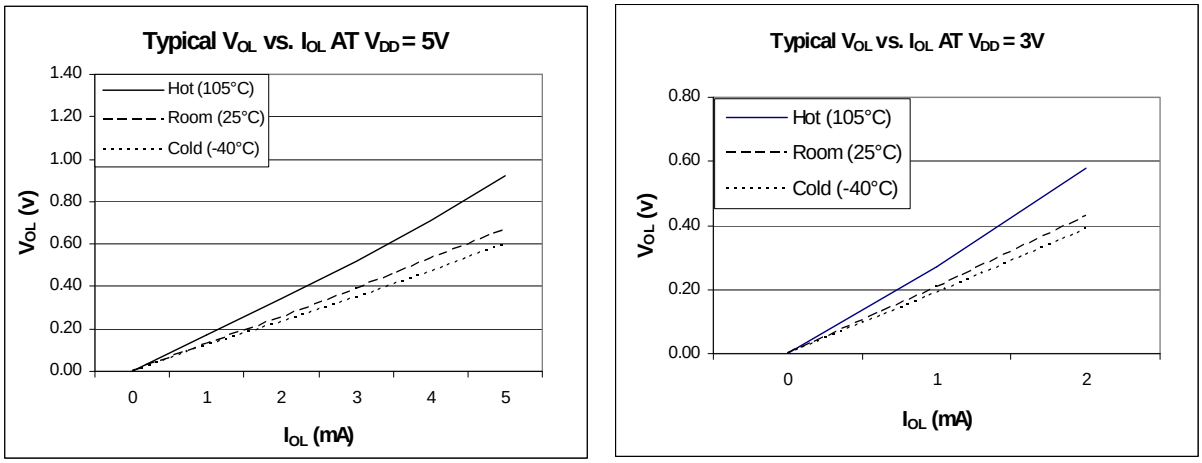


Figure 7. Typical I_{OL} vs. V_{OL} (Low Drive, PTxDSn = 0)

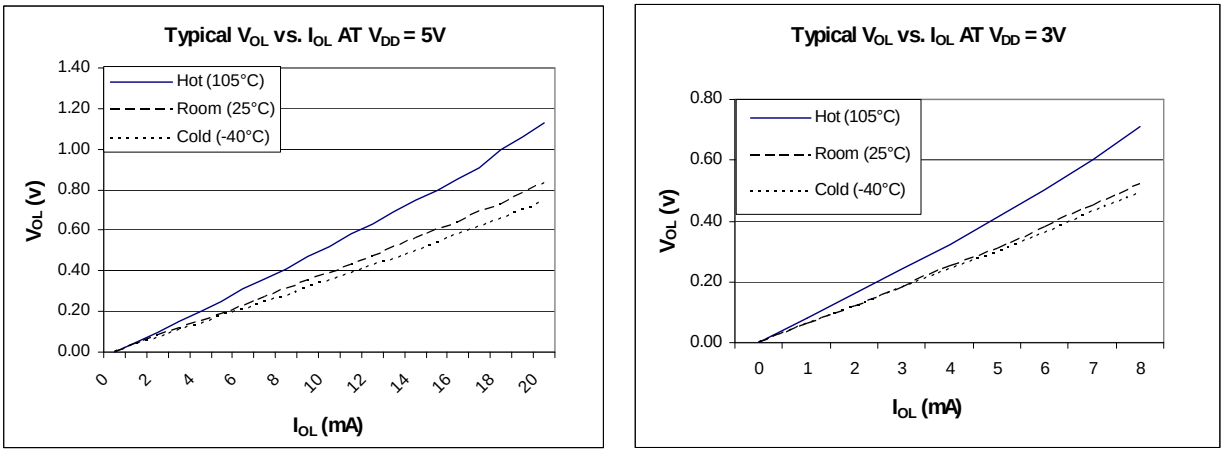


Figure 8. Typical I_{OL} vs. V_{OL} (High Drive, PTxDSn = 1)

2.6 Supply Current Characteristics

Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
1	C	Run supply current[3] measured at 4 MHz CPU clock (All Peripheral Clocks are ON)	RI_{DD}	5	5.8	7	mA
				3	5.7	7	
2	C	Run supply current[3] measured at 16 MHz CPU clock (All Peripheral Clocks are ON)		5	21	25	mA
				3	20.9	25	
3	C	Run supply current[3] measured at 32 MHz CPU clock (All Peripheral Clocks are ON)		5	39.2	50	mA
				3	39.1	50	
4	P	Run supply current[3] measured at 50MHz CPU clock (All Peripheral Clocks are ON)		5	57.9	70	mA
				3	57.8	70	
5	C	Run supply current[3] measured at 4 MHz CPU clock (All Peripheral Clocks are OFF[4])	RI_{DD}	5	4.7	6	mA
				3	4.6	6	
6	C	Run supply current[3] measured at 16 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	16.1	20	mA
				3	15.9	20	
7	C	Run supply current[3] measured at 32 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	29	35	mA
				3	28.9	35	
8	C	Run supply current[3] measured at 50 MHz CPU clock (All Peripheral Clocks are OFF[4])		5	44.1	50	mA
				3	44.0	50	
9	C	Wait supply current[3] measured at 4 MHz CPU clock	WI_{DD}	5	3.2	5	mA
				3	3.2	5	
10	C	Wait supply current[3] measured at 16 MHz CPU clock		5	10.1	13	mA
				3	10	13	
11	C	Wait supply current[3] measured at 32 MHz CPU clock		5	19	25	mA
				3	18.8	25	
12	C	Wait supply current[3] measured at 50 MHz CPU clock		5	29.2	40	mA
				3	29	40	
13	C P C	Stop2 mode supply current –40 °C 25 °C 105 °C	$S2I_{DD}$	5	 1.17 1.35 28.6	 3 3 40	µA
	C P C	–40 °C 25 °C 105 °C		3	1.0 1.34 26.8	3 3 40	µA

Table 12. 5V 12-bit ADC Operating Conditions (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
3	D	Ref Voltage High	—	V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	—
4	D	Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSA}	V_{SSA}	V	—
5	D	Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
6	C	Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
7	C	Input Resistance	—	R_{ADIN}	—	3	5	kΩ	—
8	C	Analog Source Resistance	12 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	C		10 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		 — —	 — —	 5 10		
	C		8 bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	D		Low Power (ADLPC = 1)		0.4	—	4.0		—

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 13. 5 V 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
16	D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	—
17	D	Temp Sensor Slope	–40 °C — 25 °C	m	—	3.266	—	mV/°C	—
			25 °C — 85 °C		—	3.638	—		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.10 External Oscillator (XOSC) Characteristics

Table 14. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

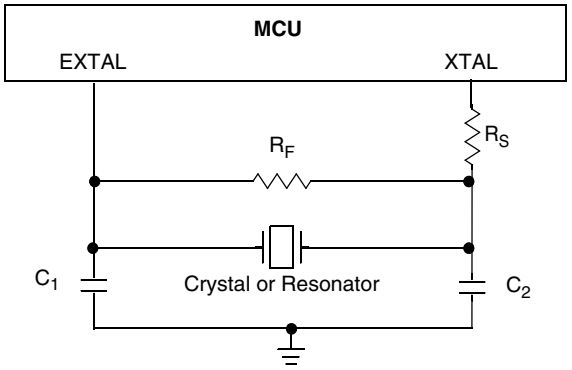
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 16 16 8	 kHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		10 1	—	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[3]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 1500 2000 3 7	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode [2] FBE mode[2] FBELP mode	f_{extal}	 0.03125 0 0	 — — —	 50.33 50.33 50.33	MHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal



2.11 ICS Specifications

Table 15. ICS Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range - untrimmed [2]	Low range (DRS = 00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	C		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS = 01)		—	33.69	—	
	P		High range (DRS = 10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over full voltage and temperature range		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 –70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$

Table 15. ICS Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
10	D	FLL acquisition time [3]	$t_{fll\_acquire}$	—	—	1	ms
11	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
12	D	Loss of external clock minimum freq. (RANGE = 0) • ext. clock freq: above $(3/5)f_{int}$, never reset • ext. clock freq: between $(2/5)f_{int}$ and $(3/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(2/5)f_{int}$, always reset	f_{loc_low}	$(3/5) \times f_{int}$	—	—	kHz
13	D	Loss of external clock minimum freq. (RANGE = 1) • ext. clock freq: above $(16/5)f_{int}$, never reset • ext. clock freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(15/5)f_{int}$, always reset	f_{loc_high}	$(16/5) \times f_{int}$	—	—	kHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry by V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

2.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.12.1 Control Timing

Table 16. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width[2] (t_{cyc} = 1/f_{Self_reset})	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
8		Port rise and fall time (load = 30 pF for SPI, rest 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	 — —	 11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

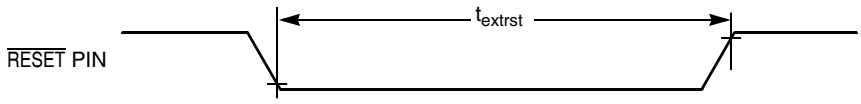


Figure 11. Reset Timing

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

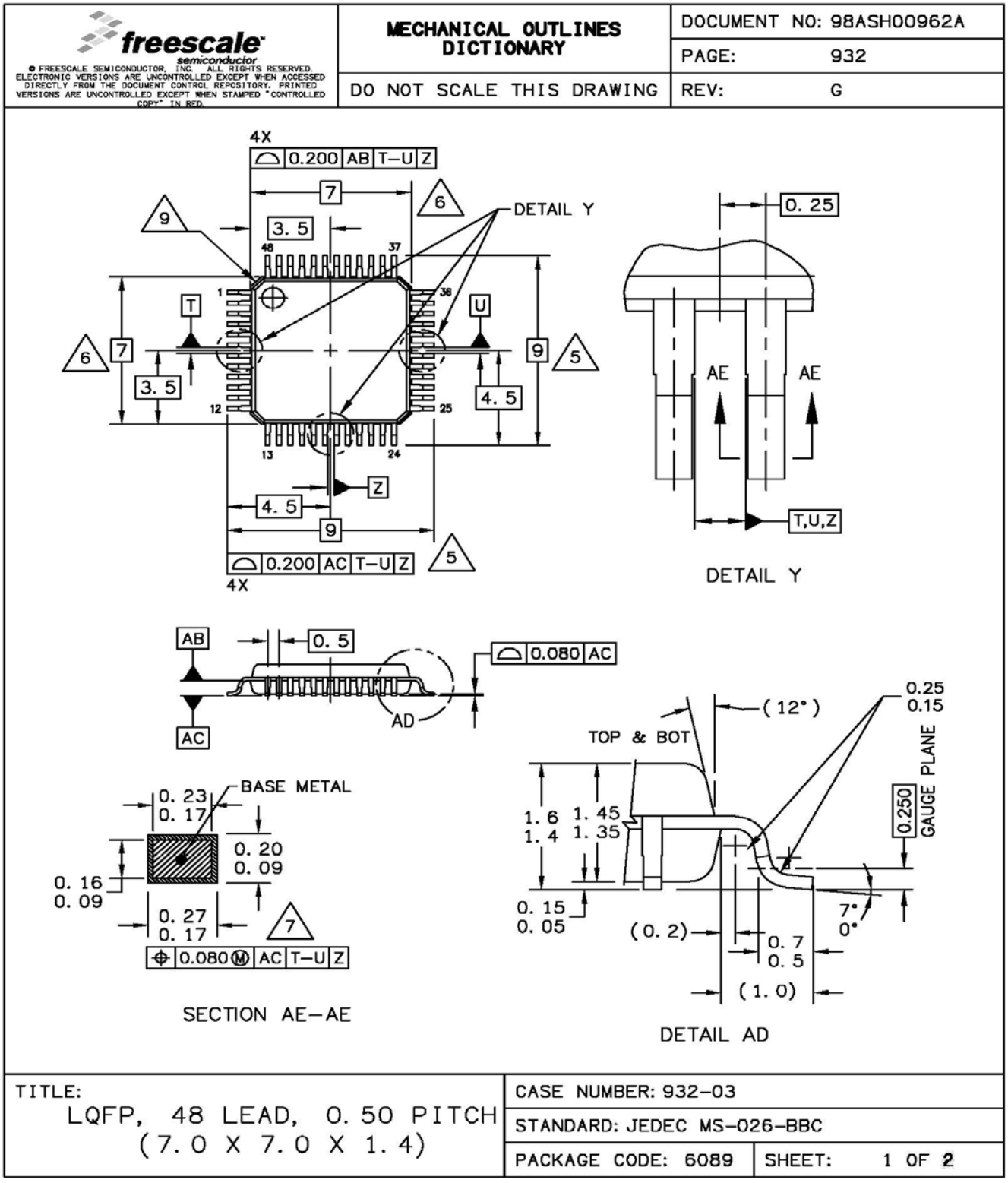
freescale semiconductor 	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE −H− IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A−B AND −D− TO BE DETERMINED AT DATUM PLANE −H−.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE −C−.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE −H−.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B−01	
	STANDARD: NON−JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

5.4 48-pin LQFP Package



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASH00962A
		PAGE: 932
	DO NOT SCALE THIS DRAWING	REV: G

NOTES:

1. DIMENSIONS AND TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE AB IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS T, U, AND Z TO BE DETERMINED AT DATUM PLANE AB.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE AC.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.250 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE AB.
7. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.350.
8. MINIMUM SOLDER PLATE THICKNESS SHALL BE 0.0076.
9. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

TITLE:	CASE NUMBER: 932–03	
LQFP, 48 LEAD, 0.50 PITCH (7.0 X 7.0 X 1.4)	STANDARD: JEDEC MS–026–BBC	
	PACKAGE CODE: 6089	SHEET: 2 OF 2