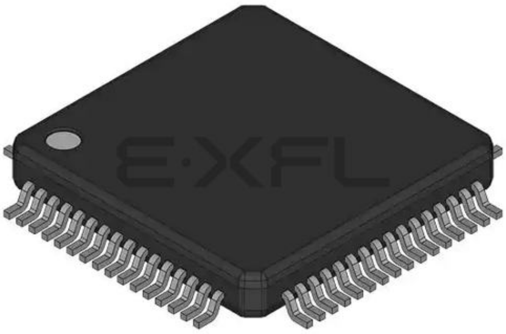

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	53
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 19x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-QFP
Supplier Device Package	64-QFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag96cqh

- System Clock Sources
  - Oscillator (XOSC) — Loop-control pierce oscillator; crystal or ceramic resonator range of 31.25 kHz to 38.4 kHz or 1 MHz to 16 MHz
  - Internal Clock Source (ICS) — Frequency-locked-loop (FLL) controlled by internal or external reference; trimmable internal reference allows 0.2% resolution and 2% deviation (1% across 0 to 70 ºC)
- Peripherals
  - ADC — 24 analog inputs with 12 bits resolution; output formatted in 12-, 10- or 8-bit right-justified format; single or continuous conversion (automatic return to idle after single conversion); interrupt or DMA request when conversion complete; operation in low-power modes for lower noise operation; asynchronous clock source for lower noise operation; selectable asynchronous hardware conversion triggers from RTC, PDB, or iEvent; dual samples based on hardware triggers during ping-pong mode; on-chip temperature sensor
  - PDB — 16-bit of resolution with prescaler; seven possible trigger events input; positive transition of trigger event signal initiates the counter; support continuous trigger or single shot, bypass mode; supports two triggered delay outputs or ORed together; pulsed output could be used for HSCMP windowing signal
  - iEvent — User programmable combinational boolean output using the four selected iEvent input channels for use as interrupt requests, DMA transfer requests, or hardware triggers
  - FTM — Two 6-channel flexible timer/PWM modules with DMA request option; deadtime insertion is available for each complementary channel pair; channels operate as pairs with equal outputs, pairs with complimentary outputs or independent channels (with independent outputs); 16-bit free-running counter; the load of the FTM registers which have write buffer can be synchronized; write protection for critical registers; backwards compatible with TPM
  - TPM — 16-bit free-running or modulo up/down count operation; two channels, each channel may be input capture, output compare, or edge-aligned PWM; one interrupt per channel plus terminal count interrupt
  - CRC — High speed hardware CRC generator circuit using 16-bit shift register; CRC16-CCITT compliancy with $x^{16} + x^{12} + x^5 + 1$ polynomial; error detection for all single, double, odd, and most multi-bit errors; programmable initial seed value
  - HSCMP — Two analog comparators with selectable interrupt on rising edge, falling edge, or either edges of comparator output; the positive and negative inputs of the comparator are both driven from 4-to-1 muxes; programmable voltage reference from two internal DACs; support DMA transfer
  - IIC — Compatible with IIC bus standard and SMBus version 2 features; up to 100 kbps with maximum bus loading; multi-master operation; software programmable for one of 64 different serial clock frequencies; programmable slave address and glitch input filter; interrupt driven byte-by-byte data transfer; arbitration lost interrupt with automatic mode switching from master to slave; calling address identification interrupt; bus busy detection; broadcast and 10-bit address extension; address matching causes wake-up when MCU is in Stop3 mode; DMA support
  - SCI — Two serial communications interface modules with optional 13-bit break; full-duplex, standard non-return-to-zero (NRZ) format; double-buffered transmitter and receiver with separate enables; 13-bit baud rate selection with /32 fractional divide; interrupt-driven or polled operation; hardware parity generation and checking; programmable 8-bit or 9-bit character length; receiver wakeup by idle-line or address-mark; address match feature in receiver to reduce address-mark wakeup ISR overhead; 1/16 bit-time noise detection; DMA transmission for both transmit and receive
  - SPI — Two serial peripheral interfaces with full-duplex or single-wire bidirectional option; double-buffered transmitter and receiver; master or slave mode operation; selectable MSB-first or LSB-first shifting; 8-bit or 16-bit data modes; programmable transmit bit rate; receive data buffer hardware match feature; DMA transmission for transmit and receive
- Input/Output
  - Up to 69 GPIOs and one Input-only pin
  - Interrupt or DMA request with selectable polarity on all input pins
  - Programmable glitch filter, hysteresis and configurable pull up/down device on all input pins
  - Configurable slew rate and drive strength on all output pins
  - Independent pin value register to read logic level on digital pin
  - Up to 16 rapid general purpose I/O (RGPIO) pins connected to the processor’s local 32-bit platform bus with set, clear, and faster toggle functionality

1.3 Features

Table 2 describes the functional units of the MCF51AG128 series.

Table 2. MCF51AG128 Series Functional Units

Functional Unit	Function
CF1Core (V1 ColdFire core)	Executes programs and interrupt handlers
BDM (background debug module)	Provides single pin debugging interface (part of the V1 ColdFire core)
DBG (debug)	Provides debugging and emulation capabilities (part of the V1 ColdFire core)
VBUS (debug visibility bus)	Allows for real-time program traces (part of the V1 ColdFire core)
SIM (system integration module)	Controls resets and chip level interfaces between modules
Flash (flash memory)	Provides storage for program code, constants, and variables
RAM (random-access memory)	Provides storage for program variables
RGPIO (rapid general-purpose input/output)	Allows for I/O port access at CPU clock speeds
VREG (voltage regulator)	Controls power management across the device
LVD (low-voltage detect)	Monitors internal and external supply voltage levels, and generates a reset or interrupt when the voltages are too low
CF1_INTC (interrupt controller)	Controls and prioritizes all device interrupts
ADC (analog-to-digital converter)	Measures analog voltages at up to 12 bits of resolution
FTM1, FTM2 (flexible timer/pulse-width modulators)	Provide a variety of timing-based features
TPM3 (timer/pulse-width modulator)	Provides a variety of timing-based features
CRC (cyclic redundancy check)	Accelerates computation of CRC values for ranges of memory
HSCMP1, HSCMP2 (analog comparators)	Compare two analog inputs
DAC1, DAC2 (digital-to-analog converter)	Provide programmable voltage reference for HSCMPx
IIC (inter-integrated circuit)	Supports standard IIC communications protocol
ICS (internal clock source)	Provides clocking options for the device, including a frequency-locked loop (FLL) for multiplying slower reference clock sources
OSC (crystal oscillator)	Allows a crystal or ceramic resonator to be used as the system clock source or reference clock for the FLL
SCI1, SCI2 (serial communications interfaces)	Serial communications UARTs capable of supporting RS-232 and LIN protocols
SPI1, SPI2 (8/16-bit serial peripheral interfaces)	Provide 8/16-bit 4-pin synchronous serial interface
DMA	Provides the means to directly transfer data between system memory and I/O peripherals
iEvent	Highly programmable module for creating combinational boolean outputs for use as interrupt requests, DMA transfer requests, or hardware triggers
EWM (External Watchdog Monitor)	Additional watchdog system to help reset external circuits

1.4 Pin Assignments

This section describes the pin assignments for the available packages.

Figure 2 shows the pinout of the 80-pin LQFP.

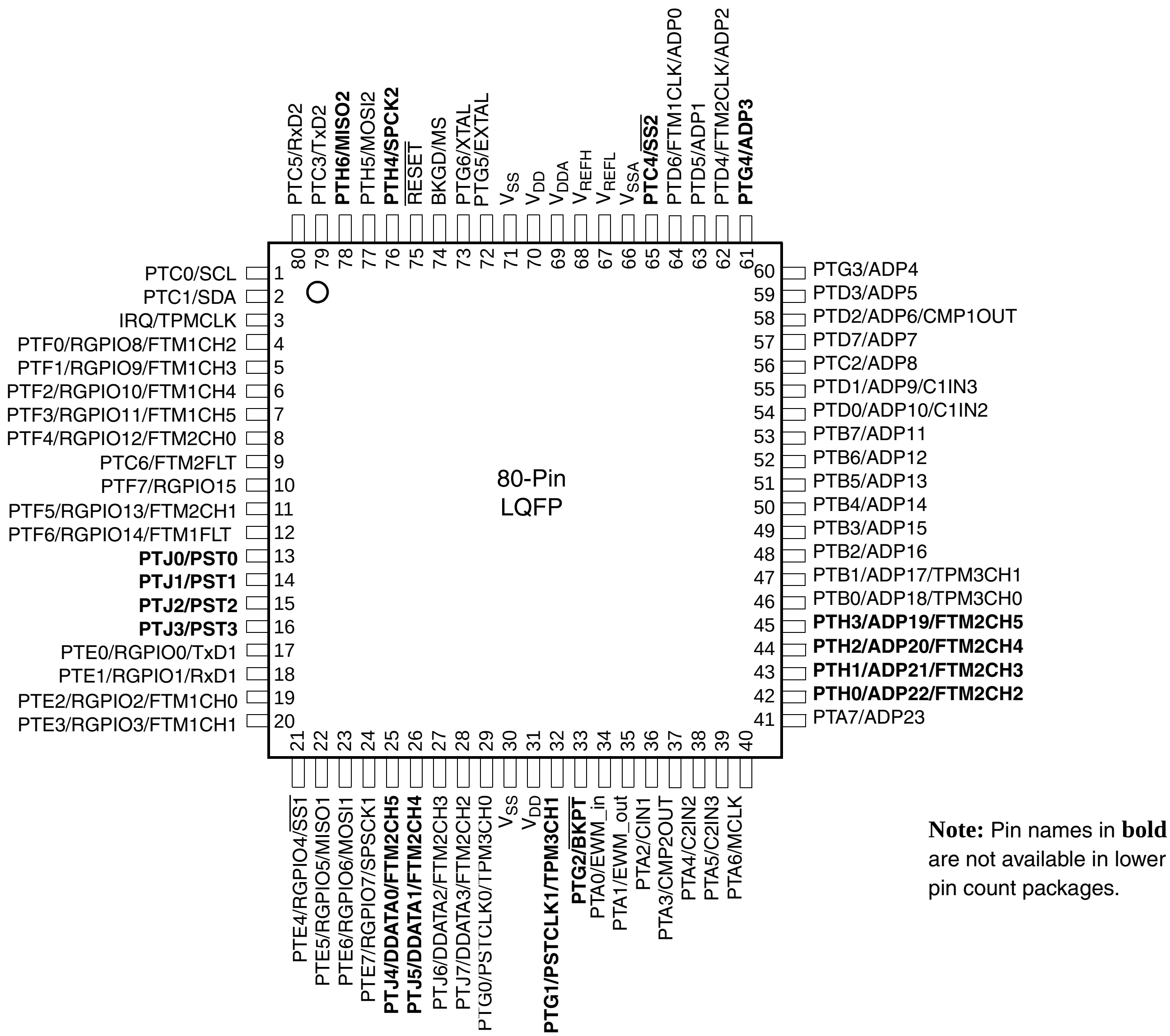


Figure 2. 80-Pin LQFP

Figure 3 shows the pinout of the 64-pin LQFP and QFP.

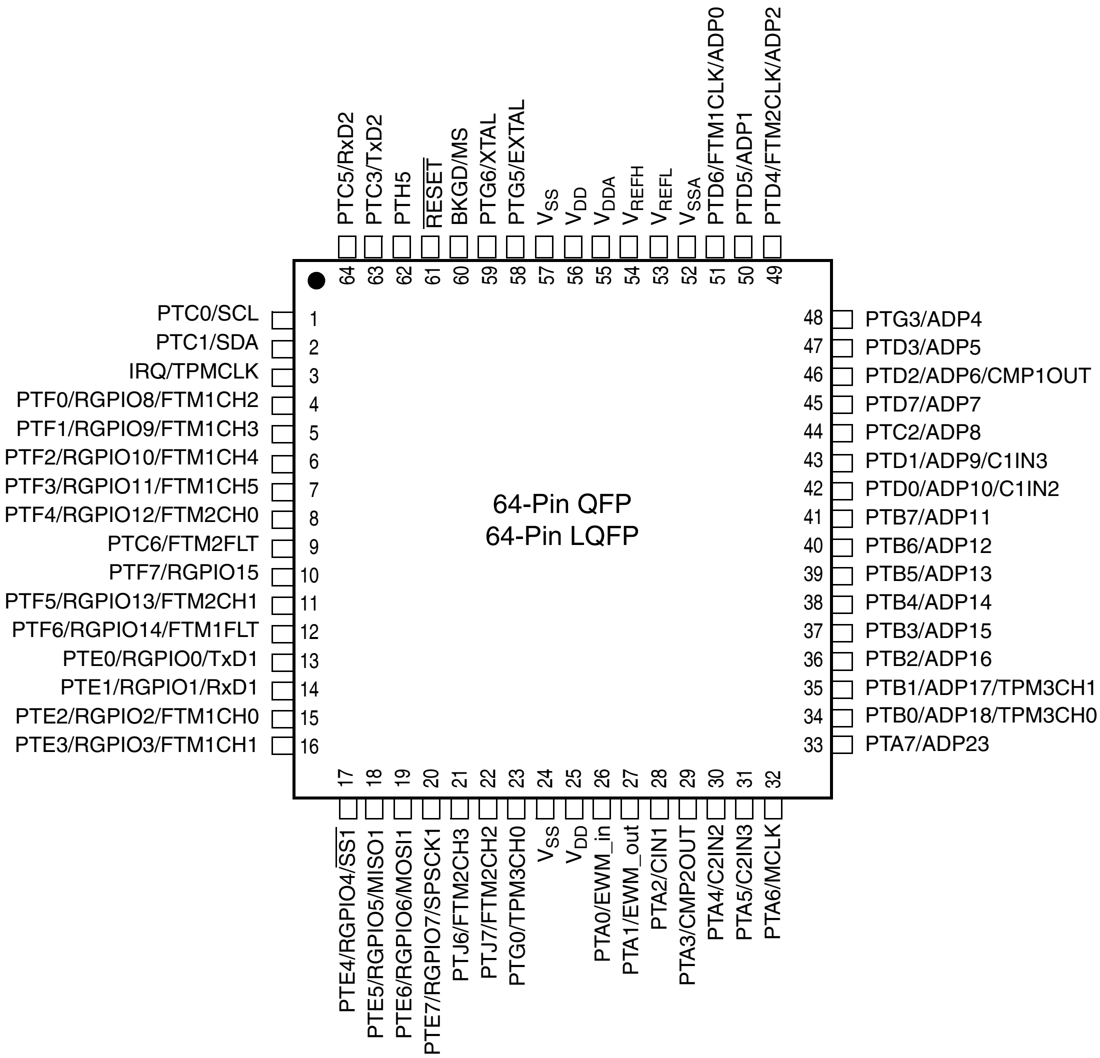


Figure 3. 64-Pin QFP and LQFP

Figure 4 shows the pinout of the 48-pin LQFP.

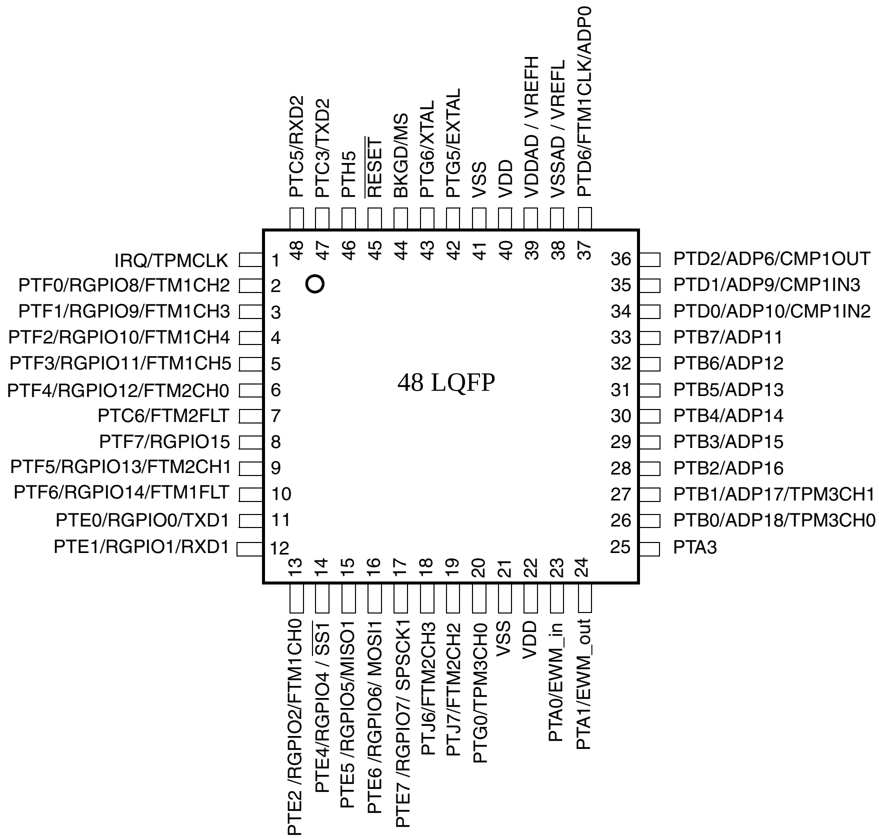


Figure 4. 48-Pin LQFP

Table 3 shows the package pin assignments.

Table 3. Pin Availability by Package Pin-Count

Pin Number			Lowest <-- Priority --> Highest		
80	64	48	Port Pin	Alt 1	Alt 2
1	1	—	PTC0	SCL	
2	2	—	PTC1	SDA	
3	3	1	IRQ	TPMCLK[1]	
4	4	2	PTF0	RGPIO8	FTM1CH2
5	5	3	PTF1	RGPIO9	FTM1CH3
6	6	4	PTF2	RGPIO10	FTM1CH4
7	7	5	PTF3	RGPIO11	FTM1CH5
8	8	6	PTF4	RGPIO12	FTM2CH0
9	9	7	PTC6	FTM2FLT	
10	10	8	PTF7	RGPIO15	
11	11	9	PTF5	RGPIO13	FTM2CH1
12	12	10	PTF6	RGPIO14	FTM1FLT
13	—	—	PTJ0	PST0	
14	—	—	PTJ1	PST1	
15	—	—	PTJ2	PST2	
16	—	—	PTJ3	PST3	
17	13	11	PTE0	RGPIO0	TxD1
18	14	12	PTE1	RGPIO1	RxD1
19	15	13	PTE2	RGPIO2	FTM1CH0
20	16	—	PTE3	RGPIO3	FTM1CH1
21	17	14	PTE4	RGPIO4	$\overline{SS1}$
22	18	15	PTE5	RGPIO5	MISO1
23	19	16	PTE6	RGPIO6	MOSI1
24	20	17	PTE7	RGPIO7	SPSCK1
25	—	—	PTJ4	DDATA0	FTM2CH5
26	—	—	PTJ5	DDATA1	FTM2CH4
27	21	18	PTJ6	DDATA2	FTM2CH3
28	22	19	PTJ7	DDATA3	FTM2CH2
29	23	20	PTG0	PSTCLK0	TPM3CH0
30	24	21	V_{SS}		
31	25	22	V_{DD}		
32	—	—	PTG1	PSTCLK1	TPM3CH1
33	—	—	PTG2	$\overline{BKPT}$	
34	26	23	PTA0	EWM_in	
35	27	24	PTA1	EWM_out	
36	28	—	PTA2	CIN1	
37	29	25	PTA3	CMP2OUT	
38	30	—	PTA4	C2IN2	
39	31	—	PTA5	C2IN3	
40	32	—	PTA6	MCLK	

Table 3. Pin Availability by Package Pin-Count (continued)

Pin Number			Lowest <-- Priority --> Highest		
80	**64**	**48**	**Port Pin**	**Alt 1**	**Alt 2**
41	33	—	PTA7	ADP23	
42	—	—	PTH0	ADP22	FTM2CH2
43	—	—	PTH1	ADP21	FTM2CH3
44	—	—	PTH2	ADP20	FTM2CH4
45	—	—	PTH3	ADP19	FTM2CH5
46	34	26	PTB0	ADP18	TPM3CH0
47	35	27	PTB1	ADP17	TPM3CH1
48	36	28	PTB2	ADP16	
49	37	29	PTB3	ADP15	
50	38	30	PTB4	ADP14	
51	39	31	PTB5	ADP13	
52	40	32	PTB6	ADP12	
53	41	33	PTB7	ADP11	
54	42	34	PTD0	ADP10	C1IN2
55	43	35	PTD1	ADP9	C1IN3
56	44	—	PTC2	ADP8	
57	45	—	PTD7	ADP7	
58	46	36	PTD2	ADP6	CMP1OUT
59	47	—	PTD3	ADP5	
60	48	—	PTG3	ADP4	
61	—	—	PTG4	ADP3	
62	49	—	PTD4	FTM2CLK	ADP2
63	50	—	PTD5	ADP1	
64	51	37	PTD6	FTM1CLK	ADP0
65	—	—	PTC4	$\overline{SS2}$	
66	52	38	V_{SSA}		
67	53	38	V_{REFL}		
68	54	39	V_{REFH}		
69	55	39	V_{DDA}		
70	56	40	V_{DD}		
71	57	41	V_{SS}		
72	58	42	PTG5	EXTAL	
73	59	43	PTG6	XTAL	
74	60	44	BKGD	MS	
75	61	45	$\overline{RESET}$		
76	—	—	PTH4	SPSCK2	
77	62	46	PTH5	MOSI2	
78	—	—	PTH6	MISO2	
79	63	47	PTC3	TxD2	
80	64	48	PTC5	RxD2	

[1] TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AG128 series MCUs, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

Table 5. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

[1] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

[2] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[3] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 6. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance [1,2,3,4]	θ_{JA}		°C/W
80-pin LQFP 1s		56	
80-pin LQFP 2s2p		45	
64-pin QFP 1s		54	
64-pin QFP 2s2p		41	
64-pin LQFP 1s		67	
64-pin LQFP 2s2p		49	
48-pin LQFP 1s		69	
48-pin LQFP 2s2p		51	

[1] Typical values are based on characterization data at 25°C unless otherwise stated.

[2] Measured with $V_{In} = V_{DD}$ or V_{SS}.

[3] Measured with $V_{In} = V_{SS}$.

[4] Measured with $V_{In} = V_{DD}$.

[5] Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

[6] All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

[7] Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

[8] The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

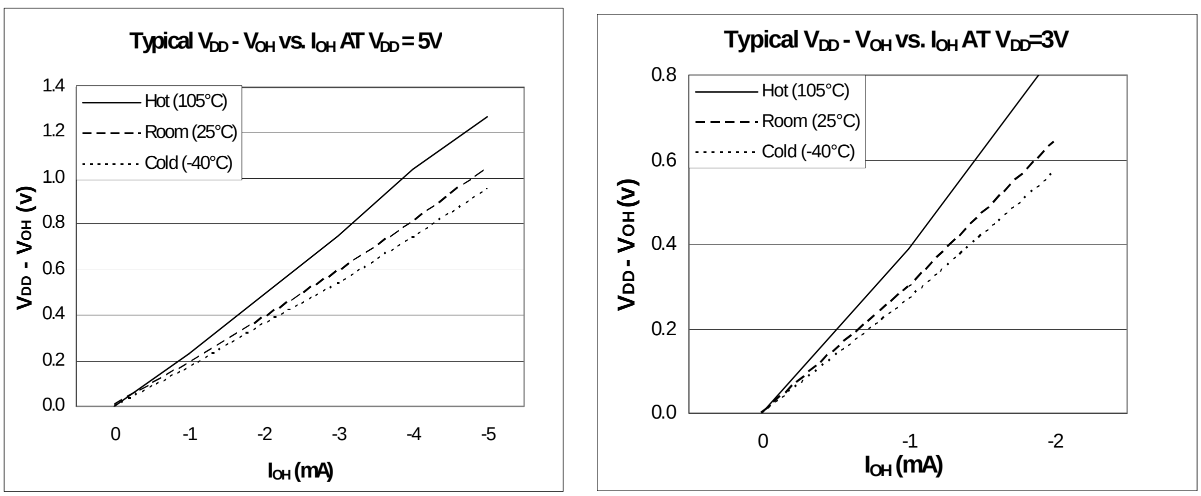


Figure 5. Typical I_{OH} vs. $V_{DD} - V_{OH}$ (Low Drive,PTxDSn = 0)

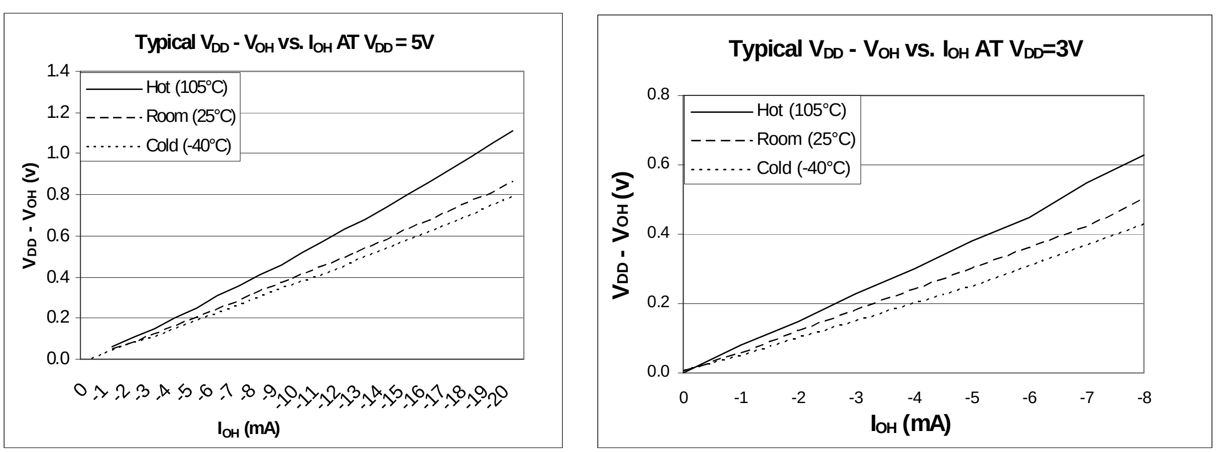


Figure 6. Typical I_{OH} vs. $V_{DD} - V_{OH}$ (High Drive, PTxDSn = 1)

Table 10. Supply Current Characteristics

Num	C	Parameter	Symbol	V_{DD} (V)	Typical[1]	Max[2]	Unit
14	 C P C	Stop3 mode supply current –40 °C 25 °C 105 °C	$S3I_{DD}$	5	1.2 1.7 43.3	3 3 60	μA
	C P C	–40 °C 25 °C 105 °C		3	1.04 1.6 45.5	3 3 60	μA
15	 C P C	Stop4 mode supply current –40 °C 25 °C 105 °C	$S4I_{DD}$	5	106 109 155	130 130 170	μA
	C P C	–40 °C 25 °C 105 °C		3	95 98 142	130 130 170	μA
16	C	RTC adder to stop2 or stop3[5], 25 °C	$S23I_{DDRTC}$	5	300	—	nA
				3	300	—	nA
17	C	Adder to stop3 for oscillator enabled[6] (ERCLKEN = 1 and EREFSTEN = 1)	$S3I_{DDOSC}$	5, 3	5	—	μA

1 Typicals are measured at 25 °C.
2 Values given here are preliminary estimates prior to completing characterization.
3 Code run from flash, FEI mode, and does not include any dc loads on port pins. Bus CLK= (CPU CLK/2)
4 GPIO filters are working on LPO clock.
5 Most customers are expected to use auto-wakeup from stop2 or stop3 instead of the higher current wait mode.
6 Values given under the following conditions: low range operation (RANGE = 0), low power mode (HGO = 0).

Figure 9. Run Current at Different Conditions

Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC = 1)		1.25	2	3.3		
7	P	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long Sample (ADLSMP = 1)		—	40	—		
8	T	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long Sample (ADLSMP = 1)		—	23.5	—		
9	T	Total Unadjusted Error	12 bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	P		10 bit mode		—	±1	±2.5		
	T		8 bit mode		—	±0.5	±1.0		
10	T	Differential Non-Linearity	12 bit mode	DNL	—	±1.75	—	LSB[2]	—
	P		10 bit mode[3]		—	±0.5	±1.0		
	T		8 bit mode[5]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12 bit mode	INL	—	±1.5	—	LSB[2]	—
	P		10 bit mode		—	±0.5	±1.0		
	T		8 bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12 bit mode	E_{ZS}	—	±1.5	—	LSB[2]	$V_{ADIN} = V_{SSAD}$
	P		10 bit mode		—	±0.5	±1.5		
	T		8 bit mode		—	±0.5	±0.5		
13	T	Full-Scale Error	12 bit mode	E_{FS}	—	±1	—	LSB[2]	$V_{ADIN} = V_{DDAD}$
	P		10 bit mode		—	±0.5	±1		
	T		8 bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12 bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10 bit mode		—	—	±0.5		
			8 bit mode		—	—	±0.5		
15	D	Input Leakage Error	12 bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10 bit mode		—	±0.2	±2.5		
			8 bit mode		—	±0.1	±1		

Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
16	D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	—
17	D	Temp Sensor Slope	–40 °C — 25 °C	m	—	3.266	—	mV/°C	—
			25 °C — 85 °C		—	3.638	—		

[1] Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

[2] 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

[3] Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

[4] Based on input pad leakage current. Refer to pad electricals.

2.10 External Oscillator (XOSC) Characteristics

Table 14. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	f_{lo} f_{hi} $f_{hi\text{-}hgo}$ $f_{hi\text{-}lp}$	32 1 1 1	— — — —	38.4 16 16 8	kHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer’s recommendation.			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		10 1	—	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	— — — — — —	0 100 0 0 0 0	— — — 0 10 20	kΩ
5	T	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[3]	$t_{CSTL\text{-}LP}$ $t_{CSTL\text{-}HGO}$ $t_{CSTH\text{-}LP}$ $t_{CSTH\text{-}HGO}$	— — — —	1500 2000 3 7	— — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode [2] FBE mode[2] FBELP mode	f_{extal}	0.03125 0 0	— — —	50.33 50.33 50.33	MHz

[1] Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

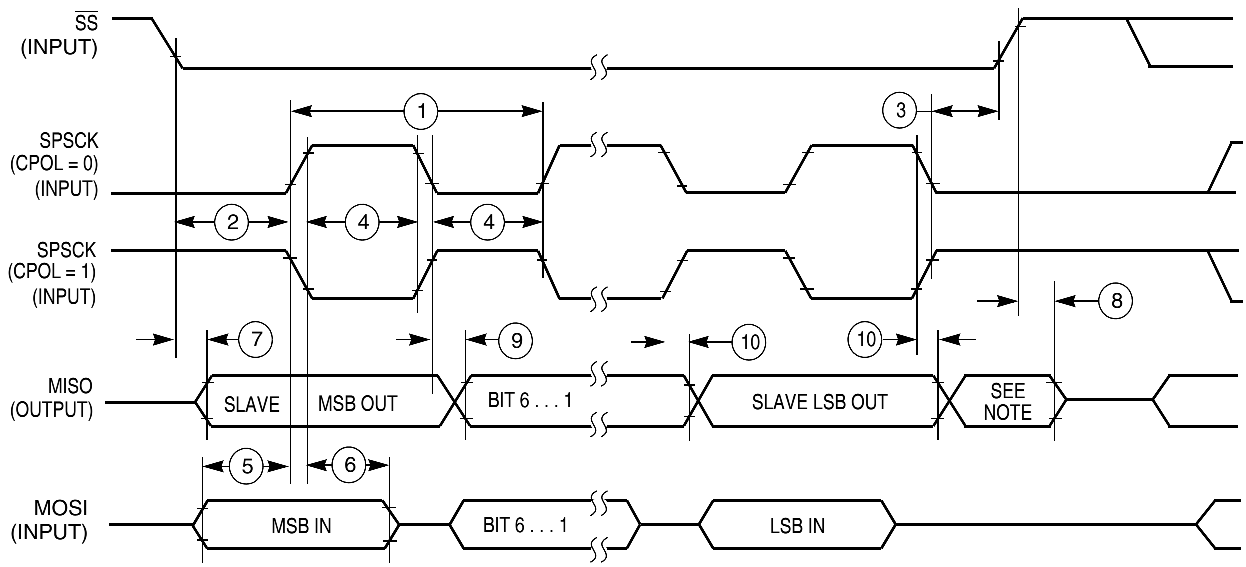
2.12.3 SPI Characteristics

Table 18 and Figure 15 through Figure 18 describe the timing requirements for the SPI system.

Table 18. SPI Timing Characteristics

No.	C	Function	Symbol	Min	Max	Unit
—	D	Operating frequency Master Slave	f_{op}	$f_{Bus}/2048$ 0	$f_{Bus}/2$ $f_{Bus}/4$	Hz
1	D	SPSCK period Master Slave	t_{SPSCK}	2 4	2048 —	t_{cyc} t_{cyc}
2	D	Enable lead time Master Slave	t_{Lead}	1/2 1	— —	t_{SPSCK} t_{cyc}
3	D	Enable lag time Master Slave	t_{Lag}	1/2 1	— —	t_{SPSCK} t_{cyc}
4	D	Clock (SPSCK) high or low time Master Slave	t_{WSPSCK}	$t_{cyc} - 30$ $t_{cyc} - 30$	1024 t_{cyc} —	ns ns
5	D	Data setup time (inputs) Master Slave	t_{SU}	30 30	— —	ns ns
6	D	Data hold time (inputs) Master Slave	t_{HI}	10 10	— —	ns ns
7	D	Slave access time	t_a	—	—	t_{cyc}
8	D	Slave MISO disable time	t_{dis}	—	—	t_{cyc}
9	D	Data valid time (maximum delay after SPCLK edge to Data output) Master Slave	t_V[1]	— —	25 70	ns ns
10	D	Data hold time (minimum delay after SPCLK edge to Data output) Master Slave	t_{HO}[1]	10 10	— —	ns ns

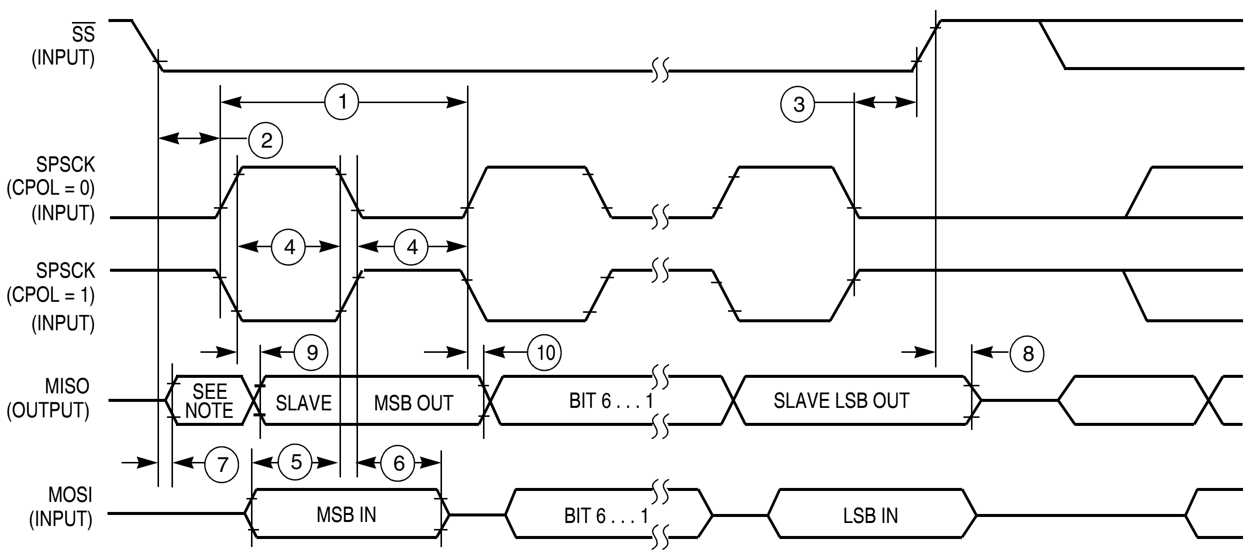
[1] SPI Output Load = 30 pf



NOTE:

1. Not defined but normally MSB of character just received

Figure 17. SPI Slave Timing (CPHA = 0)



NOTE:

1. Not defined but normally LSB of character just received

Figure 18. SPI Slave Timing (CPHA = 1)

2.13 Flash Specifications

This section provides details about program/erase times and program-erase endurance for the Flash memory.

Program and erase operations do not require any special power sources other than the normal V_{DD} supply. For more detailed information about program/erase operations, see *MCF51AG128 Reference Manual*.

MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
	PAGE: 840F
DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

△4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

△5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.

△6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.

△7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

△8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02	
	STANDARD: JEDEC MS-026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
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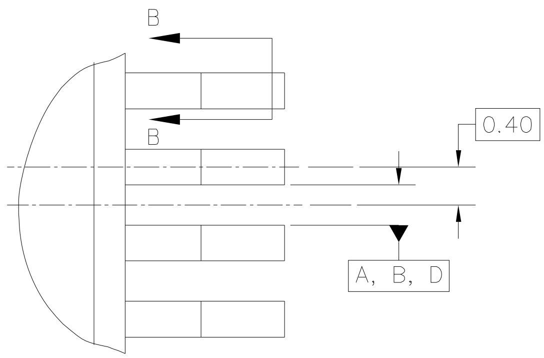
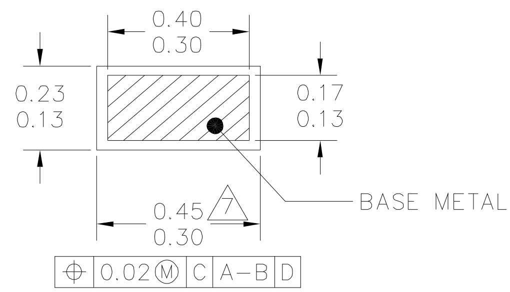
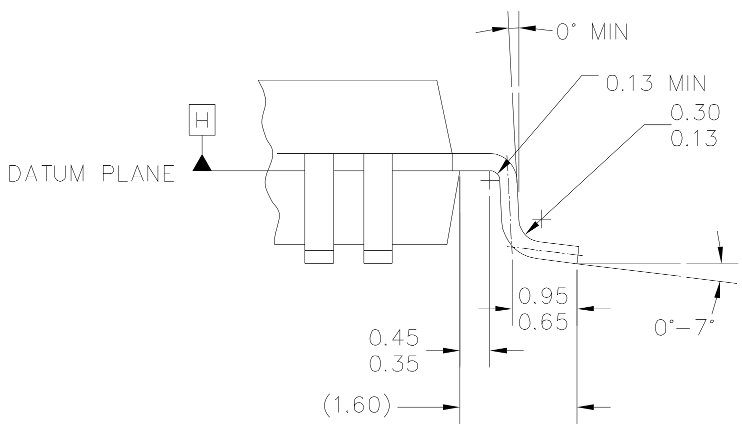


DETAIL "A"



VIEW ROTATED 90° CLOCKWISE

SECTION B–B



DETAIL "C"

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B–01	
	STANDARD: NON–JEDEC	
	PACKAGE CODE: 6057	SHEET: 2 OF 4

6 Revision History

Table 22. Revision History

Rev. No.	Date	Description
1	11/2008	Initial Draft Release.
2	4/2009	Internal Release.
3	5/2009	Alpha Customer Release.
4	12/2009	• Added 48-pin LQFP information; • Updated Section 2.5/17 and 2.6/21. • Provided the supply current in Section 2.7/23, and setup delay in Section 2.8/23.
5	6/2010	• Updated Table 10. • Added Figure 9. • Corrected pin names of PTG6 and PTG5 in 48-pin LQFP. • Standardized Generation 2008 Watchdog to Watchdog. • In Table 9, updated Output high/low voltage — Low Drive (PTxDSn = 0) 3 V, I_{Load} value.

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