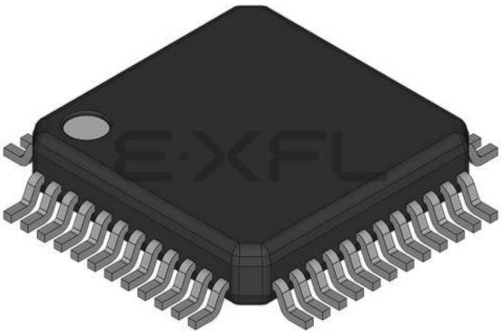


What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	39
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 12x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	48-LQFP
Supplier Device Package	48-LQFP (7x7)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag96vlf

Table of Contents

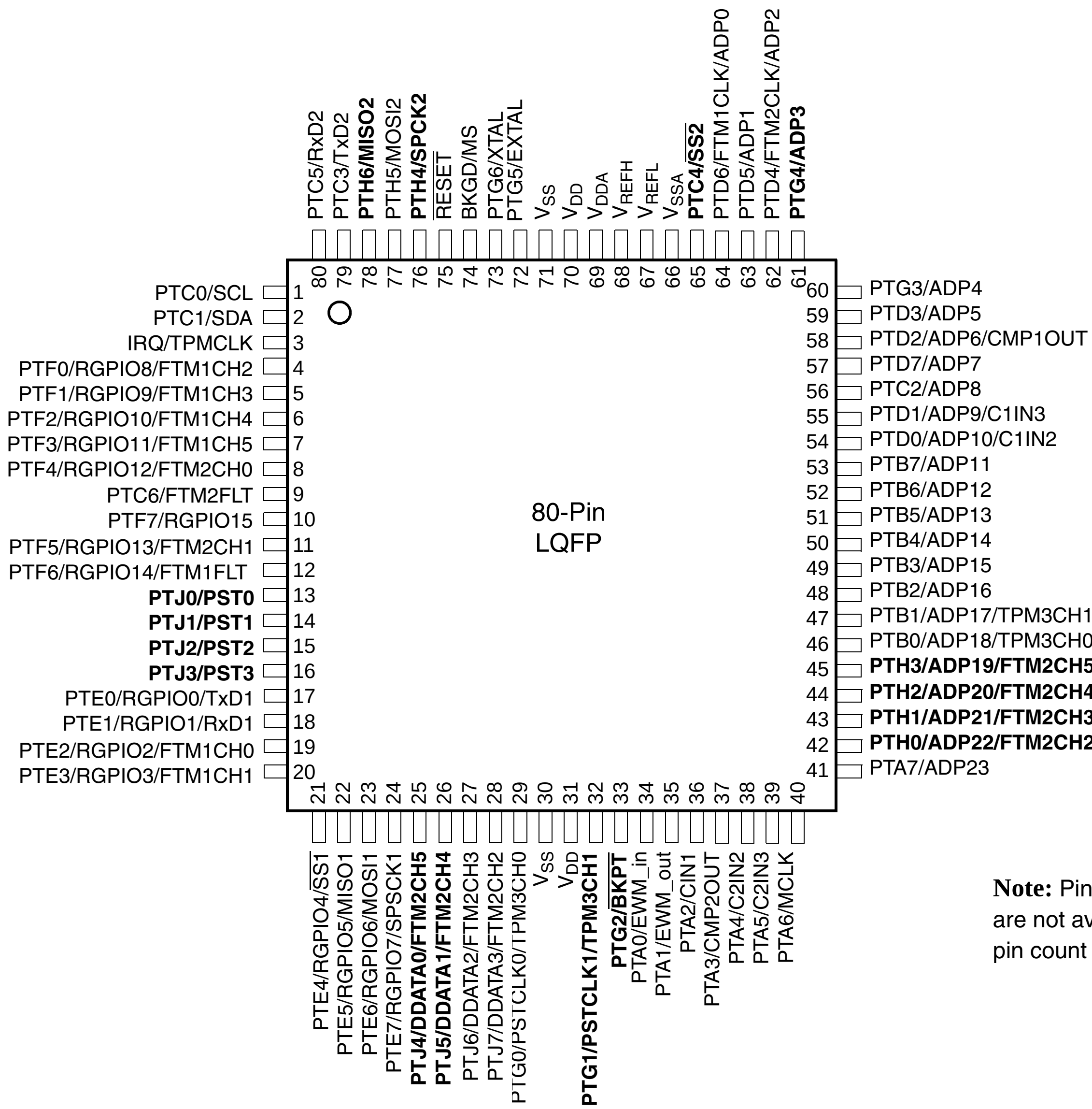
List of Tables

List of Figures

1.4 Pin Assignments

This section describes the pin assignments for the available packages.

Figure 2 shows the pinout of the 80-pin LQFP.



Note: Pin names in **bold** are not available in lower pin count packages.

Figure 2. 80-Pin LQFP

Table 5. Absolute Maximum Ratings

Rating	Symbol	Value	Unit
Supply voltage	V_{DD}	–0.3 to 5.8	V
Input voltage	V_{In}	–0.3 to V_{DD} + 0.3	V
Instantaneous maximum current Single pin limit (applies to all port pins)[1, 2, 3]	I_D	±25	mA
Maximum current into V_{DD}	I_{DD}	120	mA
Storage temperature	T_{stg}	–55 to 150	°C

1 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive (V_{DD}) and negative (V_{SS}) clamp voltages, then use the larger of the two resistance values.

2 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

3 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if the clock rate is very low which would reduce overall power consumption.

2.3 Thermal Characteristics

This section provides information about operating temperature range, power dissipation, and package thermal resistance. Power dissipation on I/O pins is usually small compared to the power dissipation in on-chip logic and it is user-determined rather than being controlled by the MCU design. To take $P_{I/O}$ into account in power calculations, determine the difference between actual pin voltage and V_{SS} or V_{DD} and multiply by the pin current for each I/O pin. Except in cases of unusually high pin current (heavy loads), the difference between pin voltage and V_{SS} or V_{DD} is very small.

Table 6. Thermal Characteristics

Rating	Symbol	Value	Unit
Operating temperature range (packaged)	T_A	–40 to 105	°C
Maximum junction temperature	T_J	150	°C
Thermal resistance [1,2,3,4]	θ_{JA}		°C/W
80-pin LQFP			
1s		56	
2s2p		45	
64-pin QFP			
1s		54	
2s2p		41	
64-pin LQFP			
1s		67	
2s2p		49	
48-pin LQFP			
1s		69	
2s2p		51	

[1] Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
[2] Junction to Ambient Natural Convection
[3] 1s — Single layer board, one signal layer
[4] 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C
θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W
$P_D = P_{int} + P_{I/O}$
$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power
$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—

Table 7. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	±500	—	V
3	Latch-up Current at T_A = 85°C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –5 mA 3 V, I_{Load} = –1.5 mA 5V, I_{Load} = –3 mA, PTC0 and PTC1 3V, I_{Load} = –1.5 mA, PTC0 and PTC1	V_{OH}	 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.4 V_{DD} – 0.4	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –20 mA 3 V, I_{Load} = –8 mA 5V, I_{Load} = –12 mA, PTC0 and PTC1 3V, I_{Load} = –8 mA, PTC0 and PTC1		 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.4 V_{DD} – 0.4	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 1.5 mA 5V, I_{Load} = 3 mA, PTC0 and PTC1 3V, I_{Load} = 1.5 mA, PTC0 and PTC1	V_{OL}	 — — — —	 — — — —	 1.5 0.8 0.4 0.4	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 20 mA 3 V, I_{Load} = 8 mA 5V, I_{Load} = 12 mA, PTC0 and PTC1 3V, I_{Load} = 8 mA, PTC0 and PTC1		 — — — —	 — — — —	 1.5 0.8 0.4 0.4	
4	C	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	C	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	 — —	 — —	 100 60	mA

Table 9. DC Characteristics (continued)

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
6	P	Input high voltage; all digital inputs	V_{IH}	$0.65 \times V_{DD}$	—	—	V
7	P	Input low voltage; all digital inputs	V_{IL}	—	—	$0.35 \times V_{DD}$	
8	D	Input hysteresis; all digital inputs	V_{hys}	$0.06 \times V_{DD}$	—	—	mV
9	P	Input leakage current; input only pins[2]	$\|I_{In}\|$	—	0.1	1	μA
10	P	High Impedance (off-state) leakage current[2]	$\|I_{OZ}\|$	—	0.1	1	μA
11	P	Internal pullup resistors[3] Internal pullup resistorsPTC0 and PTC1	R_{PU}	20 10	45 22	65 32	kΩ
12	P	Internal pulldown resistors[4]	R_{PD}	20	45	65	kΩ
13	C	Input Capacitance; all non-supply pins	C_{In}	—	—	8	pF
14	P	POR rearm voltage	V_{POR}	0.9	1.4	2.0	V
15	D	POR rearm time	t_{POR}	10	—	—	μs
16	P	Low-voltage detection threshold — high range V_{DD} falling V_{DD} rising	V_{LVD1}	3.9 4.0	4.0 4.1	4.1 4.2	V
17	P	Low-voltage detection threshold — low range V_{DD} falling V_{DD} rising	V_{LVD0}	2.48 2.54	2.56 2.62	2.64 2.70	V
18	P	Low-voltage warning threshold — high range 1 V_{DD} falling V_{DD} rising	V_{LVW3}	4.5 4.6	4.6 4.7	4.7 4.8	V
19	P	Low-voltage warning threshold — high range 0 V_{DD} falling V_{DD} rising	V_{LVW2}	4.2 4.3	4.3 4.4	4.4 4.5	V
20	P	Low-voltage warning threshold low range 1 V_{DD} falling V_{DD} rising	V_{LVW1}	2.84 2.90	2.92 2.98	3.00 3.06	V
21	P	Low-voltage warning threshold — low range 0 V_{DD} falling V_{DD} rising	V_{LVW0}	2.66 2.72	2.74 2.80	2.82 2.88	V
22	T	Low-voltage inhibit reset/recover hysteresis 5 V 3 V	V_{hys}	— —	100 60	— —	mV
23	D	RAM retention voltage	V_{RAM}	—	0.6	1.0	V
24	D	DC injection current[5 6 7 8] (single pin limit) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$	I_{IC}	0 0	— —	2 –0.2	mA
		DC injection current (Total MCU limit, includes sum of all stressed pins) $V_{IN} > V_{DD}$ $V_{IN} < V_{SS}$		0 0	— —	25 –5	mA

1 Typical values are based on characterization data at 25°C unless otherwise stated.

2 Measured with $V_{In} = V_{DD}$ or V_{SS}.

3 Measured with $V_{In} = V_{SS}$.

4 Measured with $V_{In} = V_{DD}$.

5 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{In} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Ensure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low (which would reduce overall power consumption).

6 All functional non-supply pins are internally clamped to V_{SS} and V_{DD}.

7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.

8 The $\overline{\text{RESET}}$ pin does not have a clamp diode to V_{DD}. Do not drive this pin above V_{DD}.

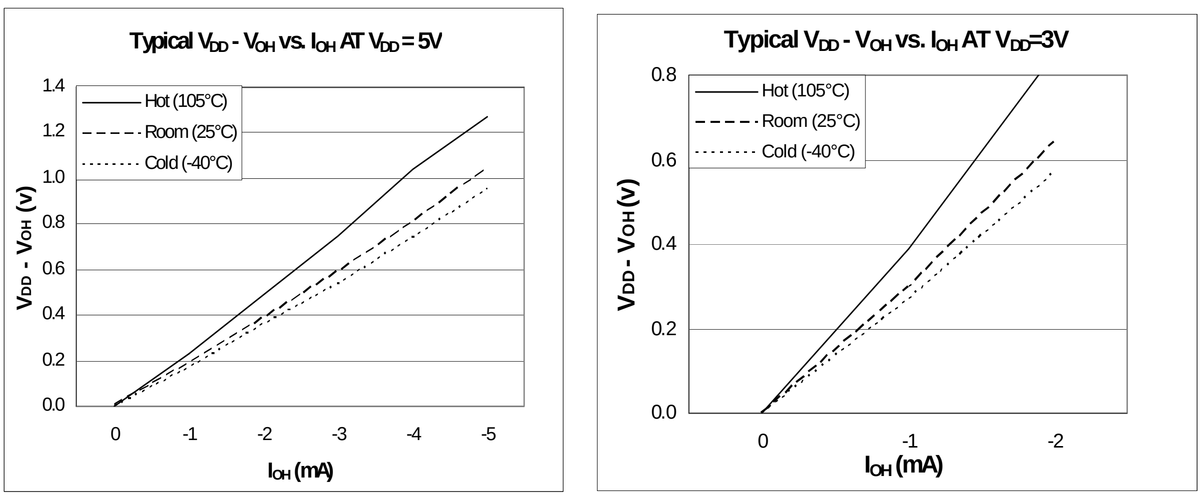


Figure 5. Typical I_{OH} vs. $V_{DD} – V_{OH}$ (Low Drive,PTxDSn = 0)

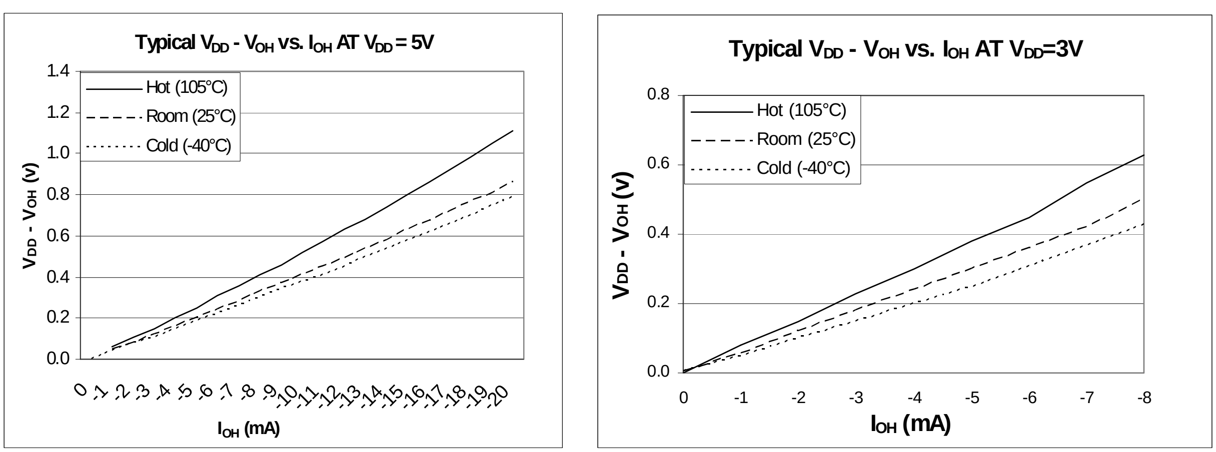


Figure 6. Typical I_{OH} vs. $V_{DD} – V_{OH}$ (High Drive, PTxDSn = 1)

2.7 High Speed Comparator (HSCMP) Electricals

Table 11. HSCMP Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current, high speed mode (EN = 1, PMODE = 1)	I_{DDAHS}	—	200	—	µA
3	T	Supply current, low speed mode (EN = 1, PMODE = 0)	I_{DDALS}	—	20	—	µA
4	—	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
5	D	Analog input offset voltage	V_{AIO}	—	5	40	mV
6	D	Analog Comparator hysteresis	V_H	3.0	9.0	20.0	mV
7	D	Propagation delay, high speed mode (EN = 1, PMODE = 1)	t_{DHS}	—	70	120	ns
8	D	Propagation delay, low speed mode (EN = 1, PMODE = 0)	t_{DLS}	—	400	600	ns
9	D	Analog Comparator initialization delay	t_{AINIT}	—	400	—	ns

2.8 Digital to Analog (DAC) Characteristics

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DDA}	2.7	—	5.5	V
2	D	Supply current (enabled)	I_{DDAC}	—	—	20	µA
3	D	Supply current (stand-by)	I_{DDACS}	—	—	150	nA
4	D	DAC reference input voltage	V_{in1}, V_{in2}	V_{SSA}	—	V_{DDA}	V
5	D	DAC setup delay	t_{PRGST}	—	1000	—	nS
6	D	DAC step size	V_{step}	$3V_{in}/128$	$V_{in}/32$	$5V_{in}/128$	V
7	D	DAC output voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.9 ADC Characteristics

Table 12. 5V 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
			Delta to V_{DD} $(V_{DD}–V_{DDA})^2$	ΔV_{DDA}	–100	0	100	mV	—
2	D	Ground voltage	Delta to V_{SS} $(V_{SS}–V_{SSA})^2$	ΔV_{SSA}	–100	0	100	mV	—

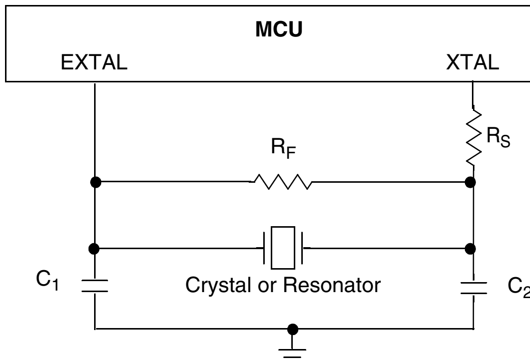
Table 13. 5 V 12-bit ADC Characteristics ($V_{REFH} = V_{DDA}$, $V_{REFL} = V_{SSA}$) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC = 1)		1.25	2	3.3		
7	P	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long Sample (ADLSMP = 1)		—	40	—		
8	T	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long Sample (ADLSMP = 1)		—	23.5	—		
9	T	Total Unadjusted Error	12 bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	P		10 bit mode		—	±1	±2.5		
	T		8 bit mode		—	±0.5	±1.0		
10	T	Differential Non-Linearity	12 bit mode	DNL	—	±1.75	—	LSB[2]	—
	P		10 bit mode[3]		—	±0.5	±1.0		
	T		8 bit mode[5]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12 bit mode	INL	—	±1.5	—	LSB[2]	—
	P		10 bit mode		—	±0.5	±1.0		
	T		8 bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12 bit mode	E_{ZS}	—	±1.5	—	LSB[2]	$V_{ADIN} = V_{SSAD}$
	P		10 bit mode		—	±0.5	±1.5		
	T		8 bit mode		—	±0.5	±0.5		
13	T	Full-Scale Error	12 bit mode	E_{FS}	—	±1	—	LSB[2]	$V_{ADIN} = V_{DDAD}$
	P		10 bit mode		—	±0.5	±1		
	T		8 bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12 bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10 bit mode		—	—	±0.5		
			8 bit mode		—	—	±0.5		
15	D	Input Leakage Error	12 bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10 bit mode		—	±0.2	±2.5		
			8 bit mode		—	±0.1	±1		

[2] When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

[3] This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

[4] 4 MHz crystal



2.11 ICS Specifications

Table 15. ICS Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	μs
4	C	DCO output frequency range - untrimmed [2]	Low range (DRS = 00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	C		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS = 01)		—	33.69	—	
	P		High range (DRS = 10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over full voltage and temperature range		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 –70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$

Table 15. ICS Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
10	D	FLL acquisition time [3]	$t_{fll\_acquire}$	—	—	1	ms
11	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
12	D	Loss of external clock minimum freq. (RANGE = 0) • ext. clock freq: above $(3/5)f_{int}$, never reset • ext. clock freq: between $(2/5)f_{int}$ and $(3/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(2/5)f_{int}$, always reset	f_{loc_low}	$(3/5) \times f_{int}$	—	—	kHz
13	D	Loss of external clock minimum freq. (RANGE = 1) • ext. clock freq: above $(16/5)f_{int}$, never reset • ext. clock freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(15/5)f_{int}$, always reset	f_{loc_high}	$(16/5) \times f_{int}$	—	—	kHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry by V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

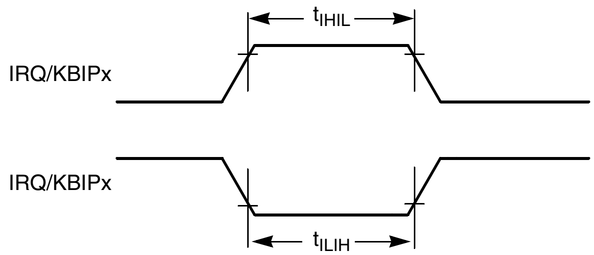


Figure 12. IRQ/KBIPx Timing

2.12.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 17. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

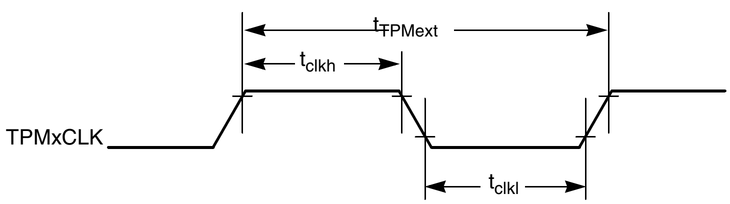


Figure 13. Timer External Clock

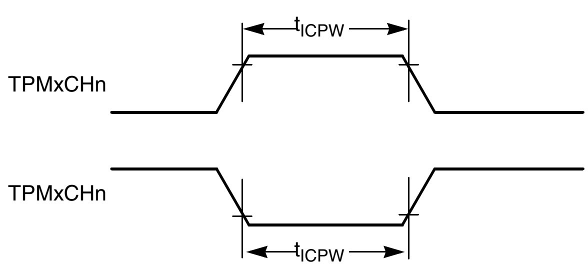
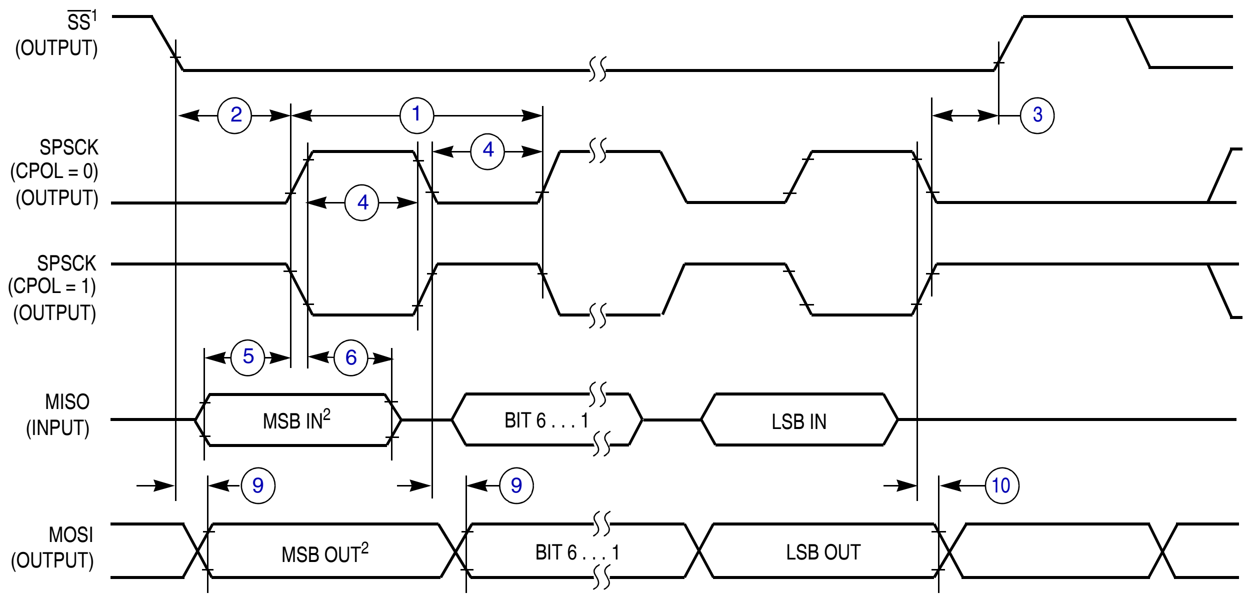
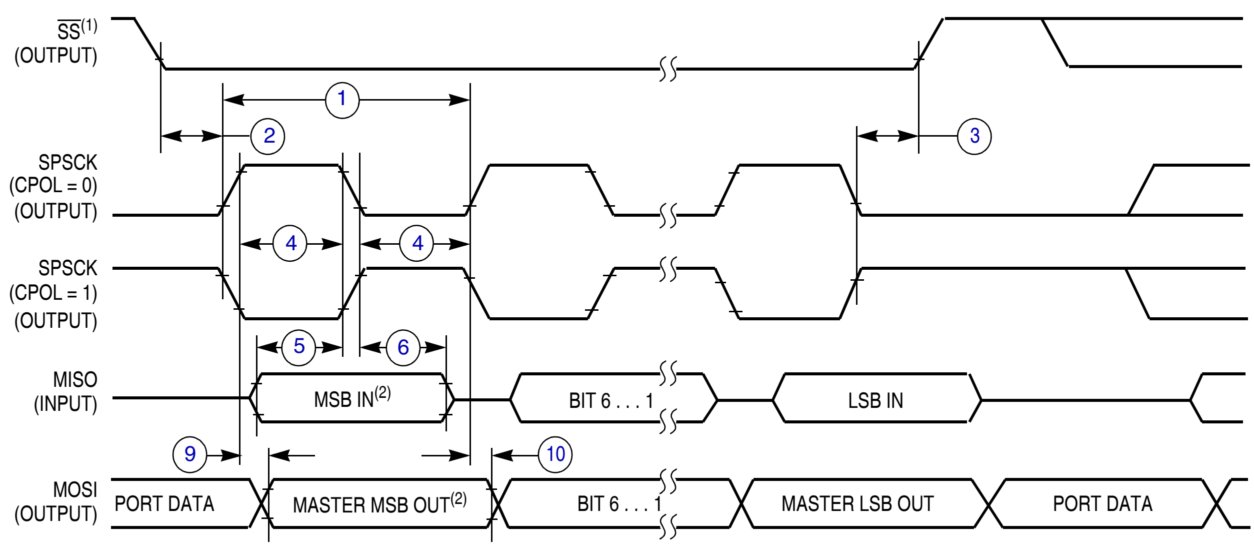


Figure 14. Timer Input Capture Pulse



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:
1. SS output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA = 1)

3 Ordering Information

This section contains ordering information for MCF51AG128 devices.

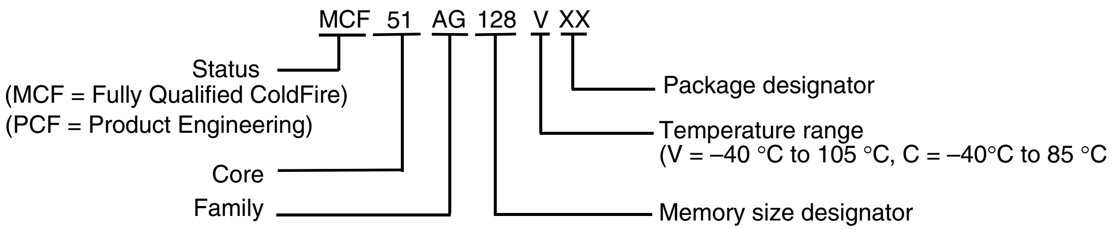


Table 20. Orderable Part Number Summary

Freescale Part Number	Description	Flash / SRAM (KB)	Package	Temperature
MCF51AG128VLK	MCF51AG128 ColdFire Microcontroller	128 / 16	80 LQFP	–40°C to 105°C
MCF51AG128VLH	MCF51AG128 ColdFire Microcontroller	128 / 16	64 LQFP	–40°C to 105°C
MCF51AG128VQH	MCF51AG128 ColdFire Microcontroller	128 / 16	64 QFP	–40°C to 105°C
MCF51AG128VLF	MCF51AG128 ColdFire Microcontroller	128 / 16	48 LQFP	–40°C to 105°C
MCF51AG96VLK	MCF51AG96 ColdFire Microcontroller	96 / 16	80 LQFP	–40°C to 105°C
MCF51AG96VLH	MCF51AG96 ColdFire Microcontroller	96 / 16	64 LQFP	–40°C to 105°C
MCF51AG96VQH	MCF51AG96 ColdFire Microcontroller	96 / 16	64 QFP	–40°C to 105°C
MCF51AG96VLF	MCF51AG96 ColdFire Microcontroller	96 / 16	48 LQFP	–40°C to 105°C

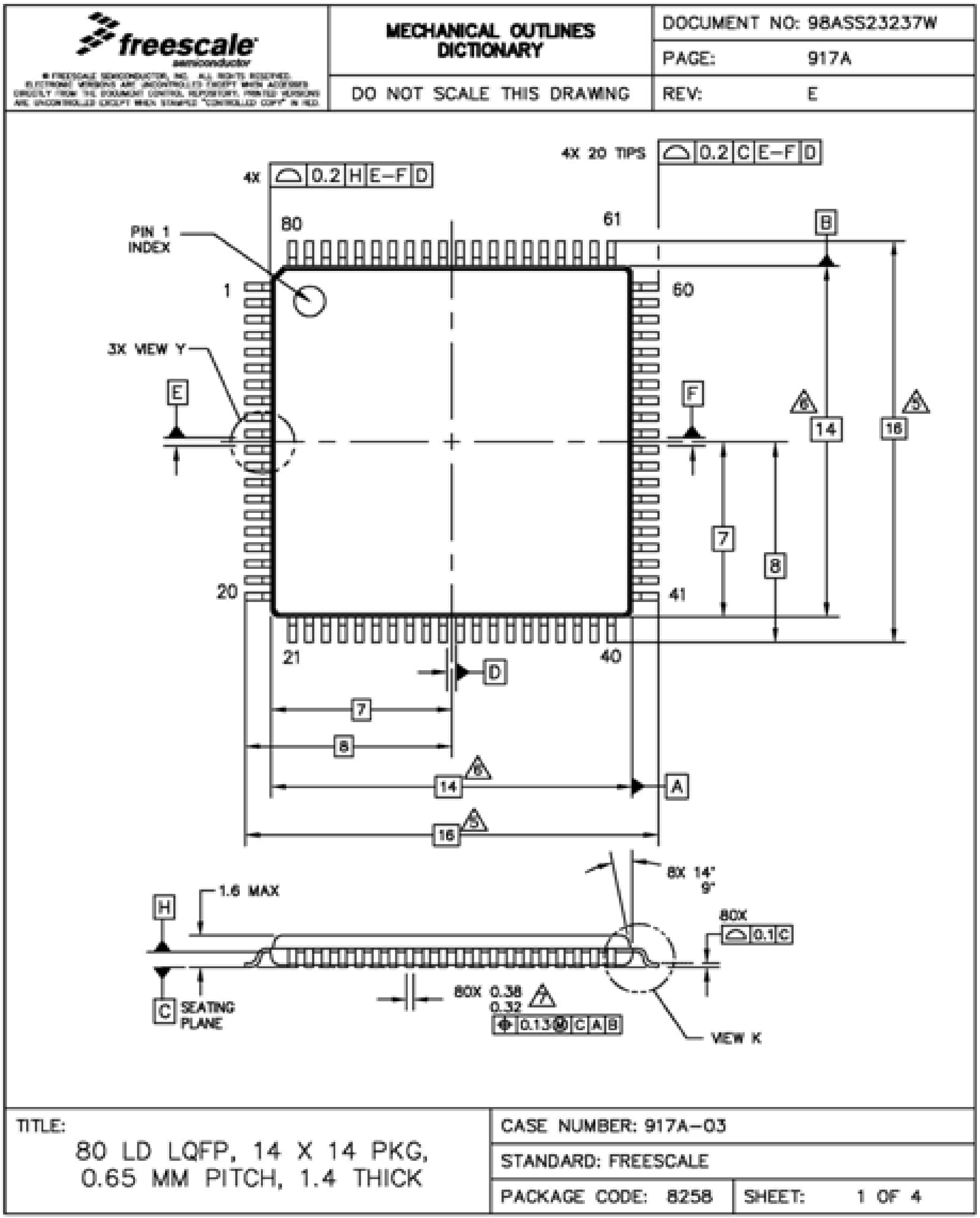
4 Package Information

Table 21. Package Descriptions

Pin Count	Package Type	Abbreviation	Designator	Case No.	Document No.
80	Low Quad Flat Package	LQFP	LK	917A	98ASS23237W
64	Low Quad Flat Package	LQFP	LH	840F	98ASS23234W
64	Quad Flat Package	QFP	QH	840B	98ASB42844B
48	Low Quad Flat Package	LQFP	LF	932	98ASH00962A

5 Mechanical Outline Drawings

5.1 80-pin LQFP Package



freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23237W
		PAGE: 917A
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M−1994.
2. CONTROLLING DIMENSION : MILIMETER.
3. DATUM PLANE H IS LOCATED AT THE BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUM E, F AND D TO BE DETERMINED AT DATUM PLANE H.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE H.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07.

TITLE: 80 LD LQFP, 14 X 14 PKG, 0.65 MM PITCH, 1.4 THICK	CASE NUMBER: 917A−03	
	STANDARD: FREESCALE	
	PACKAGE CODE: 8258	SHEET: 3 OF 4

freescale semiconductor 	**MECHANICAL OUTLINES DICTIONARY**	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

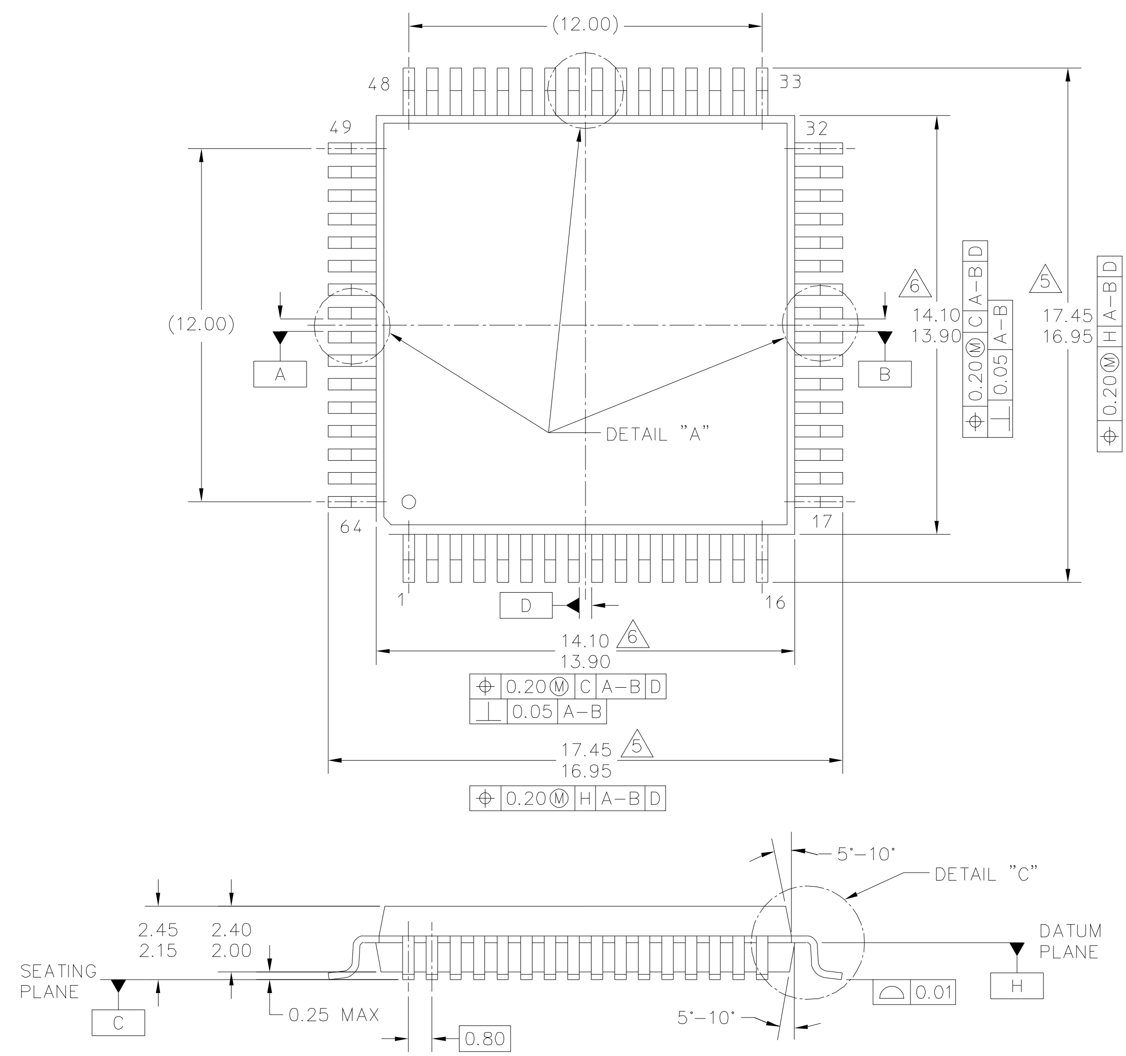
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. (△) DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. (△) THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. (△) THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. (△) EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. (△) THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F-02	
	STANDARD: JEDEC MS-026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

5.3 64-pin QFP Package

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED. ELECTRONIC VERSIONS ARE UNCONTROLLED EXCEPT WHEN ACCESSED DIRECTLY FROM THE DOCUMENT CONTROL REPOSITORY. PRINTED VERSIONS ARE UNCONTROLLED EXCEPT WHEN STAMPED "CONTROLLED COPY" IN RED.	DO NOT SCALE THIS DRAWING	REV: B



TITLE:	CASE NUMBER: 840B-01	
64LD QFP (14 X 14)	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 1 OF 4

freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASB42844B
		PAGE: 840B
	DO NOT SCALE THIS DRAWING	REV: B

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DATUM PLANE -H- IS LOCATED AT BOTTOM OF LEAD AND IS COINCIDENT WITH THE LEAD WHERE THE LEAD EXITS THE PLASTIC BODY AT THE BOTTOM OF THE PARTING LINE.
4. DATUMS A-B AND -D- TO BE DETERMINED AT DATUM PLANE -H-.
5. DIMENSIONS TO BE DETERMINED AT SEATING PLANE -C-.
6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25mm PER SIDE. DIMENSIONS DO INCLUDE MOLD MISMATCH AND ARE DETERMINED AT DATUM PLANE -H-.
7. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF THE DIMENSION AT MAXIMUM MATERIAL CONDICTION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT.

TITLE: 64LD QFP (14 X 14)	CASE NUMBER: 840B-01	
	STANDARD: NON-JEDEC	
	PACKAGE CODE: 6057	SHEET: 3 OF 4

THIS PAGE INTENTIONALLY BLANK