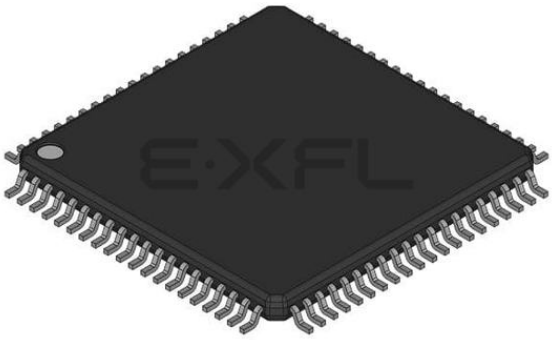

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	Coldfire V1
Core Size	32-Bit Single-Core
Speed	50MHz
Connectivity	I²C, SCI, SPI
Peripherals	DMA, LVD, PWM, WDT
Number of I/O	69
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.6V
Data Converters	A/D 24x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 105°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mcf51ag96vlk

1 MCF51AG128 Family Configurations

1.1 Device Comparison

The following table compares the various device derivatives available within the MCF51AG128 series MCUs.

Table 1. MCF51AG128 Series Device Comparison

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
Flash memory size (KB)	128			96		
RAM size (KB)	16					
ColdFire V1 core with BDM (background debug module)	Yes					
HSCMP (analog comparator)	2	2	1	2	2	1
ADC (analog-to-digital converter) channels (12-bit)	24	19	12	24	19	12
CRC (cyclic redundancy check)	Yes					
DAC	2	2	1	2	2	1
DMA controller	4-ch					
iEvent (intelligent Event module)	Yes					
EWM (External Watchdog Monitor)	Yes					
WDOG (Watchdog timer)	Yes					
RTC	Yes					
DBG (debug module)	Yes					
IIC (inter-integrated circuit)	1	1	No	1	1	No
IRQ (interrupt request input)	Yes					
INTC (interrupt controller)	Yes					
LVD (low-voltage detector)	Yes					
ICS (internal clock source)	Yes					
OSC (crystal oscillator)	Yes					
Port I/O[1]	69	53	39	69	53	39
RGPIO (rapid general-purpose I/O)	16	16	15	16	16	15
SCI (serial communications interface)	2					
SPI1 (serial peripheral interface)	Yes					
SPI2 (serial peripheral interface)	Yes	No	No	Yes	No	No
FTM1 (flexible timer module) channels	6[2]					
FTM2 channels	6[2]					

Table 1. MCF51AG128 Series Device Comparison (continued)

Feature	MCF51AG128			MCF51AG96		
	80-pin	64-pin	48-pin	80-pin	64-pin	48-pin
TPM3 (timer pulse-width modulator) channels	2					
Debug Visibility Bus	Yes	No	No	Yes	No	No

[1] Up to 16 pins on Ports E and F are shared with the ColdFire Rapid GPIO module.

[2] Some pins of FTMx might not be bonded on small package, therefore these channels could be used as soft timer only.

1.2 Block Diagram

Figure 1 shows the connections between the MCF51AG128 series pins and modules.

[1] TPMCLK, FTM1CLK, and FTM2CLK options are configured via software; out of reset, FTM1CLK, FTM2CLK, and TPMCLK are available to FTM1, FTM2, and TPM3 respectively.

2 Preliminary Electrical Characteristics

This section contains electrical specification tables and reference timing diagrams for the MCF51AG128 series MCUs, including detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle. These specifications will, however, be met for production silicon. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this data sheet supersede any values found in the module specifications.

2.1 Parameter Classification

The electrical parameters shown in this supplement are guaranteed by various methods. To give the customer a better understanding the following classification is used and the parameters are tagged accordingly in the tables where appropriate:

Table 4. Parameter Classifications

P	Those parameters are guaranteed during production testing on each individual device.
C	Those parameters are achieved by the design characterization by measuring a statistically relevant sample size across process variations.
T	Those parameters are achieved by design characterization on a small sample size from typical devices under typical conditions unless otherwise noted. All values shown in the typical column are within this category.
D	Those parameters are derived mainly from simulations.

NOTE

The classification is shown in the column labeled “C” in the parameter tables where appropriate.

2.2 Absolute Maximum Ratings

Absolute maximum ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond the limits specified in Table 5 may affect device reliability or cause permanent damage to the device. For functional operating conditions, refer to the remaining tables in this section.

This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (for instance, either V_{SS} or V_{DD}).

1 Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.

2 Junction to Ambient Natural Convection

3 1s — Single layer board, one signal layer

4 2s2p — Four layer board, 2 signal and 2 power layers

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad \textit{Eqn. 1}$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction-to-ambient, °C/W

$P_D = P_{int} + P_{I/O}$

$P_{int} = I_{DD} \times V_{DD}$, Watts — chip internal power

$P_{I/O}$ = Power dissipation on input and output pins — user determined

For most applications, $P_{I/O} << P_{int}$ and can be neglected. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad \textit{Eqn. 2}$$

Solving Equation 1 and Equation 2 for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad \textit{Eqn. 3}$$

where K is a constant pertaining to the particular part. K can be determined from Equation 3 by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving Equation 1 and Equation 2 iteratively for any value of T_A.

2.4 Electrostatic Discharge (ESD) Protection Characteristics

Although damage from static discharge is much less common on these devices than on early CMOS circuits, normal handling precautions should be used to avoid exposure to static discharge. Qualification tests are performed to ensure that these devices can withstand exposure to reasonable levels of static without suffering any permanent damage.

All ESD testing is in conformity with CDF-AEC-Q00 Stress Test Qualification for Automotive Grade Integrated Circuits. (http://www.aecouncil.com/) This device was qualified to AEC-Q100 Rev E.

A device is considered to have failed if, after exposure to ESD pulses, the device no longer meets the device specification requirements. Complete dc parametric and functional testing is performed per the applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

Table 7. ESD and Latch-up Test Conditions

Model	Description	Symbol	Value	Unit
Human Body	Series Resistance	R1	1500	Ω
	Storage Capacitance	C	100	pF
	Number of Pulse per pin	—	3	—

Table 7. ESD and Latch-up Test Conditions (continued)

Model	Description	Symbol	Value	Unit
Latch-up	Minimum input voltage limit	—	–2.5	V
	Maximum input voltage limit	—	7.5	V

Table 8. ESD and Latch-Up Protection Characteristics

Num	Rating	Symbol	Min	Max	Unit
1	Human Body Model (HBM)	V_{HBM}	±2000	—	V
2	Charge Device Model (CDM)	V_{CDM}	±500	—	V
3	Latch-up Current at T_A = 85°C	I_{LAT}	±100	—	mA

2.5 DC Characteristics

This section includes information about power supply requirements, I/O pin characteristics, and power supply current in various operating modes.

Table 9. DC Characteristics

Num	C	Parameter	Symbol	Min	Typical[1]	Max	Unit
1	—	Operating voltage		2.7	—	5.5	V
2	P	Output high voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = –5 mA 3 V, I_{Load} = –1.5 mA 5V, I_{Load} = –3 mA, PTC0 and PTC1 3V, I_{Load} = –1.5 mA, PTC0 and PTC1	V_{OH}	 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.4 V_{DD} – 0.4	 — — — —	 — — — —	V
		Output high voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = –20 mA 3 V, I_{Load} = –8 mA 5V, I_{Load} = –12 mA, PTC0 and PTC1 3V, I_{Load} = –8 mA, PTC0 and PTC1		 V_{DD} – 1.5 V_{DD} – 0.8 V_{DD} – 0.4 V_{DD} – 0.4	 — — — —	 — — — —	
3	P	Output low voltage — Low Drive (PTxDSn = 0) 5 V, I_{Load} = 5 mA 3 V, I_{Load} = 1.5 mA 5V, I_{Load} = 3 mA, PTC0 and PTC1 3V, I_{Load} = 1.5 mA, PTC0 and PTC1	V_{OL}	 — — — —	 — — — —	 1.5 0.8 0.4 0.4	V
		Output low voltage — High Drive (PTxDSn = 1) 5 V, I_{Load} = 20 mA 3 V, I_{Load} = 8 mA 5V, I_{Load} = 12 mA, PTC0 and PTC1 3V, I_{Load} = 8 mA, PTC0 and PTC1		 — — — —	 — — — —	 1.5 0.8 0.4 0.4	
4	C	Output high current — Max total I_{OH} for all ports 5V 3V	I_{OHT}	 — —	 — —	 100 60	mA
5	C	Output low current — Max total I_{OL} for all ports 5 V 3 V	I_{OLT}	 — —	 — —	 100 60	mA

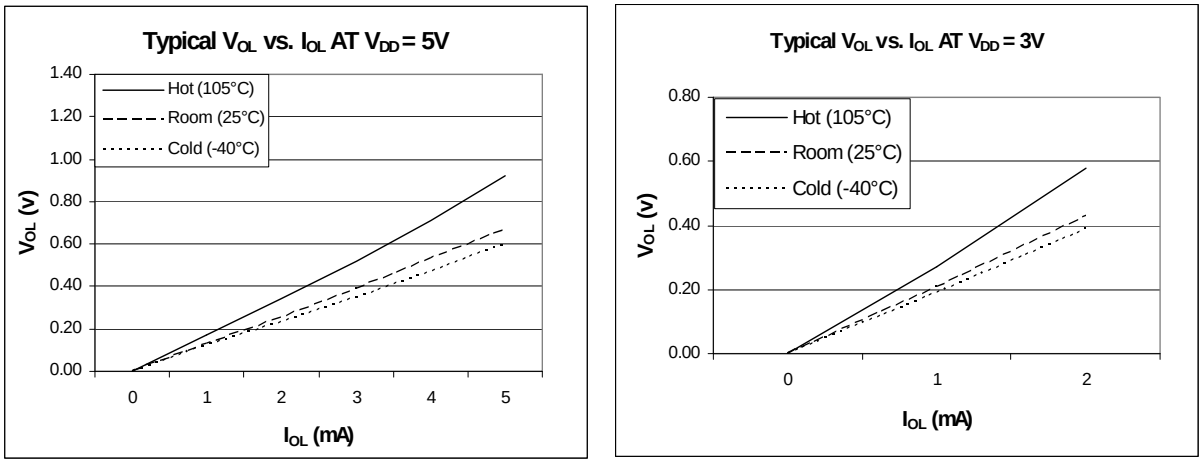


Figure 7. Typical I_{OL} vs. V_{OL} (Low Drive, PTxDSn = 0)

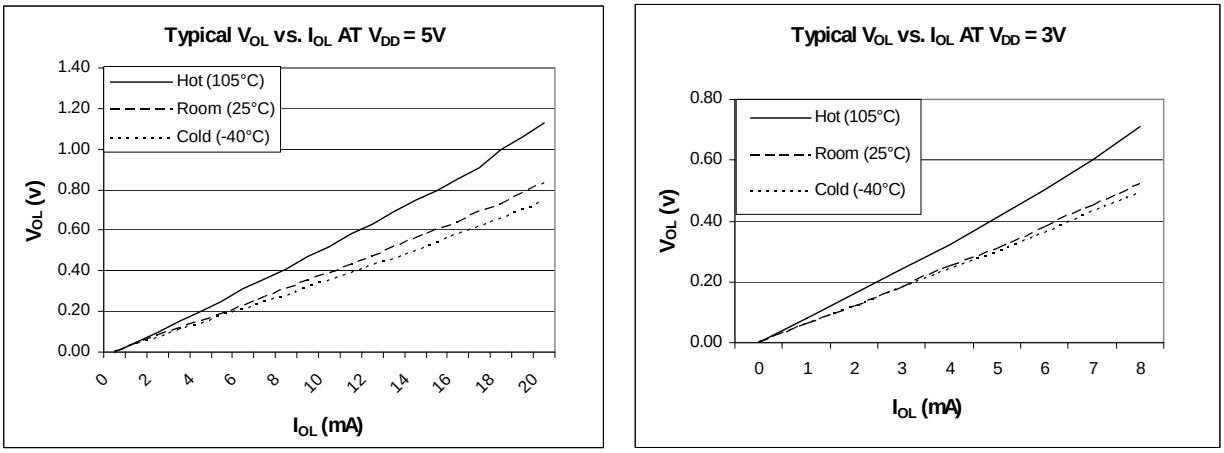


Figure 8. Typical I_{OL} vs. V_{OL} (High Drive, PTxDSn = 1)

2.7 High Speed Comparator (HSCMP) Electricals

Table 11. HSCMP Electrical Specifications

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	—	Supply voltage	V_{DD}	2.7	—	5.5	V
2	T	Supply current, high speed mode (EN = 1, PMODE = 1)	I_{DDAHS}	—	200	—	μA
3	T	Supply current, low speed mode (EN = 1, PMODE = 0)	I_{DDALS}	—	20	—	μA
4	—	Analog input voltage	V_{AIN}	V_{SS} – 0.3	—	V_{DD}	V
5	D	Analog input offset voltage	V_{AIO}	—	5	40	mV
6	D	Analog Comparator hysteresis	V_H	3.0	9.0	20.0	mV
7	D	Propagation delay, high speed mode (EN = 1, PMODE = 1)	t_{DHS}	—	70	120	ns
8	D	Propagation delay, low speed mode (EN = 1, PMODE = 0)	t_{DLS}	—	400	600	ns
9	D	Analog Comparator initialization delay	t_{AINIT}	—	400	—	ns

2.8 Digital to Analog (DAC) Characteristics

Num	C	Rating	Symbol	Min	Typical	Max	Unit
1	D	Supply voltage	V_{DDA}	2.7	—	5.5	V
2	D	Supply current (enabled)	I_{DDAC}	—	—	20	μA
3	D	Supply current (stand-by)	I_{DDACS}	—	—	150	nA
4	D	DAC reference input voltage	V_{in1}, V_{in2}	V_{SSA}	—	V_{DDA}	V
5	D	DAC setup delay	t_{PRGST}	—	1000	—	nS
6	D	DAC step size	V_{step}	$3V_{in}/128$	$V_{in}/32$	$5V_{in}/128$	V
7	D	DAC output voltage range	V_{dacout}	$V_{in}/32$	—	V_{in}	V
8	P	Bandgap voltage reference factory trimmed at V_{DD} = 5 V, Temp = 25 °C	V_{BG}	1.18	1.20	1.21	V

2.9 ADC Characteristics

Table 12. 5V 12-bit ADC Operating Conditions

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
1	D	Supply voltage	Absolute	V_{DDA}	2.7	—	5.5	V	—
			Delta to V_{DD} (V_{DD}–V_{DDA})[2]	ΔV_{DDA}	–100	0	100	mV	—
2	D	Ground voltage	Delta to V_{SS} (V_{SS}–V_{SSA})[2]	ΔV_{SSA}	–100	0	100	mV	—

Table 12. 5V 12-bit ADC Operating Conditions (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
3	D	Ref Voltage High	—	V_{REFH}	2.7	V_{DDA}	V_{DDA}	V	—
4	D	Ref Voltage Low	—	V_{REFL}	V_{SSAD}	V_{SSA}	V_{SSA}	V	—
5	D	Input Voltage	—	V_{ADIN}	V_{REFL}	—	V_{REFH}	V	—
6	C	Input Capacitance	—	C_{ADIN}	—	4.5	5.5	pF	—
7	C	Input Resistance	—	R_{ADIN}	—	3	5	kΩ	—
8	C	Analog Source Resistance	12 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz	R_{AS}	 — —	 — —	 2 5	kΩ	External to MCU
	C		10 bit mode f_{ADCK} > 4 MHz f_{ADCK} < 4 MHz		 — —	 — —	 5 10		
	C		8 bit mode (all valid f_{ADCK})		—	—	10		
9	D	ADC Conversion Clock Freq.	High Speed (ADLPC = 0)	f_{ADCK}	0.4	—	8.0	MHz	—
	D		Low Power (ADLPC = 1)		0.4	—	4.0		—

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 DC potential difference.

Table 13. 5 V 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
6	P	ADC Asynchronous Clock Source	High Speed (ADLPC = 0)	f_{ADACK}	2	3.3	5	MHz	t_{ADACK} = $1/f_{ADACK}$
			Low Power (ADLPC = 1)		1.25	2	3.3		
7	P	Conversion Time (Including sample time)	Short Sample (ADLSMP = 0)	t_{ADC}	—	20	—	ADCK cycles	See Table 10 for conversion time variances
			Long Sample (ADLSMP = 1)		—	40	—		
8	T	Sample Time	Short Sample (ADLSMP = 0)	t_{ADS}	—	3.5	—	ADCK cycles	
			Long Sample (ADLSMP = 1)		—	23.5	—		
9	T	Total Unadjusted Error	12 bit mode	E_{TUE}	—	±3.0	—	LSB[2]	Includes quantization
	P		10 bit mode		—	±1	±2.5		
	T		8 bit mode		—	±0.5	±1.0		
10	T	Differential Non-Linearity	12 bit mode	DNL	—	±1.75	—	LSB[2]	—
	P		10 bit mode[3]		—	±0.5	±1.0		
	T		8 bit mode[5]		—	±0.3	±0.5		
11	T	Integral Non-Linearity	12 bit mode	INL	—	±1.5	—	LSB[2]	—
	P		10 bit mode		—	±0.5	±1.0		
	T		8 bit mode		—	±0.3	±0.5		
12	T	Zero-Scale Error	12 bit mode	E_{ZS}	—	±1.5	—	LSB[2]	V_{ADIN} = V_{SSAD}
	P		10 bit mode		—	±0.5	±1.5		
	T		8 bit mode		—	±0.5	±0.5		
13	T	Full-Scale Error	12 bit mode	E_{FS}	—	±1	—	LSB[2]	V_{ADIN} = V_{DDAD}
	P		10 bit mode		—	±0.5	±1		
	T		8 bit mode		—	±0.5	±0.5		
14	D	Quantization Error	12 bit mode	E_Q	—	–1 to 0	—	LSB[2]	—
			10 bit mode		—	—	±0.5		
			8 bit mode		—	—	±0.5		
15	D	Input Leakage Error	12 bit mode	E_{IL}	—	±1	—	LSB[2]	Pad leakage[4] * R_{AS}
			10 bit mode		—	±0.2	±2.5		
			8 bit mode		—	±0.1	±1		

Table 13. 5 V 12-bit ADC Characteristics (V_{REFH} = V_{DDA}, V_{REFL} = V_{SSA}) (continued)

Num	C	Characteristic	Conditions	Symb	Min	Typical[1]	Max	Unit	Comment
16	D	Temp Sensor Voltage	25 °C	V_{TEMP25}	—	1.396	—	mV	—
17	D	Temp Sensor Slope	–40 °C — 25 °C	m	—	3.266	—	mV/°C	—
			25 °C — 85 °C		—	3.638	—		

1 Typical values assume V_{DDA} = 5.0 V, Temp = 25 °C, f_{ADCK} = 1.0 MHz unless otherwise stated. Typical values are for reference only and are not tested in production.

2 1 LSB = $(V_{REFH} - V_{REFL})/2^N$

3 Monotonicity and No-Missing-Codes guaranteed in 10 bit and 8 bit modes

4 Based on input pad leakage current. Refer to pad electricals.

2.10 External Oscillator (XOSC) Characteristics

Table 14. Oscillator Electrical Specifications (Temperature Range = –40 to 105 °C Ambient)

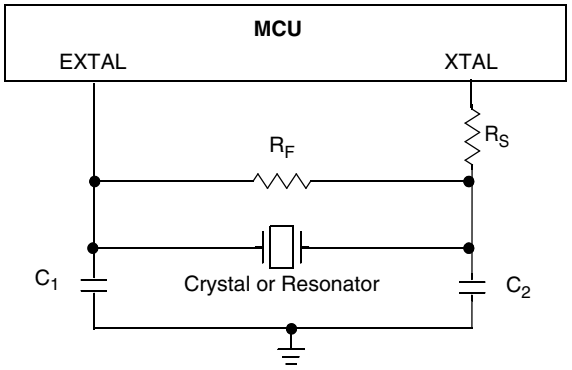
Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
1	C	Oscillator crystal or resonator (EREFS = 1, ERCLKEN = 1) Low range (RANGE = 0) High range (RANGE = 1) FEE or FBE mode [2] High range (RANGE = 1, HGO = 1) FBELP mode High range (RANGE = 1, HGO = 0) FBELP mode	 f_{lo} f_{hi} f_{hi-hgo} f_{hi-lp}	 32 1 1 1	 — — — —	 38.4 16 16 8	 kHz MHz MHz MHz
2	—	Load capacitors	C_1 C_2	See crystal or resonator manufacturer's recommendation.			
3	—	Feedback resistor Low range (32 kHz to 100 kHz) High range (1 MHz to 16 MHz)	R_F		10 1	—	MΩ
4	—	Series resistor Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0) High range, high gain (RANGE = 1, HGO = 1) ≥ 8 MHz 4 MHz 1 MHz	R_S	 — — — — — —	 0 100 0 0 0 0	 — — — 0 10 20	kΩ
5	T	Crystal start-up time [3] Low range, low gain (RANGE = 0, HGO = 0) Low range, high gain (RANGE = 0, HGO = 1) High range, low gain (RANGE = 1, HGO = 0)[4] High range, high gain (RANGE = 1, HGO = 1)[3]	 $t_{CSTL-LP}$ $t_{CSTL-HGO}$ $t_{CSTH-LP}$ $t_{CSTH-HGO}$	 — — — —	 1500 2000 3 7	 — — — —	ms
6	T	Square wave input clock frequency (EREFS = 0, ERCLKEN = 1) FEE mode [2] FBE mode[2] FBELP mode	f_{extal}	 0.03125 0 0	 — — —	 50.33 50.33 50.33	MHz

1 Data in Typical column was characterized at 5.0 V, 25 °C or is typical recommended value.

2 When MCG is configured for FEE or FBE mode, input clock source must be divisible using RDIV to within the range of 31.25 kHz to 39.0625 kHz.

3 This parameter is characterized and not tested on each device. Proper PC board layout procedures must be followed to achieve specifications.

4 4 MHz crystal



2.11 ICS Specifications

Table 15. ICS Frequency Specifications (Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating		Symbol	Min	Typical[1]	Max	Unit
1	C	Internal reference frequency - factory trimmed at V_{DD} = 5 V and temperature = 25 °C		f_{int_ft}	—	32.768	—	kHz
2	C	Average internal reference frequency – untrimmed		f_{int_ut}	31.25	—	39.06	kHz
3	T	Internal reference startup time		t_{irefst}	—	60	100	µs
4	C	DCO output frequency range - untrimmed [2]	Low range (DRS = 00)	f_{dco_ut}	16	—	20	MHz
	C		Mid range (DRS = 01)		32	—	40	
	C		High range (DRS = 10)		48	—	60	
5	P	DCO output frequency[2] Reference =32768Hz and DMX32 = 1	Low range (DRS = 00)	f_{dco_DMX32}	—	16.82	—	MHz
	P		Mid range (DRS = 01)		—	33.69	—	
	P		High range (DRS = 10)		—	50.48	—	
6	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.1	±0.2	$\%f_{dco}$
7	D	Resolution of trimmed DCO output frequency at fixed voltage and temperature (not using FTRIM)		$\Delta f_{dco\_res\_t}$	—	±0.2	±0.4	$\%f_{dco}$
8	D	Total deviation of trimmed DCO output frequency over full voltage and temperature range		Δf_{dco_t}	—	0.5 –1.0	±2	$\%f_{dco}$
9	D	Total deviation of trimmed DCO output frequency over fixed voltage and temperature range of 0 –70 °C		Δf_{dco_t}	—	±0.5	±1	$\%f_{dco}$

Table 15. ICS Frequency Specifications (continued)(Temperature Range = –40 to 105 °C Ambient)

Num	C	Rating	Symbol	Min	Typical[1]	Max	Unit
10	D	FLL acquisition time [3]	$t_{fll\_acquire}$	—	—	1	ms
11	D	Long term Jitter of DCO output clock (averaged over 2ms interval) [4]	C_{Jitter}	—	0.02	0.2	$\%f_{dco}$
12	D	Loss of external clock minimum freq. (RANGE = 0) • ext. clock freq: above $(3/5)f_{int}$, never reset • ext. clock freq: between $(2/5)f_{int}$ and $(3/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(2/5)f_{int}$, always reset	f_{loc_low}	$(3/5) \times f_{int}$	—	—	kHz
13	D	Loss of external clock minimum freq. (RANGE = 1) • ext. clock freq: above $(16/5)f_{int}$, never reset • ext. clock freq: between $(15/5)f_{int}$ and $(16/5)f_{int}$, maybe reset (phase dependency) • ext. clock freq: below $(15/5)f_{int}$, always reset	f_{loc_high}	$(16/5) \times f_{int}$	—	—	kHz

1 Data in Typical column was characterized at 3.0 V, 25 °C or is typical recommended value

2 The resulting bus clock frequency should not exceed the maximum specified bus clock frequency of the device.

3 This specification applies to any time the FLL reference source or reference divider is changed, trim value changed or changing from FLL disabled (BLPE, BLPI) to FLL enabled (FEI, FEE, FBE, FBI). If a crystal/resonator is being used as the reference, this specification assumes it is already running.

4 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum f_{BUS}. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the FLL circuitry by V_{DD} and V_{SS} and variation in crystal oscillator frequency increase the C_{Jitter} percentage for a given interval.

2.12 AC Characteristics

This section describes ac timing characteristics for each peripheral system.

2.12.1 Control Timing

Table 16. Control Timing

Num	C	Parameter	Symbol	Min	Typ[1]	Max	Unit
1	D	Bus frequency (t_{cyc} = 1/f_{Bus})	f_{Bus}	dc	—	24	MHz
2	D	Internal low-power oscillator period	t_{LPO}	800	—	1500	μs
3	D	External reset pulse width[2] (t_{cyc} = 1/f_{Self_reset})	t_{extrst}	100	—	—	ns
4	D	Reset low drive	t_{rstdrv}	66 x t_{cyc}	—	—	ns
5	D	Active background debug mode latch setup time	t_{MSSU}	500	—	—	ns
6	D	Active background debug mode latch hold time	t_{MSH}	100	—	—	ns
7	D	IRQ pulse width Asynchronous path[2] Synchronous path[3]	t_{ILIH}, t_{IHIL}	 100 1.5 x t_{cyc}	—	—	ns
8		Port rise and fall time (load = 30 pF for SPI, rest 50 pF)[4] Slew rate control disabled (PTxSE = 0) High drive Slew rate control enabled (PTxSE = 1) High drive Slew rate control disabled (PTxSE = 0) Low drive Slew rate control enabled (PTxSE = 1) Low drive	t_{Rise}, t_{Fall}	 — —	 11 35 40 75		ns

1 Typical values are based on characterization data at V_{DD} = 5.0 V, 25 °C unless otherwise stated.

2 This is the shortest pulse that is guaranteed to be recognized as a $\overline{\text{RESET}}$ pin request. Shorter pulses are not guaranteed to override reset requests from internal sources.

3 This is the minimum pulse width that is guaranteed to pass through the pin synchronization circuitry. Shorter pulses may or may not be recognized. In stop mode, the synchronizer is bypassed so shorter pulses can be recognized in that case.

4 Timing is shown with respect to 20% V_{DD} and 80% V_{DD} levels. Temperature range –40°C to 105°C.

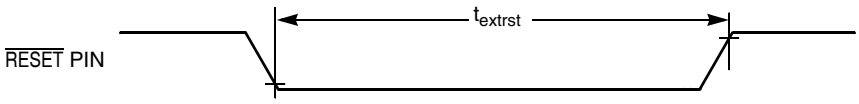


Figure 11. Reset Timing

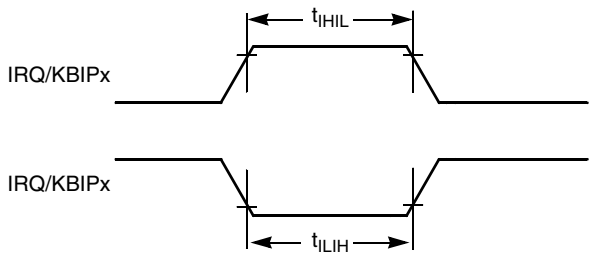


Figure 12. IRQ/KBIPx Timing

2.12.2 Timer (TPM/FTM) Module Timing

Synchronizer circuits determine the shortest input pulses that can be recognized or the fastest clock that can be used as the optional external source to the timer counter. These synchronizers operate from the current bus rate clock.

Table 17. TPM/FTM Input Timing

NUM	C	Function	Symbol	Min	Max	Unit
1	—	External clock frequency	f_{TPMext}	DC	$f_{Bus}/4$	MHz
2	—	External clock period	t_{TPMext}	4	—	t_{cyc}
3	D	External clock high time	t_{clkh}	1.5	—	t_{cyc}
4	D	External clock low time	t_{clkl}	1.5	—	t_{cyc}
5	D	Input capture pulse width	t_{ICPW}	1.5	—	t_{cyc}

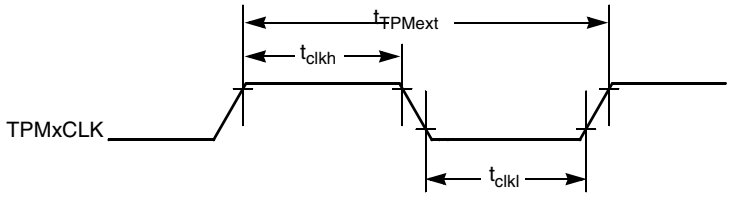


Figure 13. Timer External Clock

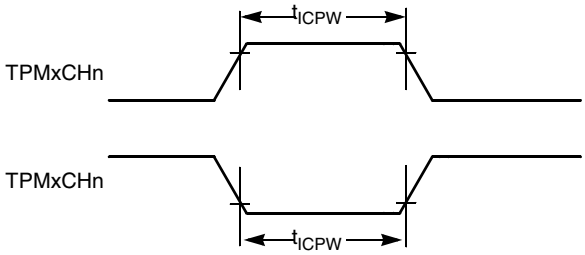
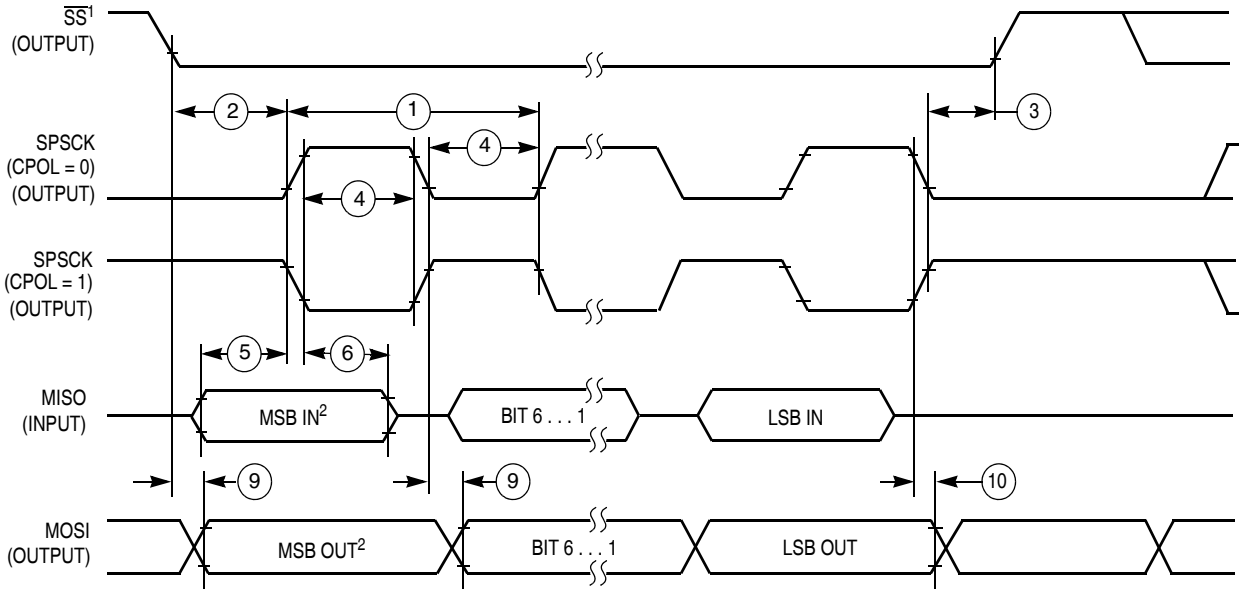


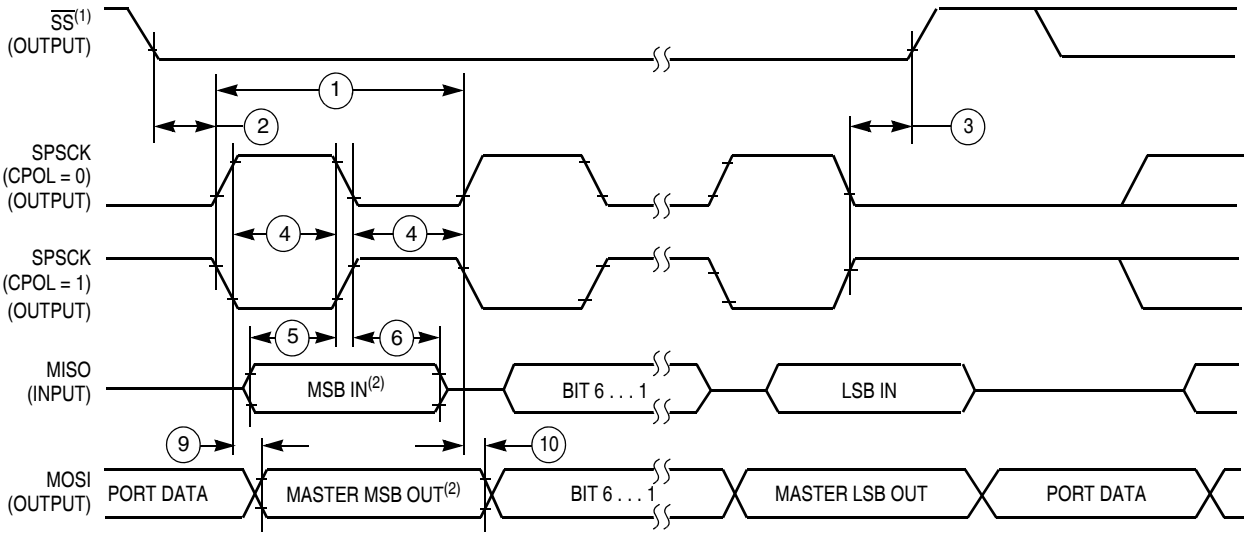
Figure 14. Timer Input Capture Pulse



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 15. SPI Master Timing (CPHA = 0)



NOTES:

1. $\overline{SS}$ output mode (DDS7 = 1, SSOE = 1).
2. LSBF = 0. For LSBF = 1, bit order is LSB, bit 1, ..., bit 6, MSB.

Figure 16. SPI Master Timing (CPHA = 1)

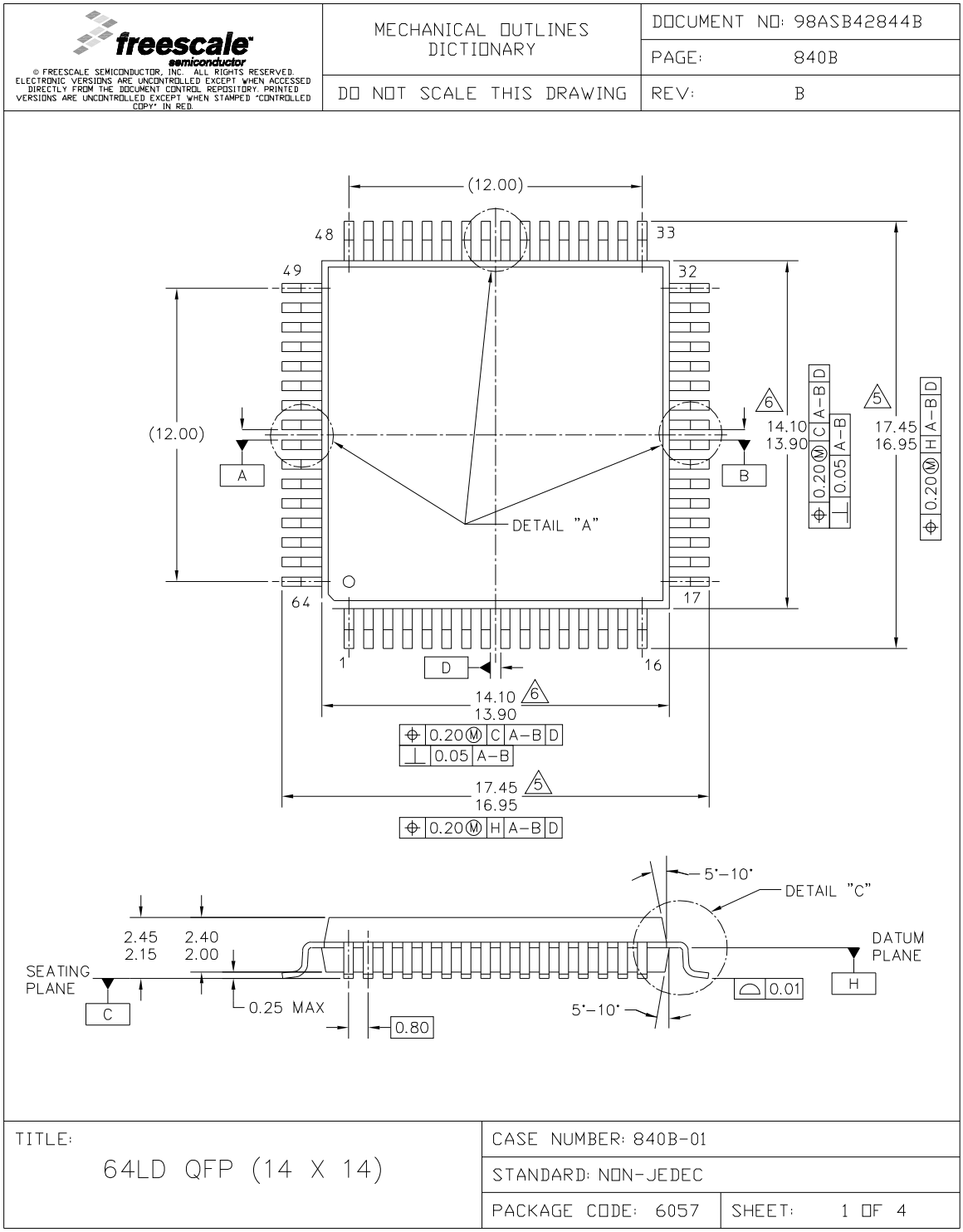
freescale semiconductor	MECHANICAL OUTLINES DICTIONARY	DOCUMENT NO: 98ASS23234W
		PAGE: 840F
	DO NOT SCALE THIS DRAWING	REV: E

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.
5. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE UPPER LIMIT BY MORE THAN 0.08 mm AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
6. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 mm PER SIDE. THIS DIMENSION IS MAXIMUM PLASTIC BODY SIZE DIMENSION INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.25 mm FROM THE LEAD TIP.

TITLE: 64LD LQFP, 10 X 10 X 1.4 PKG, 0.5 PITCH, CASE OUTLINE	CASE NUMBER: 840F–02	
	STANDARD: JEDEC MS–026 BCD	
	PACKAGE CODE: 8426	SHEET: 3

5.3 64-pin QFP Package



6 Revision History

Table 22. Revision History

Rev. No.	Date	Description
1	11/2008	Initial Draft Release.
2	4/2009	Internal Release.
3	5/2009	Alpha Customer Release.
4	12/2009	• Added 48-pin LQFP information; • Updated Section 2.5/17 and 2.6/21. • Provided the supply current in Section 2.7/23, and setup delay in Section 2.8/23.
5	6/2010	• Updated Table 10. • Added Figure 9. • Corrected pin names of PTG6 and PTG5 in 48-pin LQFP. • Standardized Generation 2008 Watchdog to Watchdog. • In Table 9, updated Output high/low voltage — Low Drive (PTxDSn = 0) 3 V, I_{Load} value.