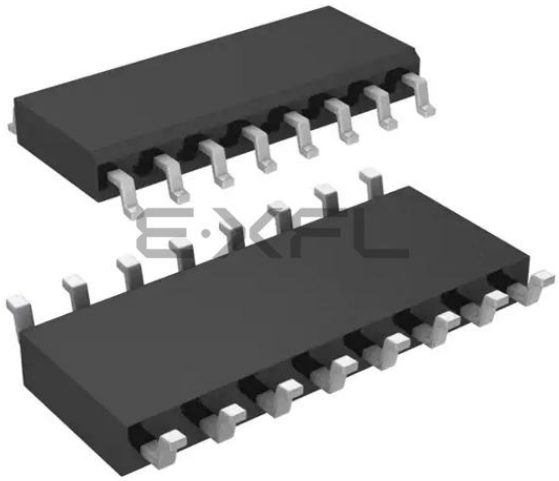

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What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	HB LED Controller
Core Processor	M8C
Program Memory Type	FLASH (4KB)
Controller Series	CY8CLED
RAM Size	256 x 8
Interface	I²C, IrDA, SPI, UART/USART
Number of I/O	12
Voltage - Supply	2.4V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	16-SOIC (0.154", 3.90mm Width)
Supplier Device Package	16-SOIC
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled02-16sxit

Contents

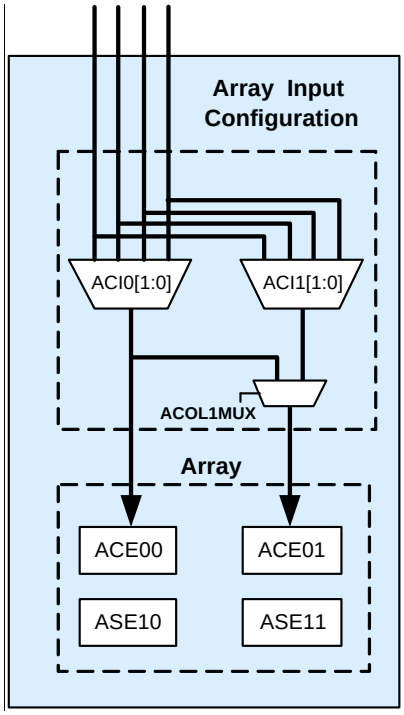
The Analog System

The analog system is composed of four configurable blocks that enable creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- ADCs (single or dual, with 10-bit resolution)
- Pin-to-pin comparators (1)
- Single-ended comparators (up to two) with absolute (1.3-V) reference or 8-bit DAC reference
- 1.3-V reference (as a system resource)

In most PSoC based devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. This particular EZ-Color device provides limited functionality Type E analog blocks. Each column contains one CT block and one SC block.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital blocks as clock dividers.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-voltage detect (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital, and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1. EZ-Color Device Characteristics

Part Number	LED Channels	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense®
CY8CLED02	2	16	1	4	8	0	2	4	256 Bytes	4K	No
CY8CLED04	4	56	1	4	48	2	2	6	1K	16K	Yes
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	44	4	16	12	4	4	12	2K	32K	No

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this datasheet and using the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date ordering, packaging, and electrical specification information, reference the latest device datasheets on the cypress website at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

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Technical Support

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Pin Information

Pinouts

This section describes, lists, and illustrates the CY8CLED02 EZ-Color device pins and pinout configurations. The CY8CLED02 device is available in a variety of packages which are listed and illustrated in the following tables. Every port pin (labeled with a “P”) is capable of Digital I/O. However, V_{SS}, V_{DD}, SMP, and XRES are not capable of Digital I/O.

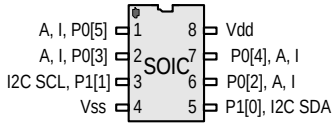
8-Pin Part Pinout

Table 2. 8-Pin Part Pinout (SOIC)

Pin No.	Type		Pin Name	Description
	Digital	Analog		
1	I/O	I	P0[5]	Analog column mux input.
2	I/O	I	P0[3]	Analog column mux input.
3	I/O	–	P1[1]	I^2C serial clock (SCL), ISSP-SCLK.
4	Power		V_{SS}	Ground connection.
5	I/O	–	P1[0]	I^2C serial data (SDA), ISSP-SDATA.
6	I/O	I	P0[2]	Analog column mux input.
7	I/O	I	P0[4]	Analog column mux input.
8	Power		V_{DD}	Supply voltage.

LEGEND: A = Analog, I = Input, and O = Output.

Figure 3. 8-Pin EZ-Color Device



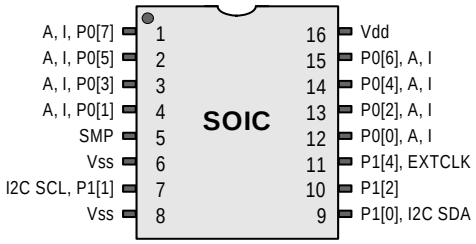
16-Pin Part Pinout

Table 3. 16-Pin Part Pinout (SOIC)

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[7]	Analog column mux input.
2	I/O	I	P0[5]	Analog column mux input.
3	I/O	I	P0[3]	Analog column mux input.
4	I/O	I	P0[1]	Analog column mux input.
5	Power		SMP	Switch mode pump (SMP) connection to required external components.
6	Power		V_{SS}	Ground connection.
7	I/O	–	P1[1]	I^2C SCL, ISSP-SCLK.
8	Power		V_{SS}	Ground connection.
9	I/O	–	P1[0]	I^2C SDA, ISSP-SDATA.
10	I/O	–	P1[2]	
11	I/O	–	P1[4]	Optional external clock input (EXTCLK).
12	I/O	I	P0[0]	Analog column mux input.
13	I/O	I	P0[2]	Analog column mux input.
14	I/O	I	P0[4]	Analog column mux input.
15	I/O	I	P0[6]	Analog column mux input.
16	Power		V_{DD}	Supply voltage.

LEGEND A = Analog, I = Input, and O = Output.

Figure 4. 16-Pin EZ-Color Device



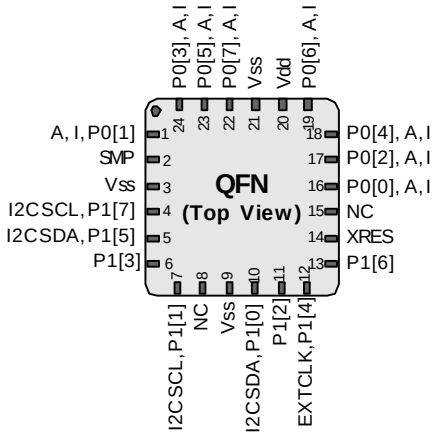
24-Pin Part Pinout

Table 4. 24-Pin Part Pinout (QFN)[2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	Analog column mux input.
2	Power		SMP	SMP connection to required external components.
3	Power		V_{SS}	Ground connection.
4	I/O	–	P1[7]	I^2C SCL.
5	I/O	–	P1[5]	I^2C SDA.
6	I/O	–	P1[3]	–
7	I/O	–	P1[1]	I^2C SCL, ISSP-SCLK[1].
8			NC	No connection.
9	Power		V_{SS}	Ground connection.
10	I/O	–	P1[0]	I^2C SDA, ISSP-SDATA[1].
11	I/O	–	P1[2]	–
12	I/O	–	P1[4]	Optional external clock input (EXTCLK).
13	I/O	–	P1[6]	
14	Input		XRES	Active high external reset with internal pull down.
15			NC	No connection.
16	I/O	I	P0[0]	Analog column mux input.
17	I/O	I	P0[2]	Analog column mux input.
18	I/O	I	P0[4]	Analog column mux input.
19	I/O	I	P0[6]	Analog column mux input.
20	Power		V_{DD}	Supply voltage.
21	Power		V_{SS}	Ground connection.
22	I/O	I	P0[7]	Analog column mux input.
23	I/O	I	P0[5]	Analog column mux input.
24	I/O	I	P0[3]	Analog column mux input.

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. 24-Pin EZ-Color Device



Notes
1. These are the ISSP pins, which are not High Z at power-on reset (POR).
2. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Register Reference

Register Conventions

This section lists the registers of the CY8CLED02 EZ-Color device.

The register conventions specific to this section are listed in the following table.

Table 5. Register Conventions

Convention	Description
R	Read register or bit(s)
W	Write register or bit(s)
L	Logical register or bit(s)
C	Clearable register or bit(s)
#	Access is bit specific

Register Mapping Tables

The device has a total register address space of 512 bytes. The register space is referred to as I/O space and is divided into two banks, Bank 0 and Bank 1. The XOI bit in the Flag register (CPU_F) determines which bank the user is currently in. When the XOI bit is set to 1, the user is in Bank 1.

Note In the following register mapping tables, blank fields are Reserved and should not be accessed.

Table 7. Register Map Bank 1: Configuration Space

Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access	Name	Addr (1,Hex)	Access
PRT0DM0	00	RW		40		ASE10CR0	80	RW		C0	
PRT0DM1	01	RW		41			81			C1	
PRT0IC0	02	RW		42			82			C2	
PRT0IC1	03	RW		43			83			C3	
PRT1DM0	04	RW		44		ASE11CR0	84	RW		C4	
PRT1DM1	05	RW		45			85			C5	
PRT1IC0	06	RW		46			86			C6	
PRT1IC1	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90		GDI_O_IN	D0	RW
	11			51			91		GDI_E_IN	D1	RW
	12			52			92		GDI_O_OU	D2	RW
	13			53			93		GDI_E_OU	D3	RW
	14			54			94			D4	
	15			55			95			D5	
	16			56			96			D6	
	17			57			97			D7	
	18			58			98			D8	
	19			59			99			D9	
	1A			5A			9A			DA	
	1B			5B			9B			DB	
	1C			5C			9C			DC	
	1D			5D			9D		OSC_GO_EN	DD	RW
	1E			5E			9E		OSC_CR4	DE	RW
	1F			5F			9F		OSC_CR3	DF	RW
DBB00FN	20	RW	CLK_CR0	60	RW		A0		OSC_CR0	E0	RW
DBB00IN	21	RW	CLK_CR1	61	RW		A1		OSC_CR1	E1	RW
DBB00OU	22	RW	ABF_CR0	62	RW		A2		OSC_CR2	E2	RW
	23		AMD_CR0	63	RW		A3		VLT_CR	E3	RW
DBB01FN	24	RW	CMP_GO_EN	64	RW		A4		VLT_CMP	E4	R
DBB01IN	25	RW		65			A5		ADC0_TR	E5	RW
DBB01OU	26	RW	AMD_CR1	66	RW		A6		ADC1_TR	E6	RW
	27		ALT_CR0	67	RW		A7			E7	
DCB02FN	28	RW		68			A8		IMO_TR	E8	W
DCB02IN	29	RW		69			A9		ILO_TR	E9	W
DCB02OU	2A	RW		6A			AA		BDG_TR	EA	RW
	2B		CLK_CR3	6B	RW		AB		ECO_TR	EB	W
DCB03FN	2C	RW	TMP_DR0	6C	RW		AC			EC	
DCB03IN	2D	RW	TMP_DR1	6D	RW		AD			ED	
DCB03OU	2E	RW	TMP_DR2	6E	RW		AE			EE	
	2F		TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA		FLS_PR1	FA	RW
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

DC Electrical Characteristics

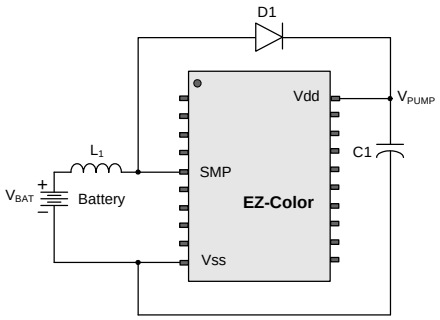
DC Chip-Level Specifications

Table 10 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 10. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See DC POR and LVD specifications, Table 18 on page 20.
I_{DD}	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are V_{DD} = 5.0 V, 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply current, IMO = 6 MHz	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply current, IMO = 6 MHz	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C to 40 °C.
I_{SB}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, -40 °C ≤ T_A ≤ 85 °C.
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 3.0 V to 5.25 V.
V_{REF27}	Reference voltage (Bandgap)	1.16	1.30	1.330	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V.
AGND	Analog ground	V_{REF} - 0.003	V_{REF}	V_{REF} + 0.003	V	

Figure 7. Basic Switch Mode Pump Circuit



DC POR and LVD Specifications

Table 18 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 18. DC POR and LVD Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
	V_{DD} value for PPOR trip					V_{DD} must be greater than or equal to 2.5 V during startup, reset from the XRES pin, or reset from Watchdog.
V_{PPOR0}	PORLEV[1:0] = 00b	–	2.36	2.40	V	
V_{PPOR1}	PORLEV[1:0] = 01b		2.82	2.95	V	
V_{PPOR2}	PORLEV[1:0] = 10b		4.55	4.70	V	
	V_{DD} value for LVD trip					
V_{LVD0}	VM[2:0] = 000b	2.40	2.45	2.51[4]	V	
V_{LVD1}	VM[2:0] = 001b	2.85	2.92	2.99[5]	V	
V_{LVD2}	VM[2:0] = 010b	2.95	3.02	3.09	V	
V_{LVD3}	VM[2:0] = 011b	3.06	3.13	3.20	V	
V_{LVD4}	VM[2:0] = 100b	4.37	4.48	4.55	V	
V_{LVD5}	VM[2:0] = 101b	4.50	4.64	4.75	V	
V_{LVD6}	VM[2:0] = 110b	4.62	4.73	4.83	V	
V_{LVD7}	VM[2:0] = 111b	4.71	4.81	4.95	V	
	V_{DD} value for PUMP trip					
V_{PUMP0}	VM[2:0] = 000b	2.45	2.55	2.62[6]	V	
V_{PUMP1}	VM[2:0] = 001b	2.96	3.02	3.09	V	
V_{PUMP2}	VM[2:0] = 010b	3.03	3.10	3.16	V	
V_{PUMP3}	VM[2:0] = 011b	3.18	3.25	3.32[7]	V	
V_{PUMP4}	VM[2:0] = 100b	4.54	4.64	4.74	V	
V_{PUMP5}	VM[2:0] = 101b	4.62	4.73	4.83	V	
V_{PUMP6}	VM[2:0] = 110b	4.71	4.82	4.92	V	
V_{PUMP7}	VM[2:0] = 111b	4.89	5.00	5.12	V	

Notes
4. Always greater than 50 mV above PPOR (PORLEV = 00) for falling supply.
5. Always greater than 50 mV above PPOR (PORLEV = 10) for falling supply.
6. Always greater than 50 mV above V_{LVD0}.
7. Always greater than 50 mV above V_{LVD3}.

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operations	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} - 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC I^2C Specifications[10]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Notes

8. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
   For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
10. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications mentioned in section DC General Purpose I/O Specifications on page 16. The I^2C GPIO pins also meet the mentioned specs.

AC GPIO Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

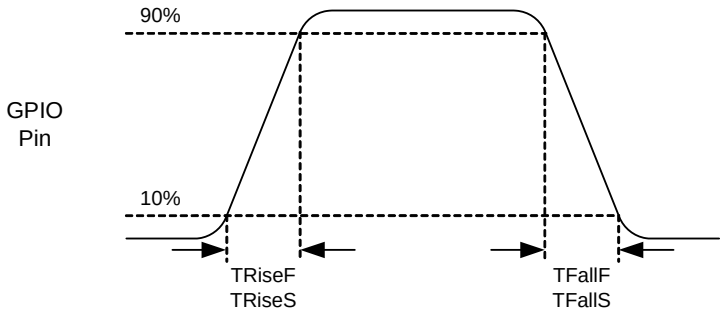
Table 23. 5-V and 3.3-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	12	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	3	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	2	–	18	ns	V_{DD} = 4.5 to 5.25 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	10	27	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	10	22	–	ns	V_{DD} = 3 to 5.25 V, 10% - 90%

Table 24. 2.7-V AC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{GPIO}	GPIO operating frequency	0	–	3	MHz	Normal strong mode
TRiseF	Rise time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%
TFallF	Fall time, normal strong mode, Cload = 50 pF	6	–	50	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%
TRiseS	Rise time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%
TFallS	Fall time, slow strong mode, Cload = 50 pF	18	40	120	ns	V_{DD} = 2.4 to 3.0 V, 10% - 90%

Figure 8. GPIO Timing Diagram



AC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.Settling times, slew rates, and gain bandwidth are based on the Analog Continuous Time PSoC block.

Table 25. 5-V and 3.3-V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP1}	Comparator mode response time, 50 mVpp signal centered on reference	–	–	100	ns	
T_{COMP2}	Comparator mode response time, 2.5 V input, 0.5 V overdrive	–	–	300	ns	

Table 26. 2.7V AC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{COMP1}	Comparator mode response Time, 50 mVpp signal centered on Ref	–	–	600	ns	
T_{COMP2}	Comparator mode response time, 1.5 V input, 0.5 V overdrive	–	–	300	ns	

AC Low Power Comparator Specifications

Table 27 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V at 25 °C and are for design guidance only.

Table 27. AC Low Power Comparator Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RLPC}	LPC response time	–	–	50	µs	≥ 50 mV overdrive comparator reference set within V_{REFLPC}.

Table 29. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Block input clock frequency			12.7	MHz	2.4 V < V_{DD} < 3.0 V.
Timer	Capture pulse width	100[18]	–	–	ns	
	Input clock frequency, with or without Capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power up IMO to switch	150	–	–	µs	

Note
18. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Table 31. 3.3-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	12.3	MHz	Maximum CPU frequency is 12 MHz at 3.3 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	24.6	MHz	If the frequency of the external clock is greater than 12 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	41.7	–	5300	ns	
–	Low period with CPU clock divide by 1	41.7	–	–	ns	
–	Power up IMO to switch	150	–	–	µs	

Table 32. 2.7-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency with CPU clock divide by 1	0.093	–	6.06	MHz	Maximum CPU frequency is 3 MHz at 2.7 V. With the CPU clock divider set to 1, the external clock must adhere to the maximum frequency and duty cycle requirements.
F_{OSCEXT}	Frequency with CPU clock divide by 2 or greater	0.186	–	12.12	MHz	If the frequency of the external clock is greater than 3 MHz, the CPU clock divider must be set to 2 or greater. In this case, the CPU clock divider will ensure that the fifty percent duty cycle requirement is met.
–	High period with CPU clock divide by 1	83.4	–	5300	ns	
–	Low period with CPU clock divide by 1	83.4	–	–	ns	
–	Power up IMO to switch	150	–	–	µs	

AC Programming Specifications

Table 33 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 33. AC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
T_{RSCLK}	Rise time of SCLK	1	–	20	ns	
T_{FSCLK}	Fall time of SCLK	1	–	20	ns	
T_{SSCLK}	Data setup time to falling edge of SCLK	40	–	–	ns	
T_{HSCLK}	Data hold time from falling edge of SCLK	40	–	–	ns	
F_{SCLK}	Frequency of SCLK	0	–	8	MHz	
T_{ERASEB}	Flash erase time (block)	–	10	–	ms	
T_{WRITE}	Flash block write time	–	80	–	ms	
T_{DSCLK3}	Data out delay from falling edge of SCLK	–	–	50	ns	3.0 ≤ V_{DD} ≤ 3.6
T_{DSCLK2}	Data out delay from falling edge of SCLK	–	–	70	ns	2.4 ≤ V_{DD} ≤ 3.0
$T_{ERASEALL}$	Flash erase time (Bulk)	–	20	–	ms	Erase all blocks and protection fields at once.
$T_{PROGRAM\_HOT}$	Flash block erase + flash block write time	–	–	180[19]	ms	0 °C ≤ T_J ≤ 100 °C
$T_{PROGRAM\_COLD}$	Flash block erase + flash block write time	–	–	360[19]	ms	–40 °C ≤ T_J ≤ 0 °C

AC I^2C Specifications

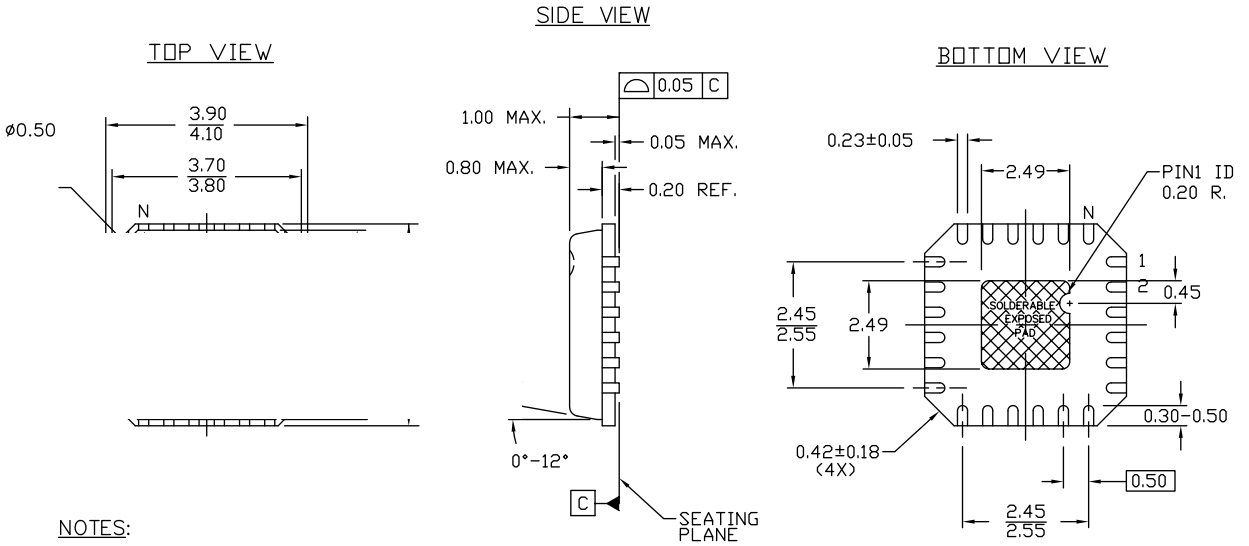
The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and -40°C ≤ T_A ≤ 85°C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 34. AC Characteristics of the I^2C SDA and SCL Pins for Vcc ≥ 3.0 V

Symbol	Description	Standard-Mode		Fast-Mode		Units	Notes
		Min	Max	Min	Max		
F_{SCLI2C}	SCL clock frequency	0	100	0	400	kHz	
$T_{HDSTAI2C}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4.0	–	0.6	–	µs	
T_{LOWI2C}	LOW period of the SCL Clock	4.7	–	1.3	–	µs	
$T_{HIGHI2C}$	HIGH period of the SCL Clock	4.0	–	0.6	–	µs	
$T_{SUSTAI2C}$	Setup time for a repeated START condition	4.7	–	0.6	–	µs	
$T_{HDDATI2C}$	Data hold time	0	–	0	–	µs	
$T_{SUDATI2C}$	Data setup time	250	–	100[20]	–	ns	
$T_{SUSTOI2C}$	Setup time for STOP condition	4.0	–	0.6	–	µs	
T_{BUFI2C}	Bus free time between a STOP and START condition	4.7	–	1.3	–	µs	
T_{SPI2C}	Pulse width of spikes are suppressed by the input filter.	–	–	0	50	ns	

Note
19. For the full industrial range, you must employ a Temperature Sensor User Module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 - PSoC® 1 - Reading and Writing PSoC Flash.

Figure 12. 24-Pin (4x4) QFN



NOTES:

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.042g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF24A	STANDARD
LY24A	LEAD FREE

51-85203 *C

Accessories (Emulation and Programming)

Table 38. Emulation and Programming Accessories

Part #	Pin Package	Flex-Pod Kit[23]	Foot Kit[24]	Adapter[25]
CY8CLED02-16SXI	16-pin SOIC	CY3250-LED02	CY3250-16SOIC-FK	Adapters can be found at http://www.emulation.com.
CY8CLED02-24LFXI	24-pin QFN	CY3250-LED02QFN	CY3250-24QFN-FK	

Ordering Information

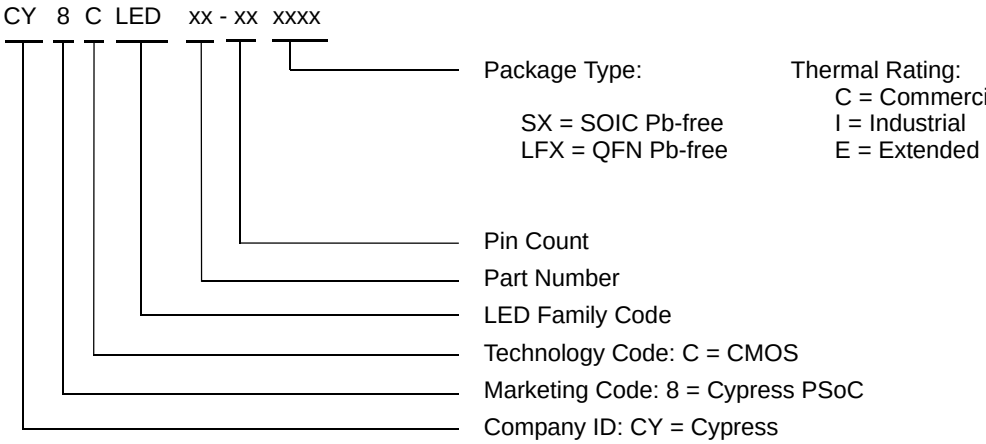
Key Device Features

The following table lists the CY8CLED02 EZ-Color devices' key package features and ordering codes.

Table 39. Device Key Features and Ordering Information

Package	Ordering Code	Flash (Bytes)	RAM (Bytes)	Switch Mode Pump	Temperature Range	Digital Blocks	Analog Blocks	Digital I/O Pins	Analog Inputs	Analog Outputs	XRES Pin
16-Pin (150-Mil) SOIC	CY8CLED02-16SXI	4 K	256	Yes	–40 °C to +85 °C	4	4	12	8	0	No
16-Pin (150-Mil) SOIC (Tape and Reel)	CY8CLED02-16SXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	12	8	0	No
24-Pin (4x4) QFN	CY8CLED02-24LFXI	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes
24-Pin (4x4) QFN (Tape and Reel)	CY8CLED02-24LFXIT	4 K	256	Yes	–40 °C to +85 °C	4	4	16	8	0	Yes

Ordering Code Definitions



Notes
23. Flex-Pod kit includes a practice flex-pod and a practice PCB, in addition to two flex-pods.
24. Foot kit includes surface mount feet that can be soldered to the target PCB.
25. Programming adapter converts non-DIP package to DIP footprint. Specific details and ordering information for each of the adapters can be found at http://www.emulation.com.

Glossary (continued)

digital-to-analog (DAC)	A device that changes a digital signal to an analog signal of corresponding magnitude. The analog-to-digital (ADC) converter performs the reverse operation.
duty cycle	The relationship of a clock period high time to its low time, expressed as a percent.
emulator	Duplicates (provides an emulation of) the functions of one system with a different system, so that the second system appears to behave like the first system.
External Reset (XRES)	An active high signal that is driven into the PSoC device. It causes all operation of the CPU and blocks to stop and return to a pre-defined state.
Flash	An electrically programmable and erasable, non-volatile technology that provides you the programmability and data storage of EPROMs, plus in-system erasability. Non-volatile means that the data is retained when power is OFF.
Flash block	The smallest amount of flash ROM space that may be programmed at one time and the smallest amount of flash space that may be protected. A flash block holds 64 bytes.
frequency	The number of cycles or events per unit of time, for a periodic function.
gain	The ratio of output current, voltage, or power to input current, voltage, or power, respectively. Gain is usually expressed in dB.
I^2C	A two-wire serial computer bus by Philips Semiconductors (now NXP Semiconductors). I^2C is an Inter-Integrated Circuit. It is used to connect low-speed peripherals in an embedded system. The original system was created in the early 1980s as a battery control interface, but it was later used as a simple internal bus system for building control electronics. I^2C uses only two bi-directional pins, clock and data, both running at +5 V and pulled high with resistors. The bus operates at 100 kbits/second in standard mode and 400 kbits/second in fast mode.
ICE	The in-circuit emulator that allows you to test the project in a hardware environment, while viewing the debugging device activity in a software environment (PSoC Designer).
input/output (I/O)	A device that introduces data into or extracts data from a system.
interrupt	A suspension of a process, such as the execution of a computer program, caused by an event external to that process, and performed in such a way that the process can be resumed.
interrupt service routine (ISR)	A block of code that normal code execution is diverted to when the M8C receives a hardware interrupt. Many interrupt sources may each exist with its own priority and individual ISR code block. Each ISR code block ends with the RETI instruction, returning the device to the point in the program where it left normal program execution.
jitter	1. A misplacement of the timing of a transition from its ideal position. A typical form of corruption that occurs on serial data streams. 2. The abrupt and unwanted variations of one or more signal characteristics, such as the interval between successive pulses, the amplitude of successive cycles, or the frequency or phase of successive cycles.
low-voltage detect (LVD)	A circuit that senses V_{DD} and provides an interrupt to the system when V_{DD} falls lower than a selected threshold.
M8C	An 8-bit Harvard-architecture microprocessor. The microprocessor coordinates all activity inside a PSoC by interfacing to the flash, SRAM, and register space.

Glossary (continued)

serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level *API* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
Watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

Document History Page

Document Title: CY8CLED02 EZ-Color™ HB LED Controller Document Number: 001-13704				
Revision	**ECN #**	**Submission Date**	**Origin of Change**	**Description of Change**
**	1383443	See ECN	SFVTMP3/AESA	New document
*A	2732564	07/09/2009	CGX	Converted from Preliminary to Final
*B	2794355	10/28/2009	XBM	Added "Contents" on page 2 Updated "Development Tools" on page 6. Corrected FCPU1 and FCPU2 parameters in Table 21, "5-V and 3.3-V AC Chip-Level Specifications," on page 22 and Table 22, "2.7-V AC Chip-Level Specifications," on page 23
*C	2850593	01/14/2010	FRE	Updated DC GPIO, AC Chip-Level, and AC Programming Specifications as follows: Modified FIMO6 and TWRITE specifications. Replaced TRAMP (time) specification with SRPOWER_UP (slew rate) specification. Added note to Flash Endurance specification. Added IOH, IOL, DCILO, F32K_U, TPOWERUP, TERASEALL, TPROGRAM_HOT, and TPROGRAM_COLD specifications. Corrected the Pod Kit part numbers. Updated Development Tool Selection. Updated copyright and Sales, Solutions, and Legal Information URLs. Updated 24-Pin QFN package diagram.
*D	2903043	04/01/2010	NJF	Updated Cypress website links Added $T_{BAKETEMP}$ and $T_{BAKETIME}$ parameters Updated package diagrams Removed sections "Third Party Tools" and "Build a PSoC Emulator"
*E	3111554	12/15/10	NJF	Added DC I^2C Specifications table. Added F_{32K_U} max limit. Added Tjit_IMO specification, removed existing jitter specifications. Updated Units of Measure, Acronyms, Glossary, and References sections. Updated solder reflow specifications. No specific changes were made to AC Digital Block Specifications table and I^2C Timing Diagram. They were updated for clearer understanding.
*F	3283843	07/13/11	DIVA	Updated Getting Started, Development Tools, and Designing with PSoC Designer. Removed obsolete kits. Removed reference to obsolete spec AN2012.
*G	3403622	10/12/11	MKKU	Removed the following pruned parts from the Ordering Information and Accessories (Emulation and Programming) sections. CY8CLED02-8SXI CY8CLED02-8SXIT