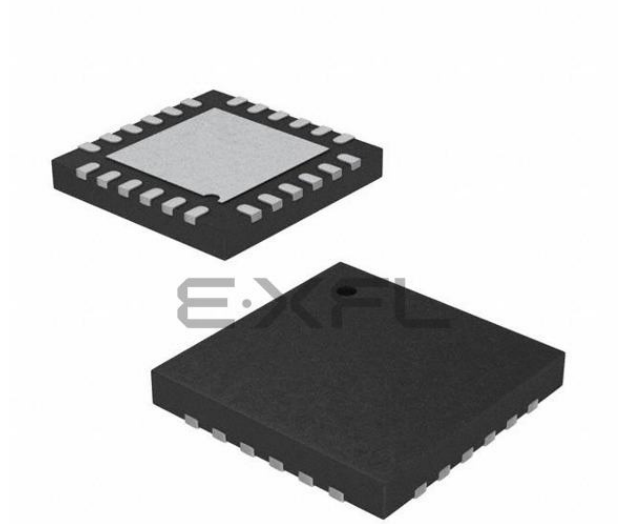

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Embedded - Microcontrollers - Application Specific: Tailored Solutions for Precision and Performance

Embedded - Microcontrollers - Application Specific represents a category of microcontrollers designed with unique features and capabilities tailored to specific application needs. Unlike general-purpose microcontrollers, application-specific microcontrollers are optimized for particular tasks, offering enhanced performance, efficiency, and functionality to meet the demands of specialized applications.

What Are Embedded - Microcontrollers - Application Specific?

Application-specific microcontrollers are engineered to

Details	
Product Status	Obsolete
Applications	HB LED Controller
Core Processor	M8C
Program Memory Type	FLASH (4KB)
Controller Series	CY8CLED
RAM Size	256 x 8
Interface	I²C, IrDA, SPI, UART/USART
Number of I/O	16
Voltage - Supply	2.4V ~ 5.25V
Operating Temperature	-40°C ~ 85°C
Mounting Type	Surface Mount
Package / Case	24-VFQFN Exposed Pad
Supplier Device Package	24-QFN (4x4)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8cled02-24lfxit

EZ-Color™ Functional Overview

Cypress's EZ-Color family of devices offers the ideal control solution for High Brightness LED applications requiring intelligent dimming control. EZ-Color devices combine the power and flexibility of Programmable System-on-Chip (PSoC®); with Cypress' precise illumination signal modulation (PrISM™) drive technology providing lighting designers a fully customizable and integrated lighting solution platform.

The EZ-Color family supports a range of independent LED channels from 4 channels at 32 bits of resolution each, up to 16 channels at 8 bits of resolution each. This enables lighting designers the flexibility to choose the LED array size and color quality. PSoC Designer software, with lighting specific drivers, can significantly cut development time and simplify implementation of fixed color points through temperature, optical, and LED binning compensation. EZ-Color's virtually limitless analog and digital customization enables the simple integration of features in addition to intelligent lighting, such as Battery Charging, Image Stabilization, and Motor Control during the development process. These features, along with Cypress's best-in-class quality and design support, make EZ-Color the ideal choice for intelligent HB LED control applications.

Target Applications

- LCD Backlight
- Large Signs
- General Lighting
- Architectural Lighting
- Camera/Cell Phone Flash
- Flashlights

The PSoC Core

The PSoC Core is a powerful engine that supports a rich instruction set. It encompasses SRAM for data storage, an interrupt controller, sleep and watchdog timers, and an internal main oscillator (IMO) and an internal low-speed oscillator (ILO). The CPU core, called the M8C, is a powerful, four-million instructions per second (MIPS), 8-bit Harvard-architecture microprocessor with speeds up to 24 MHz.

System resources provide additional capability, such as digital clocks to increase the flexibility of the PSoC; I^2C functionality for implementing an I^2C master, slave, or multi-master; an internal voltage reference that provides an absolute value of 1.3 V to a number of PSoC subsystems; a switch mode pump (SMP) that generates normal operating voltages off a single battery cell; and various system resets supported by the M8C.

The digital system is composed of an array of digital blocks, which can be configured into any number of digital peripherals. The digital blocks can be connected to the GPIO through a series of global busses that can route any signal to any pin, freeing designers from the constraints of a fixed peripheral controller.

The analog system consists of four analog blocks, supporting comparators, and analog-to-digital conversion up to 10 bits of precision.

The Digital System

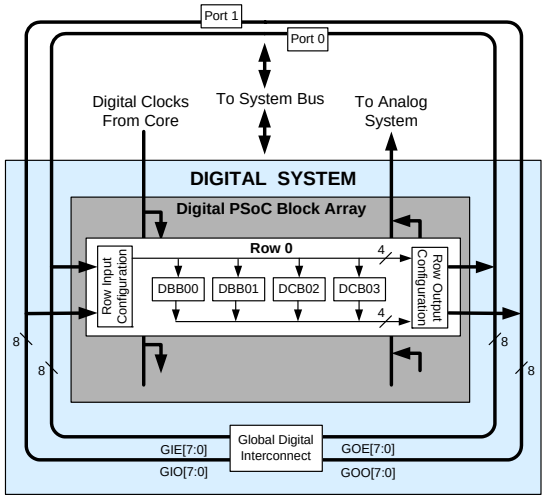
The digital system is composed of four digital PSoC blocks. Each block is an 8-bit resource that can be used alone or combined with other blocks to form 8-, 16-, 24-, and 32-bit peripherals, which are called user modules. Digital peripheral configurations include those listed below.

- PrISM (8- to 32-bit)
- PWMs (8- to 32-bit)
- PWMs with dead band (8- to 32-bit)
- Counters (8- to 32-bit)
- Timers (8- to 32-bit)
- UART 8-bit with selectable parity
- SPI master and slave
- I^2C slave, master, multi-master (one available as a system resource)
- Cyclical redundancy checker (CRC)/generator (8- to 32-bit)
- IrDA (up to four)
- Generators (8- to 32-bit)

Connect the digital blocks to any GPIO through a series of global busses that can route any signal to any pin. The buses also allow for signal multiplexing and for performing logic operations. This configurability frees your designs from the constraints of a fixed peripheral controller.

Digital blocks are provided in rows of four, where the number of blocks varies by device family. This allows you the optimum choice of system resources for your application. Family resources are shown in the table titled EZ-Color Device Characteristics.

Figure 1. Digital System Block Diagram



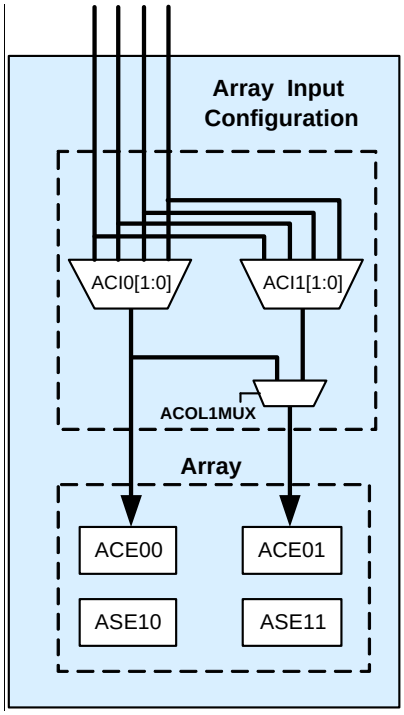
The Analog System

The analog system is composed of four configurable blocks that enable creation of complex analog signal flows. Analog peripherals are very flexible and can be customized to support specific application requirements. Some of the more common EZ-Color analog functions (most available as user modules) are listed below.

- ADCs (single or dual, with 10-bit resolution)
- Pin-to-pin comparators (1)
- Single-ended comparators (up to two) with absolute (1.3-V) reference or 8-bit DAC reference
- 1.3-V reference (as a system resource)

In most PSoC based devices, analog blocks are provided in columns of three, which includes one continuous time (CT) and two switched capacitor (SC) blocks. This particular EZ-Color device provides limited functionality Type E analog blocks. Each column contains one CT block and one SC block.

Figure 2. Analog System Block Diagram



Additional System Resources

System resources, some of which have been previously listed, provide additional capability useful to complete systems. Additional resources include:

- Digital clock dividers provide three customizable clock frequencies for use in applications. The clocks can be routed to both the digital and analog systems. Additional clocks can be generated using digital blocks as clock dividers.
- The I^2C module provides 100- and 400-kHz communication over two wires. Slave, master, and multi-master modes are all supported.
- Low-voltage detect (LVD) interrupts can signal the application of falling voltage levels, while the advanced power-on reset (POR) circuit eliminates the need for a system supervisor.
- An internal 1.3-V voltage reference provides an absolute reference for the analog system, including ADCs and DACs.
- An integrated switch mode pump generates normal operating voltages from a single 1.2-V battery cell, providing a low cost boost converter.

EZ-Color Device Characteristics

Depending on your EZ-Color device characteristics, the digital, and analog systems can have 16, 8, or 4 digital blocks and 12, 6, or 4 analog blocks. The following table lists the resources available for specific EZ-Color device groups. The device covered by this data sheet is shown in the highlighted row of the table.

Table 1. EZ-Color Device Characteristics

Part Number	LED Channels	Digital I/O	Digital Rows	Digital Blocks	Analog Inputs	Analog Outputs	Analog Columns	Analog Blocks	SRAM Size	Flash Size	CapSense®
CY8CLED02	2	16	1	4	8	0	2	4	256 Bytes	4K	No
CY8CLED04	4	56	1	4	48	2	2	6	1K	16K	Yes
CY8CLED08	8	44	2	8	12	4	4	12	256 Bytes	16K	No
CY8CLED16	16	44	4	16	12	4	4	12	2K	32K	No

Getting Started

The quickest path to understanding the EZ-Color silicon is by reading this datasheet and using the PSoC Designer integrated development environment (IDE). This datasheet is an overview of the EZ-Color integrated circuit and presents specific pin, register, and electrical specifications.

For up-to-date ordering, packaging, and electrical specification information, reference the latest device datasheets on the cypress website at http://www.cypress.com.

Application Notes

Cypress application notes are an excellent introduction to the wide variety of possible PSoC designs.

Development Kits

PSoC Development Kits are available online from and through a growing number of regional and global distributors, which include Arrow, Avnet, Digi-Key, Farnell, Future Electronics, and Newark.

Training

Free PSoC technical training (on demand, webinars, and workshops), which is available online via www.cypress.com, covers a wide variety of topics and skill levels to assist you in your designs.

CYPros Consultants

Certified PSoC consultants offer everything from technical assistance to completed PSoC designs. To contact or become a PSoC consultant go to the CYPros Consultants website.

Solutions Library

Visit our growing library of solution focused designs. Here you can find various application designs that include firmware and hardware design files that enable you to complete your designs quickly.

Technical Support

Technical support – including a searchable Knowledge Base articles and technical forums – is also available online. If you cannot find an answer to your question, call our Technical Support hotline at 1-800-541-4736.

Development Tools

PSoC Designer™ is the revolutionary integrated design environment (IDE) that you can use to customize PSoC to meet your specific application requirements. PSoC Designer software accelerates system design and time to market. Develop your applications using a library of precharacterized analog and digital peripherals (called user modules) in a drag-and-drop design environment. Then, customize your design by leveraging the dynamically generated application programming interface (API) libraries of code. Finally, debug and test your designs with the integrated debug environment, including in-circuit emulation and standard software debug features. PSoC Designer includes:

- Application editor graphical user interface (GUI) for device and user module configuration and dynamic reconfiguration
- Extensive user module catalog
- Integrated source-code editor (C and assembly)
- Free C compiler with no size restrictions or time limits
- Built-in debugger
- In-circuit emulation
- Built-in support for communication interfaces:
  - Hardware and software I^2C slaves and masters
  - Full-speed USB 2.0
  - Up to four full-duplex universal asynchronous receiver/transmitters (UARTs), SPI master and slave, and wireless

PSoC Designer supports the entire library of PSoC 1 devices and runs on Windows XP, Windows Vista, and Windows 7.

PSoC Designer Software Subsystems

Design Entry

In the chip-level view, choose a base device to work with. Then select different onboard analog and digital components that use the PSoC blocks, which are called user modules. Examples of user modules are analog-to-digital converters (ADCs), digital-to-analog converters (DACs), amplifiers, and filters. Configure the user modules for your chosen application and connect them to each other and to the proper pins. Then generate your project. This prepopulates your project with APIs and libraries that you can use to program your application.

The tool also supports easy development of multiple configurations and dynamic reconfiguration. Dynamic reconfiguration makes it possible to change configurations at run time. In essence, this lets you to use more than 100 percent of PSoC's resources for an application.

Code Generation Tools

The code generation tools work seamlessly within the PSoC Designer interface and have been tested with a full range of debugging tools. You can develop your design in C, assembly, or a combination of the two.

Assemblers. The assemblers allow you to merge assembly code seamlessly with C code. Link libraries automatically use absolute addressing or are compiled in relative mode, and linked with other software modules to get absolute addressing.

C Language Compilers. C language compilers are available that support the PSoC family of devices. The products allow you to create complete C programs for the PSoC family devices. The optimizing C compilers provide all of the features of C, tailored to the PSoC architecture. They come complete with embedded libraries providing port and bus operations, standard keypad and display support, and extended math functionality.

Debugger

PSoC Designer has a debug environment that provides hardware in-circuit emulation, allowing you to test the program in a physical system while providing an internal view of the PSoC device. Debugger commands allow you to read and program and read and write data memory, and read and write I/O registers. You can read and write CPU registers, set and clear breakpoints, and provide program run, halt, and step control. The debugger also lets you to create a trace buffer of registers and memory locations of interest.

Online Help System

The online help system displays online, context-sensitive help. Designed for procedural and quick reference, each functional subsystem has its own context-sensitive help. This system also provides tutorials and links to FAQs and an Online Support Forum to aid the designer.

In-Circuit Emulator

A low-cost, high-functionality in-circuit emulator (ICE) is available for development support. This hardware can program single devices.

The emulator consists of a base unit that connects to the PC using a USB port. The base unit is universal and operates with all PSoC devices. Emulation pods for each device family are available separately. The emulation pod takes the place of the PSoC device in the target board and performs full-speed (24 MHz) operation.

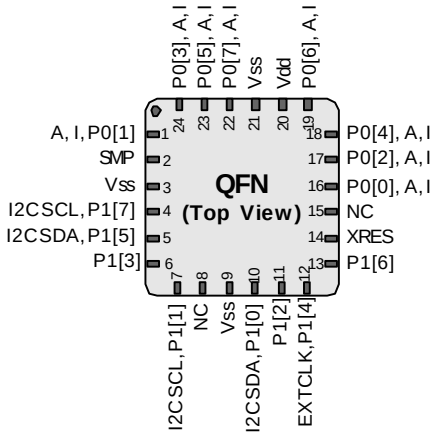
24-Pin Part Pinout

Table 4. 24-Pin Part Pinout (QFN)[2]

Pin No.	Type		Name	Description
	Digital	Analog		
1	I/O	I	P0[1]	Analog column mux input.
2	Power		SMP	SMP connection to required external components.
3	Power		V_{SS}	Ground connection.
4	I/O	–	P1[7]	I^2C SCL.
5	I/O	–	P1[5]	I^2C SDA.
6	I/O	–	P1[3]	–
7	I/O	–	P1[1]	I^2C SCL, ISSP-SCLK[1].
8			NC	No connection.
9	Power		V_{SS}	Ground connection.
10	I/O	–	P1[0]	I^2C SDA, ISSP-SDATA[1].
11	I/O	–	P1[2]	–
12	I/O	–	P1[4]	Optional external clock input (EXTCLK).
13	I/O	–	P1[6]	
14	Input		XRES	Active high external reset with internal pull down.
15			NC	No connection.
16	I/O	I	P0[0]	Analog column mux input.
17	I/O	I	P0[2]	Analog column mux input.
18	I/O	I	P0[4]	Analog column mux input.
19	I/O	I	P0[6]	Analog column mux input.
20	Power		V_{DD}	Supply voltage.
21	Power		V_{SS}	Ground connection.
22	I/O	I	P0[7]	Analog column mux input.
23	I/O	I	P0[5]	Analog column mux input.
24	I/O	I	P0[3]	Analog column mux input.

LEGEND A = Analog, I = Input, and O = Output.

Figure 5. 24-Pin EZ-Color Device



Notes
1. These are the ISSP pins, which are not High Z at power-on reset (POR).
2. The center pad on the QFN package should be connected to ground (V_{SS}) for best mechanical, thermal, and electrical performance. If not connected to ground, it should be electrically floated and not connected to any other signal.

Table 6. Register Map Bank 0: User Space

Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access	Name	Addr (0,Hex)	Access
PRT0DR	00	RW		40		ASE10CR0	80	RW		C0	
PRT0IE	01	RW		41			81			C1	
PRT0GS	02	RW		42			82			C2	
PRT0DM2	03	RW		43			83			C3	
PRT1DR	04	RW		44		ASE11CR0	84	RW		C4	
PRT1IE	05	RW		45			85			C5	
PRT1GS	06	RW		46			86			C6	
PRT1DM2	07	RW		47			87			C7	
	08			48			88			C8	
	09			49			89			C9	
	0A			4A			8A			CA	
	0B			4B			8B			CB	
	0C			4C			8C			CC	
	0D			4D			8D			CD	
	0E			4E			8E			CE	
	0F			4F			8F			CF	
	10			50			90			D0	
	11			51			91			D1	
	12			52			92			D2	
	13			53			93			D3	
	14			54			94			D4	
	15			55			95			D5	
	16			56			96		I2C_CFG	D6	RW
	17			57			97		I2C_SCR	D7	#
	18			58			98		I2C_DR	D8	RW
	19			59			99		I2C_MSCR	D9	#
	1A			5A			9A		INT_CLR0	DA	RW
	1B			5B			9B		INT_CLR1	DB	RW
	1C			5C			9C			DC	
	1D			5D			9D		INT_CLR3	DD	RW
	1E			5E			9E		INT_MSK3	DE	RW
	1F			5F			9F			DF	
DBB00DR0	20	#	AMX_IN	60	RW		A0		INT_MSK0	E0	RW
DBB00DR1	21	W		61			A1		INT_MSK1	E1	RW
DBB00DR2	22	RW	PWM_CR	62	RW		A2		INT_VC	E2	RC
DBB00CR0	23	#		63			A3		RES_WDT	E3	W
DBB01DR0	24	#	CMP_CR0	64	#		A4			E4	
DBB01DR1	25	W		65			A5			E5	
DBB01DR2	26	RW	CMP_CR1	66	RW		A6		DEC_CR0	E6	RW
DBB01CR0	27	#		67			A7		DEC_CR1	E7	RW
DCB02DR0	28	#	ADC0_CR	68	#		A8			E8	
DCB02DR1	29	W	ADC1_CR	69	#		A9			E9	
DCB02DR2	2A	RW		6A			AA			EA	
DCB02CR0	2B	#		6B			AB			EB	
DCB03DR0	2C	#	TMP_DR0	6C	RW		AC			EC	
DCB03DR1	2D	W	TMP_DR1	6D	RW		AD			ED	
DCB03DR2	2E	RW	TMP_DR2	6E	RW		AE			EE	
DCB03CR0	2F	#	TMP_DR3	6F	RW		AF			EF	
	30			70		RDI0RI	B0	RW		F0	
	31			71		RDI0SYN	B1	RW		F1	
	32		ACE00CR1	72	RW	RDI0IS	B2	RW		F2	
	33		ACE00CR2	73	RW	RDI0LT0	B3	RW		F3	
	34			74		RDI0LT1	B4	RW		F4	
	35			75		RDI0RO0	B5	RW		F5	
	36		ACE01CR1	76	RW	RDI0RO1	B6	RW		F6	
	37		ACE01CR2	77	RW		B7		CPU_F	F7	RL
	38			78			B8			F8	
	39			79			B9			F9	
	3A			7A			BA			FA	
	3B			7B			BB			FB	
	3C			7C			BC			FC	
	3D			7D			BD			FD	
	3E			7E			BE		CPU_SCR1	FE	#
	3F			7F			BF		CPU_SCR0	FF	#

Blank fields are Reserved and should not be accessed. # Access is bit specific.

Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

Symbol	Description	Min	Typ	Max	Units	Notes
T_{STG}	Storage temperature	–55	25	+100	°C	Higher storage temperatures reduce data retention time. Recommended storage temperature is +25 °C ± 25 °C. Extended duration storage temperatures above 65 °C degrade reliability.
$T_{BAKETEMP}$	Bake temperature	–	125	See package label	°C	
$T_{BAKETIME}$	Bake Time	See package label	–	72	Hours	
T_A	Ambient temperature with power applied	–40	–	+85	°C	
V_{DD}	Supply voltage on V_{DD} relative to V_{SS}	–0.5	–	+6.0	V	
V_{IO}	DC input voltage	V_{SS} - 0.5	–	V_{DD} + 0.5	V	
V_{IOZ}	DC voltage applied to tri-state	V_{SS} - 0.5	–	V_{DD} + 0.5	V	
I_{MIO}	Maximum current into any port pin	–25	–	+50	mA	
ESD	Electrostatic discharge voltage	2000	–	–	V	Human Body Model ESD.
LU	Latch up current	–	–	200	mA	

Operating Temperature

Table 9. Operating Temperature

Symbol	Description	Min	Typ	Max	Units	Notes
T_A	Ambient temperature	–40	–	+85	°C	
T_J	Junction temperature	–40	–	+100	°C	The temperature rise from ambient to junction is package specific. See Thermal Impedances on page 34. You must limit the power consumption to comply with this requirement.

DC Electrical Characteristics

DC Chip-Level Specifications

Table 10 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 10. DC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DD}	Supply voltage	2.40	–	5.25	V	See DC POR and LVD specifications, Table 18 on page 20.
I_{DD}	Supply current, IMO = 24 MHz	–	3	4	mA	Conditions are V_{DD} = 5.0 V, 25 °C, CPU = 3 MHz, SYSCLK doubler disabled. VC1 = 1.5 MHz, VC2 = 93.75 kHz, VC3 = 0.366 kHz.
I_{DD3}	Supply current, IMO = 6 MHz	–	1.2	2	mA	Conditions are V_{DD} = 3.3 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{DD27}	Supply current, IMO = 6 MHz	–	1.1	1.5	mA	Conditions are V_{DD} = 2.55 V, 25 °C, CPU = 3 MHz, clock doubler disabled. VC1 = 375 kHz, VC2 = 23.4 kHz, VC3 = 0.091 kHz.
I_{SB27}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active. Mid temperature range.	–	2.6	4	µA	V_{DD} = 2.55 V, 0 °C to 40 °C.
I_{SB}	Sleep (mode) current with POR, LVD, Sleep Timer, WDT, and internal slow oscillator active.	–	2.8	5	µA	V_{DD} = 3.3 V, -40 °C ≤ T_A ≤ 85 °C.
V_{REF}	Reference voltage (Bandgap)	1.28	1.30	1.32	V	Trimmed for appropriate V_{DD}. V_{DD} = 3.0 V to 5.25 V.
V_{REF27}	Reference voltage (Bandgap)	1.16	1.30	1.330	V	Trimmed for appropriate V_{DD}. V_{DD} = 2.4 V to 3.0 V.
AGND	Analog ground	V_{REF} - 0.003	V_{REF}	V_{REF} + 0.003	V	

Table 12 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C. Typical parameters are measured at 2.7 V at 25 °C and are for design guidance only.

Table 12. 2.7-V DC GPIO Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
R_{PU}	Pull-up resistor	4	5.6	8	kΩ	
R_{PD}	Pull-down resistor	4	5.6	8	kΩ	
V_{OH}	High output level	V_{DD} - 0.4	–	–	V	I_{OH} = 2.5 mA (6.25 typical), V_{DD} = 2.4 to 3.0 V (16 mA maximum, 50 mA typical combined I_{OH} budget).
V_{OL}	Low output level	–	–	0.75	V	I_{OL} = 10 mA, V_{DD} = 2.4 to 3.0 V (90 mA maximum combined I_{OL} budget).
I_{OH}	High level source current	2.5	–	–	mA	V_{OH} = V_{DD}-0.4 V. See the limitations of the total current in the Note for V_{OH}.
I_{OL}	Low Level Sink Current	10	–	–	mA	V_{OL} = 0.75 V. See the limitations of the total current in the Note for VOL.
V_{IL}	Input low level	–	–	0.75	V	V_{DD} = 2.4 to 3.0.
V_{IH}	Input high level	2.0	–	–	V	V_{DD} = 2.4 to 3.0.
V_H	Input hysteresis	–	60	–	mV	
I_{IL}	Input leakage (absolute value)	–	1	–	nA	Gross tested to 1 μA.
C_{IN}	Capacitive load on pins as input	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.
C_{OUT}	Capacitive load on pins as output	–	3.5	10	pF	Package and pin dependent. Temp = 25 °C.

DC Amplifier Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 13. 5-V DC Amplifier Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{OSOA}	Input offset voltage (absolute value)	–	2.5	15	mV	
TCV_{OSOA}	Average input offset voltage drift	–	10	–	μV/°C	
I_{EBOA}	Input leakage current (Port 0 analog pins)	–	200	–	pA	Gross tested to 1 μA.
C_{INOA}	Input capacitance (Port 0 analog pins)	–	4.5	9.5	pF	Package and pin dependent. Temp = 25 °C.
V_{CMOA}	Common mode voltage range	0.0	–	V_{DD} - 1	V	
G_{OLOA}	Open loop gain	80	–	–	dB	
I_{SOA}	Amplifier supply current	–	10	30	μA	

DC Programming Specifications

Table 19 lists guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 19. DC Programming Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
V_{DDP}	V_{DD} for programming and erase	4.5	5.0	5.5	V	This specification applies to the functional requirements of external programmer tools
V_{DDLV}	Low V_{DD} for verify	3.0	3.1	3.2	V	This specification applies to the functional requirements of external programmer tools
V_{DDHV}	High V_{DD} for verify	5.1	5.2	5.3	V	This specification applies to the functional requirements of external programmer tools
$V_{DDIWRITE}$	Supply voltage for flash write operations	3.0	–	5.25	V	This specification applies to this device when it is executing internal flash writes
I_{DDP}	Supply current during programming or verify	–	5	25	mA	
V_{ILP}	Input low voltage during programming or verify	–	–	0.8	V	
V_{IHP}	Input high voltage during programming or verify	2.2	–	–	V	
I_{ILP}	Input current when applying V_{ILP} to P1[0] or P1[1] during programming or verify	–	–	0.2	mA	Driving internal pull-down resistor.
I_{IHP}	Input current when applying V_{IHP} to P1[0] or P1[1] during programming or verify	–	–	1.5	mA	Driving internal pull-down resistor.
V_{OLV}	Output low voltage during programming or verify	–	–	V_{SS} + 0.75	V	
V_{OHV}	Output high voltage during programming or verify	V_{DD} - 1.0	–	V_{DD}	V	
$Flash_{ENPB}$	Flash endurance (per block)	50,000[8]	–	–	–	Erase/write cycles per block.
$Flash_{ENT}$	Flash endurance (total)[9]	1,800,000	–	–	–	Erase/write cycles.
$Flash_{DR}$	Flash data retention	10	–	–	Years	

DC I^2C Specifications

Table 20 lists the guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 20. DC I^2C Specifications[10]

Symbol	Description	Min	Typ	Max	Units	Notes
V_{ILI2C}	Input low level	–	–	0.3 × V_{DD}	V	3.0 V ≤ V_{DD} ≤ 3.6 V
		–	–	0.25 × V_{DD}	V	4.75 V ≤ V_{DD} ≤ 5.25 V
V_{IHI2C}	Input high level	0.7 × V_{DD}	–	–	V	3.0 V ≤ V_{DD} ≤ 5.25 V

Notes

8. The 50,000 cycle flash endurance per block will only be guaranteed if the flash is operating within one voltage range. Voltage ranges are 2.4 V to 3.0 V, 3.0 V to 3.6 V, and 4.75 V to 5.25 V.
9. A maximum of 36 x 50,000 block endurance cycles is allowed. This may be balanced between operations on 36x1 blocks of 50,000 maximum cycles each, 36x2 blocks of 25,000 maximum cycles each, or 36x4 blocks of 12,500 maximum cycles each (to limit the total number of cycles to 36x50,000 and that no single block ever sees more than 50,000 cycles).
   For the full industrial range, you must employ a temperature sensor user module (FlashTemp) and feed the result to the temperature argument before writing. Refer to the flash APIs Application Note AN2015 at http://www.cypress.com under Application Notes for more information.
10. All GPIO meet the DC GPIO V_{IL} and V_{IH} specifications mentioned in section DC General Purpose I/O Specifications on page 16. The I^2C GPIO pins also meet the mentioned specs.

Table 22. 2.7-V AC Chip-Level Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{IMO12}	IMO frequency for 12 MHz	11.5	12	12.7[15]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{IMO6}	IMO frequency for 6 MHz	5.5	6	6.5[15]	MHz	Trimmed for 2.7 V operation using factory trim values. See Figure 6 on page 13. SLIMO mode = 1.
F_{CPU1}	CPU frequency (2.7 V nominal)	0.093	3	3.15[15]	MHz	24 MHz only for SLIMO mode = 0.
F_{BLK27}	Digital PSoC block frequency (2.7 V nominal)	0	12	12.5[15]	MHz	Refer to the section AC Digital Block Specifications on page 26.
F_{32K1}	ILO frequency	8	32	96	kHz	
F_{32K_U}	ILO untrimmed frequency	5	–	100	kHz	After a reset and before the M8C starts to run, the ILO is not trimmed. See the system resets section of the PSoC Technical Reference Manual for details on this timing.
t_{XRST}	External reset pulse width	10	–	–	µs	
DC_{ILO}	ILO duty cycle	20	50	80	%	
F_{MAX}	Maximum frequency of signal on row input or row output	–	–	12.3	MHz	
SR_{POWER_UP}	Power supply slew rate	–	–	250	V/ms	V_{DD} slew rate during power up.
$t_{POWERUP}$	Time from end of POR to CPU executing code	–	16	100	ms	Power up from 0 V. See the system resets section of the PSoC Technical Reference Manual.
t_{jit_IMO}	12-MHz IMO cycle-to-cycle jitter (RMS)[16]	–	400	1000	ps	
	12-MHz IMO long term N cycle-to-cycle jitter (RMS)[16]	–	600	1300	ps	N = 32
	12-MHz IMO period jitter (RMS)[16]	–	100	500	ps	

Notes
15. 2.4 V < V_{DD} < 3.0 V.
16. Refer to the application note, Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 for more information on jitter specifications.

AC Digital Block Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, or 2.4 V to 3.0 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 28. 5-V and 3.3-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Unit	Notes
All functions	Block input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Timer	Input clock frequency					
	No capture, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No capture, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With capture	–	–	24.6	MHz	
	Capture pulse width	50[17]	–	–	ns	
Counter	Input clock frequency					
	No enable input, V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	No enable input, V_{DD} < 4.75 V	–	–	24.6	MHz	
	With enable input	–	–	24.6	MHz	
	Enable input pulse width	50[17]	–	–	ns	
Dead Band	Kill pulse width					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	50[17]	–	–	ns	
	Disable mode	50[17]	–	–	ns	
	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (PRS Mode)	Input clock frequency					
	V_{DD} ≥ 4.75 V	–	–	49.2	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	24.6	MHz	
SPIM	Input clock frequency	–	–	8.2	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input clock (SCLK) frequency	–	–	4.1	MHz	The input clock is the SPI SCLK in SPIS mode.
	Width of SS_negated between transmissions	50[17]	–	–	ns	
Transmitter	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	
Receiver	Input clock frequency					The baud rate is equal to the input clock frequency divided by 8.
	V_{DD} ≥ 4.75 V, 2 stop bits	–	–	49.2	MHz	
	V_{DD} ≥ 4.75 V, 1 stop bit	–	–	24.6	MHz	
	V_{DD} < 4.75 V	–	–	24.6	MHz	

Note
17. 50 ns minimum input pulse width is based on the input synchronizers running at 24 MHz (42 ns nominal period).

Table 29. 2.7-V AC Digital Block Specifications

Function	Description	Min	Typ	Max	Units	Notes
All Functions	Block input clock frequency			12.7	MHz	2.4 V < V_{DD} < 3.0 V.
Timer	Capture pulse width	100[18]	–	–	ns	
	Input clock frequency, with or without Capture	–	–	12.7	MHz	
Counter	Enable input pulse width	100	–	–	ns	
	Input clock frequency, no enable input	–	–	12.7	MHz	
	Input clock frequency, enable input	–	–	12.7	MHz	
Dead Band	Kill pulse width:					
	Asynchronous restart mode	20	–	–	ns	
	Synchronous restart mode	100	–	–	ns	
	Disable mode	100	–	–	ns	
	Input clock frequency	–	–	12.7	MHz	
CRCPRS (PRS Mode)	Input clock frequency	–	–	12.7	MHz	
CRCPRS (CRC Mode)	Input clock frequency	–	–	12.7	MHz	
SPIM	Input clock frequency	–	–	6.35	MHz	The SPI serial clock (SCLK) frequency is equal to the input clock frequency divided by 2.
SPIS	Input Clock (SCLK) Frequency	–	–	4.1	MHz	
	Width of SS_ Negated between transmissions	100	–	–	ns	
Transmitter	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.
Receiver	Input clock frequency	–	–	12.7	MHz	The baud rate is equal to the input clock frequency divided by 8.

AC External Clock Specifications

The following tables list guaranteed maximum and minimum specifications for the voltage and temperature ranges: 4.75 V to 5.25 V and –40 °C ≤ T_A ≤ 85 °C, or 3.0 V to 3.6 V and –40 °C ≤ T_A ≤ 85 °C, respectively. Typical parameters are measured at 5 V, 3.3 V, or 2.7 V at 25 °C and are for design guidance only.

Table 30. 5-V AC External Clock Specifications

Symbol	Description	Min	Typ	Max	Units	Notes
F_{OSCEXT}	Frequency	0.093	–	24.6	MHz	
–	High period	20.6	–	5300	ns	
–	Low period	20.6	–	–	ns	
–	Power up IMO to switch	150	–	–	µs	

Note
18. 100 ns minimum input pulse width is based on the input synchronizers running at 12 MHz (84 ns nominal period).

Packaging Information

This section illustrates the packaging specifications for the CY8CLED02 EZ-Color device, along with the thermal impedances for each package and minimum solder reflow peak temperature.

Important Note Emulation tools may require a larger area on the target PCB than the chip's footprint. For a detailed description of the emulation tools' dimensions, refer to the emulator pod drawings at http://www.cypress.com.

Figure 10. 8-Pin (150-Mil) SOIC

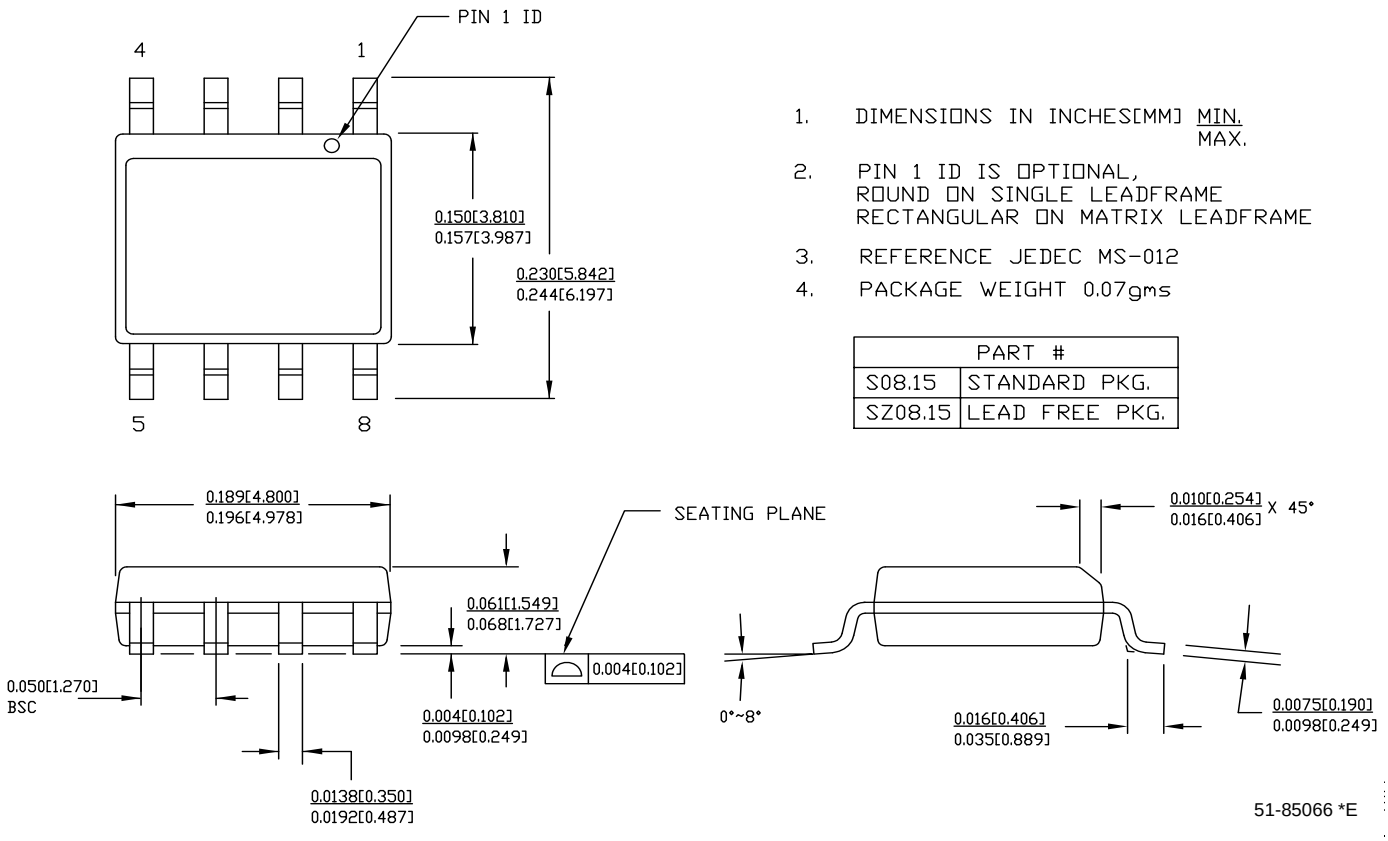


Figure 11. 16-Pin (150-Mil) SOIC

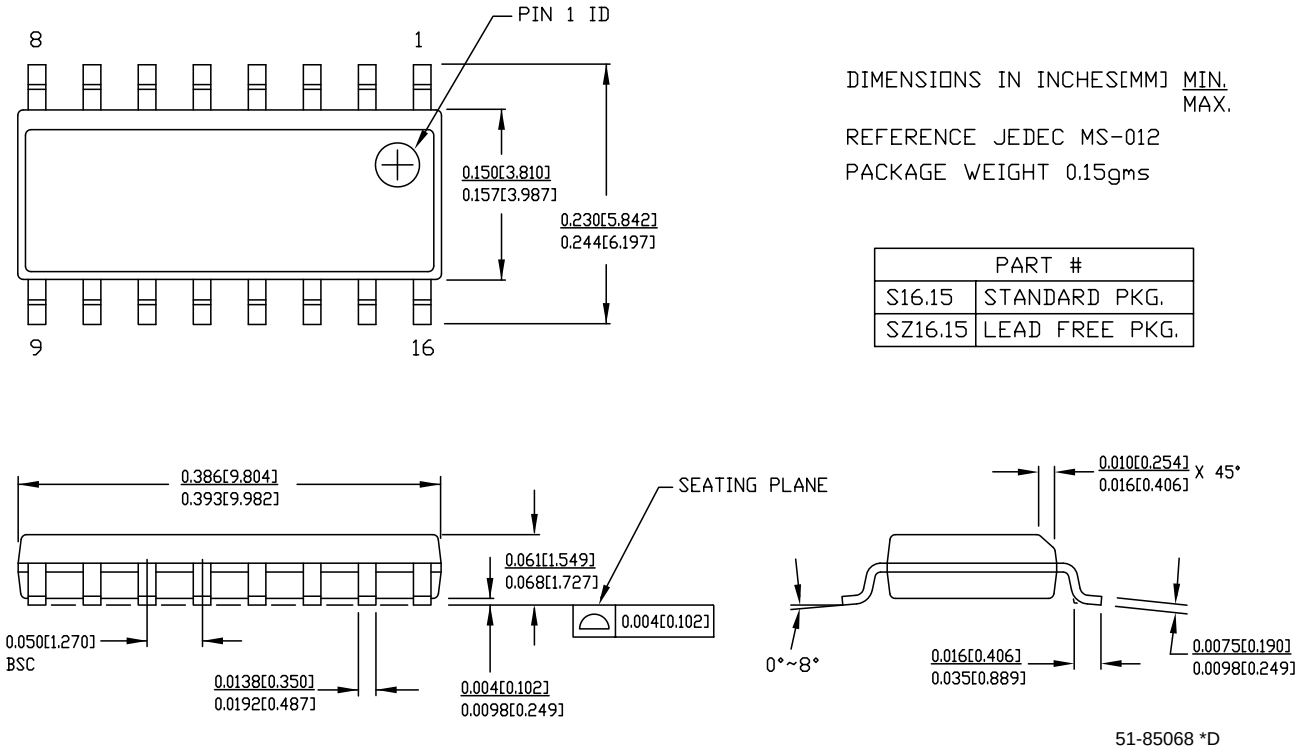
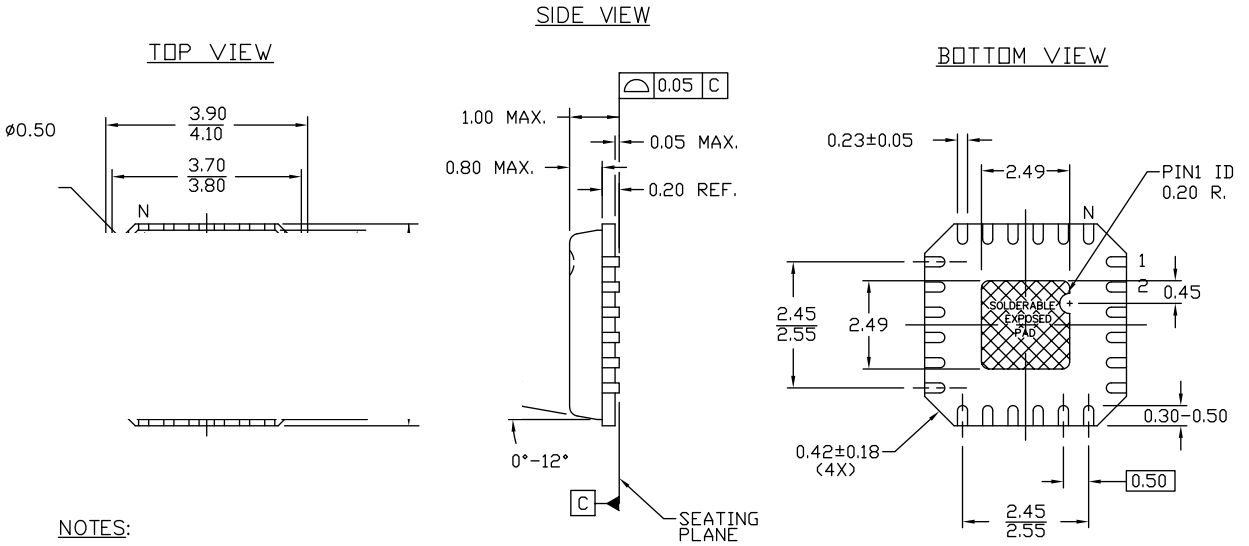


Figure 12. 24-Pin (4x4) QFN



NOTES:

1. HATCH IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 0.042g
4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
5. PACKAGE CODE

PART #	DESCRIPTION
LF24A	STANDARD
LY24A	LEAD FREE

51-85203 *C

Acronyms

Table 40 lists the acronyms that are used in this document.

Table 40. Acronyms Used in this Datasheet

Acronym	Description	Acronym	Description
AC	alternating current	LPC	low power comparator
ADC	analog-to-digital converter	MIPS	million instructions per second
API	application programming interface	PCB	printed circuit board
CMOS	complementary metal oxide semiconductor	PDIP	plastic dual-in-line package
CPU	central processing unit	POR	power-on reset
CRC	cyclic redundancy check	PPOR	precision power on reset
CT	continuous time	PRS	pseudo-random sequence
DAC	digital-to-analog converter	PSoC®	Programmable System-on-Chip
DC	direct current	PWM	pulse-width modulator
EEPROM	electrically erasable programmable read-only memory	QFN	quad flat no leads
GPIO	general purpose I/O	SC	switched capacitor
I/O	input/output	SRAM	static random access memory
ICE	in-circuit emulator	SLIMO	slow IMO
IDE	integrated development environment	SMP	switch mode pump
ILO	internal low speed oscillator	SOIC	small-outline integrated circuit
IMO	internal main oscillator	SPI™	serial peripheral interface
IrDA	infrared data association	SROM	supervisory read only memory
ISSP	in-system serial programming	UART	universal asynchronous receiver / transmitter
LCD	liquid crystal display	USB	universal serial bus
LED	light-emitting diode	XRES	external reset
LVD	low-voltage detect	WDT	watchdog timer

Reference Documents

Design Aids – Reading and Writing PSoC® Flash – AN2015 (001-40459)

Understanding Datasheet Jitter Specifications for Cypress Timing Products – AN5054 (001-14503)

Application Notes for Surface Mount Assembly of Amkor's MicroLeadFrame (MLF) Packages – available at http://www.amkor.com.

Document Conventions

Units of Measure

Table 41 lists the units of measure.

Table 41. Units of Measure

Symbol	Unit of Measure	Symbol	Unit of Measure
°C	degree Celsius	µs	microsecond
dB	decibels	µH	micro henry
kHz	kilohertz	ps	picosecond
kΩ	kilo ohm	mV	millivolt
mA	milliampere	V	volt
mH	millihenry	%	percent
MHz	megahertz	µV	microvolt
nA	nano ampere	W	watt
pA	pico ampere	mm	millimeter
pF	picofarad	ns	nanosecond
µA	microampere	mVpp	millivolts peak-to-peak
µF	microfarad	ms	millisecond

Numeric Conventions

Hexadecimal numbers are represented with all letters in uppercase with an appended lowercase ‘h’ (for example, ‘14h’ or ‘3Ah’). Hexadecimal numbers may also be represented by a ‘0x’ prefix, the C coding convention. Binary numbers have an appended lowercase ‘b’ (for example, 01010100b’ or ‘01000011b’). Numbers not indicated by an ‘h’ or ‘b’ are decimals.

Glossary

active high	1. A logic signal having its asserted state as the logic 1 state. 2. A logic signal having the logic 1 state as the higher voltage of the two states.
analog blocks	The basic programmable opamp circuits. These are switched capacitor (SC) and continuous time (CT) blocks. These blocks can be interconnected to provide ADCs, DACs, multi-pole filters, gain stages, and much more.
analog-to-digital (ADC)	A device that changes an analog signal to a digital signal of corresponding magnitude. Typically, an ADC converts a voltage to a digital number. The digital-to-analog (DAC) converter performs the reverse operation.
Application programming interface (API)	A series of software routines that comprise an interface between a computer application and lower level services and functions (for example, user modules and libraries). APIs serve as building blocks for programmers that create software applications.
asynchronous	A signal whose data is acknowledged or acted upon immediately, irrespective of any clock signal.
bandgap reference	A stable voltage reference design that matches the positive temperature coefficient of VT with the negative temperature coefficient of VBE, to produce a zero temperature coefficient (ideally) reference.
bandwidth	1. The frequency range of a message or information processing system measured in hertz. 2. The width of the spectral region over which an amplifier (or absorber) has substantial gain (or loss); it is sometimes represented more specifically as, for example, full width at half maximum.

Glossary (continued)

serial	1. Pertaining to a process in which all events occur one after the other. 2. Pertaining to the sequential or consecutive occurrence of two or more related activities in a single device or channel.
settling time	The time it takes for an output signal or value to stabilize after the input has changed from one value to another.
shift register	A memory storage device that sequentially shifts a word either left or right to output a stream of serial data.
slave device	A device that allows another device to control the timing for data exchanges between two devices. Or when devices are cascaded in width, the slave device is the one that allows another device to control the timing of data exchanges between the cascaded devices and an external interface. The controlling device is called the master device.
SRAM	An acronym for static random access memory. A memory device where you can store and retrieve data at a high rate of speed. The term static is used because, after a value is loaded into an SRAM cell, it remains unchanged until it is explicitly altered or until power is removed from the device.
SROM	An acronym for supervisory read only memory. The SROM holds code that is used to boot the device, calibrate circuitry, and perform flash operations. The functions of the SROM may be accessed in normal user code, operating from flash.
stop bit	A signal following a character or block that prepares the receiving device to receive the next character or block.
synchronous	1. A signal whose data is not acknowledged or acted upon until the next active edge of a clock signal. 2. A system whose operation is synchronized by a clock signal.
tri-state	A function whose output can adopt three states: 0, 1, and Z (high-impedance). The function does not drive any value in the Z state and, in many respects, may be considered to be disconnected from the rest of the circuit, allowing another output to drive the same net.
UART	A UART or universal asynchronous receiver-transmitter translates between parallel bits of data and serial bits.
user modules	Pre-build, pre-tested hardware/firmware peripheral functions that take care of managing and configuring the lower level Analog and Digital PSoC Blocks. User Modules also provide high level *API* for the peripheral function.
user space	The bank 0 space of the register map. The registers in this bank are more likely to be modified during normal program execution and not just during initialization. Registers in bank 1 are most likely to be modified only during the initialization phase of the program.
V_{DD}	A name for a power net meaning "voltage drain." The most positive power supply signal. Usually 5 V or 3.3 V.
V_{SS}	A name for a power net meaning "voltage source." The most negative power supply signal.
Watchdog timer	A timer that must be serviced periodically. If it is not serviced, the CPU resets after a specified period of time.

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