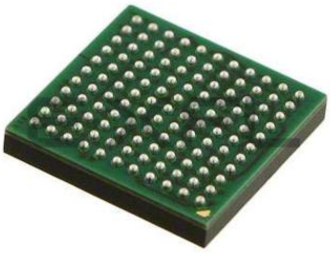
NXP USA Inc. - MK51DX128CMC7 Datasheet



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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	ARM® Cortex®-M4
Core Size	32-Bit Single-Core
Speed	72MHz
Connectivity	I²C, IrDA, SPI, UART/USART, USB, USB OTG
Peripherals	DMA, I²S, LVD, POR, PWM, WDT
Number of I/O	61
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 3.6V
Data Converters	A/D 35x16b; D/A 1x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	121-LFBGA
Supplier Device Package	121-MAPBGA (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/mk51dx128cmc7

3.1.1 Example

This is an example of an operating requirement, which you must meet for the accompanying operating behaviors to be guaranteed:

Symbol	Description	Min.	Max.	Unit
V_{DD}	1.0 V core supply voltage	0.9	1.1	V

3.2 Definition: Operating behavior

An *operating behavior* is a specified value or range of values for a technical characteristic that are guaranteed during operation if you meet the operating requirements and any other specified conditions.

3.2.1 Example

This is an example of an operating behavior, which is guaranteed if you meet the accompanying operating requirements:

Symbol	Description	Min.	Max.	Unit
I_{WP}	Digital I/O weak pullup/ pulldown current	10	130	µA

3.3 Definition: Attribute

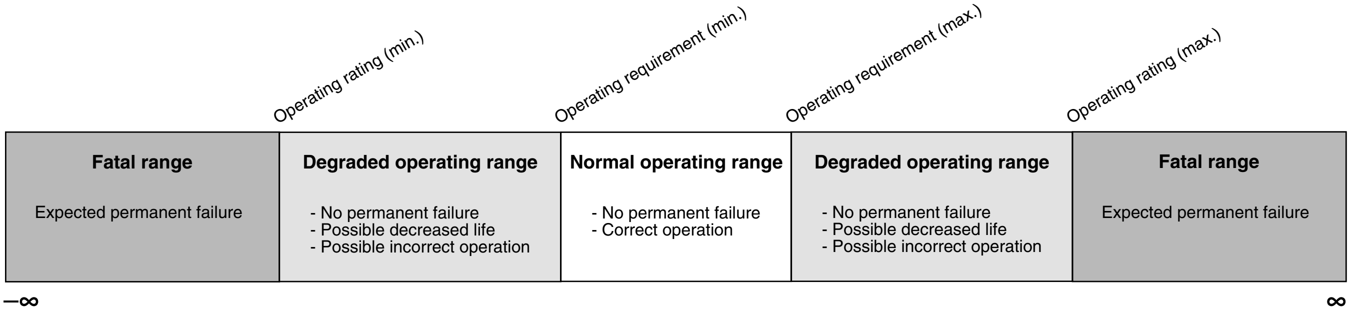
An *attribute* is a specified value or range of values for a technical characteristic that are guaranteed, regardless of whether you meet the operating requirements.

3.3.1 Example

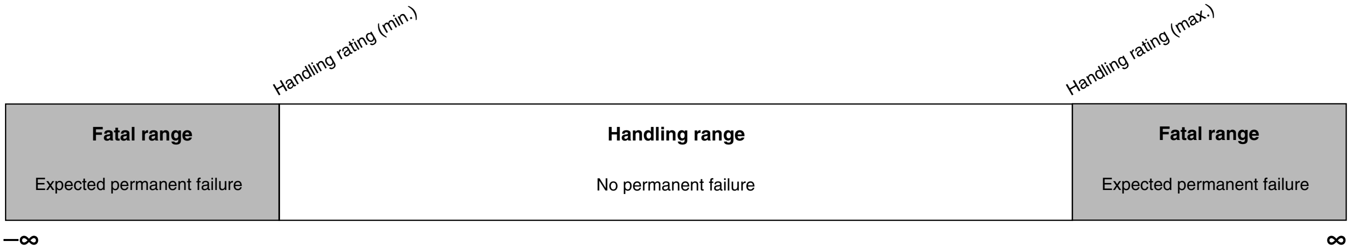
This is an example of an attribute:

Symbol	Description	Min.	Max.	Unit
CIN_D	Input capacitance: digital pins	—	7	pF

3.6 Relationship between ratings and operating requirements



Operating (power on)



Handling (power off)

3.7 Guidelines for ratings and operating requirements

Follow these guidelines for ratings and operating requirements:

- Never exceed any of the chip's ratings.
- During normal operation, don't exceed any of the chip's operating requirements.
- If you must exceed an operating requirement at times other than during normal operation (for example, during power sequencing), limit the duration as much as possible.

3.8 Definition: Typical value

A *typical value* is a specified value for a technical characteristic that:

- Lies within the range of values specified by the operating behavior
- Given the typical manufacturing process, is representative of that characteristic during operation when you meet the typical-value conditions or other specified conditions

Typical values are provided as design guidelines and are neither tested nor guaranteed.

5.2.1 Voltage and current operating requirements

Table 1. Voltage and current operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	3.6	V	
V_{DDA}	Analog supply voltage	1.71	3.6	V	
$V_{DD} – V_{DDA}$	V_{DD}-to-V_{DDA} differential voltage	–0.1	0.1	V	
$V_{SS} – V_{SSA}$	V_{SS}-to-V_{SSA} differential voltage	–0.1	0.1	V	
V_{BAT}	RTC battery supply voltage	1.71	3.6	V	
V_{IH}	Input high voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 0.7 × V_{DD} 0.75 × V_{DD}	 — —	 V V	
V_{IL}	Input low voltage • 2.7 V ≤ V_{DD} ≤ 3.6 V • 1.7 V ≤ V_{DD} ≤ 2.7 V	 — —	 0.35 × V_{DD} 0.3 × V_{DD}	 V V	
V_{HYS}	Input hysteresis	0.06 × V_{DD}	—	V	
I_{ICDIO}	Digital pin negative DC injection current — single pin • $V_{IN} < V_{SS}$-0.3V	-5	—	mA	1
I_{ICAIO}	Analog[2], EXTAL, and XTAL pin DC injection current — single pin • $V_{IN} < V_{SS}$-0.3V (Negative current injection) • $V_{IN} > V_{DD}$+0.3V (Positive current injection)	 -5 —	 — +5	mA	3
I_{ICcont}	Contiguous pin DC injection current —regional limit, includes sum of negative injection currents or sum of positive injection currents of 16 contiguous pins • Negative current injection • Positive current injection	 -25 —	 — +25	mA	
V_{RAM}	V_{DD} voltage required to retain RAM	1.2	—	V	
V_{RFVBAT}	V_{BAT} voltage required to retain the VBAT register file	V_{POR_VBAT}	—	V	

1. All 5 V tolerant digital I/O pins are internally clamped to V_{SS} through a ESD protection diode. There is no diode connection to V_{DD}. If V_{IN} greater than V_{DIO_MIN} (=V_{SS}-0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If this limit cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{DIO\_MIN}-V_{IN})/|I_{IC}|$.
2. Analog pins are defined as pins that do not have an associated general purpose I/O port function.
3. All analog pins are internally clamped to V_{SS} and V_{DD} through ESD protection diodes. If V_{IN} is greater than V_{AIO_MIN} (=V_{SS}-0.3V) and V_{IN} is less than V_{AIO_MAX}(=V_{DD}+0.3V) is observed, then there is no need to provide current limiting resistors at the pads. If these limits cannot be observed then a current limiting resistor is required. The negative DC injection current limiting resistor is calculated as $R=(V_{AIO\_MIN}-V_{IN})/|I_{IC}|$. The positive injection current limiting resistor is calculated as $R=(V_{IN}-V_{AIO\_MAX})/|I_{IC}|$. Select the larger of these two calculated resistances.

5.2.2 LVD and POR operating requirements

Table 2. V_{DD} supply LVD and POR operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR}	Falling VDD POR detect voltage	0.8	1.1	1.5	V	
V_{LVDH}	Falling low-voltage detect threshold — high range (LVDV=01)	2.48	2.56	2.64	V	
	Low-voltage warning thresholds — high range					1
V_{LVW1H}	• Level 1 falling (LVWV=00)	2.62	2.70	2.78	V	
V_{LVW2H}	• Level 2 falling (LVWV=01)	2.72	2.80	2.88	V	
V_{LVW3H}	• Level 3 falling (LVWV=10)	2.82	2.90	2.98	V	
V_{LVW4H}	• Level 4 falling (LVWV=11)	2.92	3.00	3.08	V	
V_{HYSH}	Low-voltage inhibit reset/recover hysteresis — high range	—	±80	—	mV	
V_{LVDL}	Falling low-voltage detect threshold — low range (LVDV=00)	1.54	1.60	1.66	V	
	Low-voltage warning thresholds — low range					1
V_{LVW1L}	• Level 1 falling (LVWV=00)	1.74	1.80	1.86	V	
V_{LVW2L}	• Level 2 falling (LVWV=01)	1.84	1.90	1.96	V	
V_{LVW3L}	• Level 3 falling (LVWV=10)	1.94	2.00	2.06	V	
V_{LVW4L}	• Level 4 falling (LVWV=11)	2.04	2.10	2.16	V	
V_{HYSL}	Low-voltage inhibit reset/recover hysteresis — low range	—	±60	—	mV	
V_{BG}	Bandgap voltage reference	0.97	1.00	1.03	V	
t_{LPO}	Internal low power oscillator period — factory trimmed	900	1000	1100	μs	

1. Rising thresholds are falling threshold + hysteresis voltage

Table 3. VBAT power operating requirements

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{POR_VBAT}	Falling VBAT supply POR detect voltage	0.8	1.1	1.5	V	

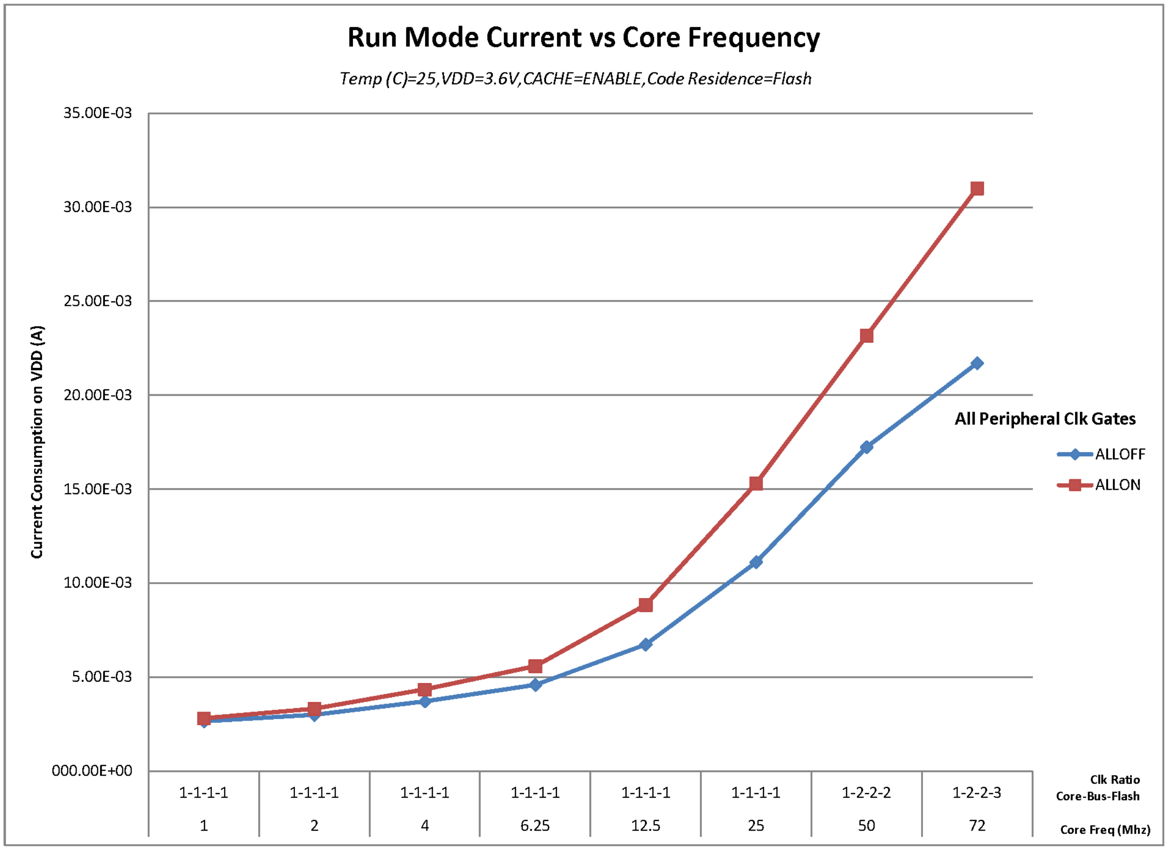


Figure 2. Run mode supply current vs. core frequency

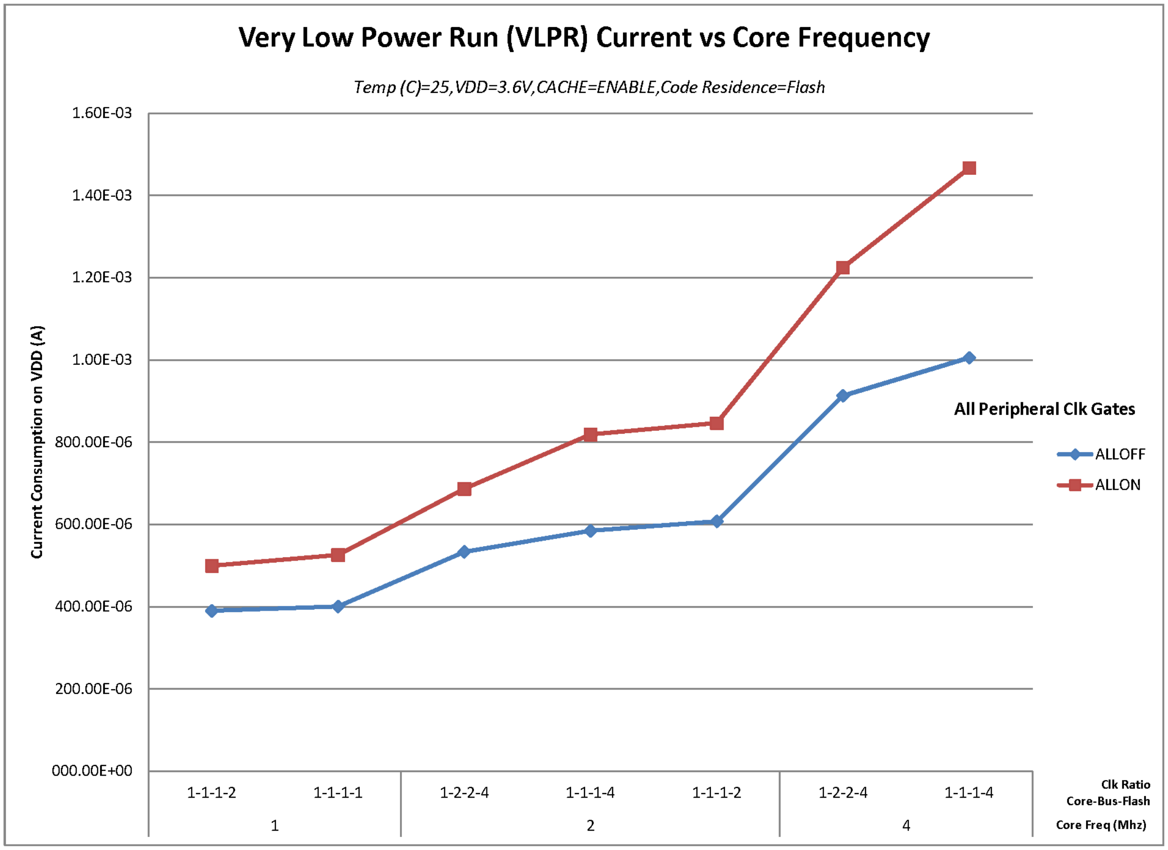


Figure 3. VLPR mode supply current vs. core frequency

5.2.6 Designing with radiated emissions in mind

To find application notes that provide guidance on designing your system to minimize interference from radiated emissions:

1. Go to www.freescale.com.
2. Perform a keyword search for "EMC design."

5.2.7 Capacitance attributes

Table 7. Capacitance attributes

Symbol	Description	Min.	Max.	Unit
C_{IN_A}	Input capacitance: analog pins	—	7	pF
C_{IN_D}	Input capacitance: digital pins	—	7	pF

Table 13. JTAG full voltage range electricals (continued)

Symbol	Description	Min.	Max.	Unit
J5	Boundary scan input data setup time to TCLK rise	20	—	ns
J6	Boundary scan input data hold time after TCLK rise	0	—	ns
J7	TCLK low to boundary scan output data valid	—	25	ns
J8	TCLK low to boundary scan output high-Z	—	25	ns
J9	TMS, TDI input data setup time to TCLK rise	8	—	ns
J10	TMS, TDI input data hold time after TCLK rise	1.4	—	ns
J11	TCLK low to TDO data valid	—	22.1	ns
J12	TCLK low to TDO high-Z	—	22.1	ns
J13	$\overline{\text{TRST}}$ assert time	100	—	ns
J14	$\overline{\text{TRST}}$ setup time (negation) to TCLK high	8	—	ns

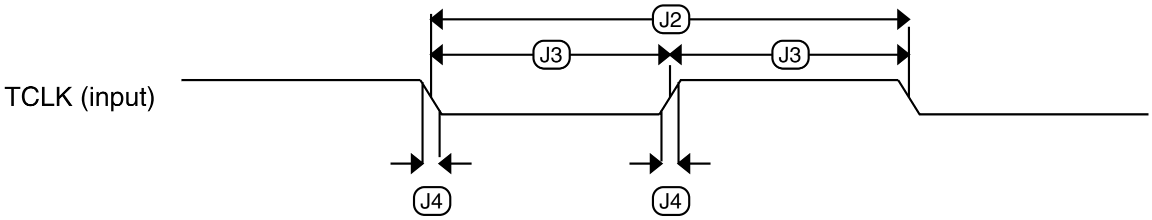


Figure 6. Test clock input timing

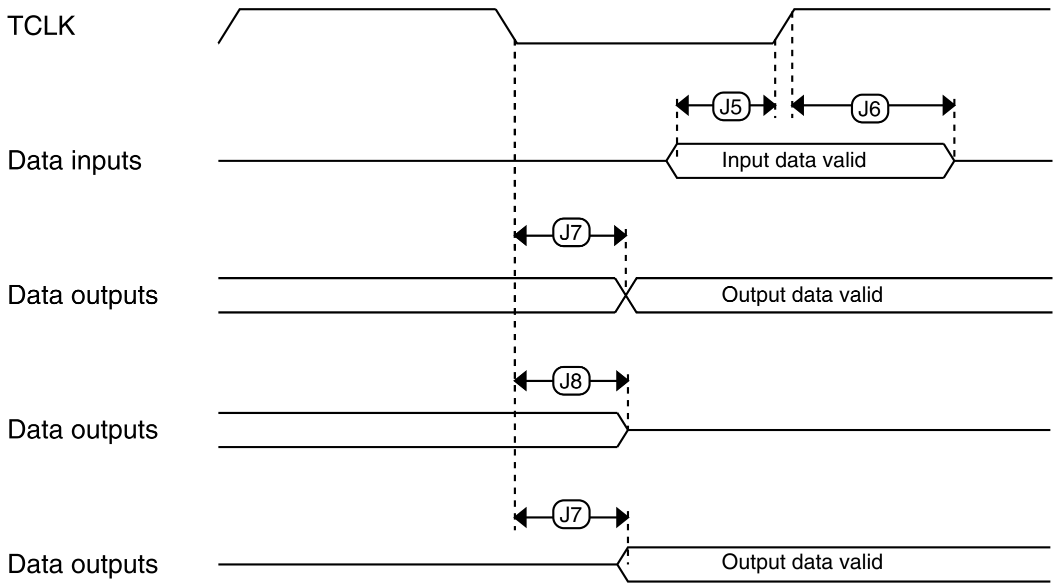


Figure 7. Boundary scan (JTAG) timing

6.3.2.1 Oscillator DC electrical specifications

Table 15. Oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DD}	Supply voltage	1.71	—	3.6	V	
I_{DDOSC}	Supply current — low-power mode (HGO=0)					1
	• 32 kHz	—	500	—	nA	
	• 4 MHz	—	200	—	μA	
	• 8 MHz (RANGE=01)	—	300	—	μA	
	• 16 MHz	—	950	—	μA	
	• 24 MHz	—	1.2	—	mA	
	• 32 MHz	—	1.5	—	mA	
I_{DDOSC}	Supply current — high gain mode (HGO=1)					1
	• 32 kHz	—	25	—	μA	
	• 4 MHz	—	400	—	μA	
	• 8 MHz (RANGE=01)	—	500	—	μA	
	• 16 MHz	—	2.5	—	mA	
	• 24 MHz	—	3	—	mA	
	• 32 MHz	—	4	—	mA	
C_x	EXTAL load capacitance	—	—	—		2, 3
C_y	XTAL load capacitance	—	—	—		2, 3
R_F	Feedback resistor — low-frequency, low-power mode (HGO=0)	—	—	—	MΩ	2, 4
	Feedback resistor — low-frequency, high-gain mode (HGO=1)	—	10	—	MΩ	
	Feedback resistor — high-frequency, low-power mode (HGO=0)	—	—	—	MΩ	
	Feedback resistor — high-frequency, high-gain mode (HGO=1)	—	1	—	MΩ	
R_S	Series resistor — low-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — low-frequency, high-gain mode (HGO=1)	—	200	—	kΩ	
	Series resistor — high-frequency, low-power mode (HGO=0)	—	—	—	kΩ	
	Series resistor — high-frequency, high-gain mode (HGO=1)	—	0	—	kΩ	

Table continues on the next page...

4. Crystal startup time is defined as the time between the oscillator being enabled and the OSCINIT bit in the MCG_S register being set.

NOTE

The 32 kHz oscillator works in low power mode by default and cannot be moved into high power/gain mode.

6.3.3 32 kHz Oscillator Electrical Characteristics

This section describes the module electrical characteristics.

6.3.3.1 32 kHz oscillator DC electrical specifications

Table 17. 32kHz oscillator DC electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit
V_{BAT}	Supply voltage	1.71	—	3.6	V
R_F	Internal feedback resistor	—	100	—	MΩ
C_{para}	Parasitical capacitance of EXTAL32 and XTAL32	—	5	7	pF
V_{pp}[1]	Peak-to-peak amplitude of oscillation	—	0.6	—	V

1. When a crystal is being used with the 32 kHz oscillator, the EXTAL32 and XTAL32 pins should only be connected to required oscillator components and must not be connected to any other devices.

6.3.3.2 32kHz oscillator frequency specifications

Table 18. 32kHz oscillator frequency specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
f_{osc_lo}	Oscillator crystal	—	32.768	—	kHz	
t_{start}	Crystal start-up time	—	1000	—	ms	1
$v_{ec\_extal32}$	Externally provided input clock amplitude	700	—	V_{BAT}	mV	2, 3

1. Proper PC board layout procedures must be followed to achieve specifications.
2. This specification is for an externally supplied clock driven to EXTAL32 and does not apply to any other clock input. The oscillator remains enabled and XTAL32 must be left unconnected.
3. The parameter specified is a peak-to-peak value and V_{IH} and V_{IL} specifications do not apply. The voltage of the applied clock must be within the range of V_{SS} to V_{BAT}.

6.4 Memories and memory interfaces

6.4.1 Flash electrical specifications

This section describes the electrical characteristics of the flash memory module.

The bytes not assigned to data flash via the FlexNVM partition code are used by the flash memory module to obtain an effective endurance increase for the EEPROM data. The built-in EEPROM record management system raises the number of program/erase cycles that can be attained prior to device wear-out by cycling the EEPROM data through a larger EEPROM NVM storage space.

While different partitions of the FlexNVM are available, the intention is that a single choice for the FlexNVM partition code and EEPROM data set size is used throughout the entire lifetime of a given application. The EEPROM endurance equation and graph shown below assume that only one configuration is ever used.

$$\text{Writes\_subsystem} = \frac{\text{EEPROM} - 2 \times \text{EEESPLIT} \times \text{EEESIZE}}{\text{EEESPLIT} \times \text{EEESIZE}} \times \text{Write\_efficiency} \times n_{\text{nvmcycd}}$$

where

- Writes_subsystem — minimum number of writes to each FlexRAM location for subsystem (each subsystem can have different endurance)
- EEPROM — allocated FlexNVM for each EEPROM subsystem based on DEPART; entered with the Program Partition command
- EEESPLIT — FlexRAM split factor for subsystem; entered with the Program Partition command
- EEESIZE — allocated FlexRAM based on DEPART; entered with the Program Partition command
- Write_efficiency —
  - 0.25 for 8-bit writes to FlexRAM
  - 0.50 for 16-bit or 32-bit writes to FlexRAM
- n_{nvmcycd} — data flash cycling endurance (the following graph assumes 10,000 cycles)

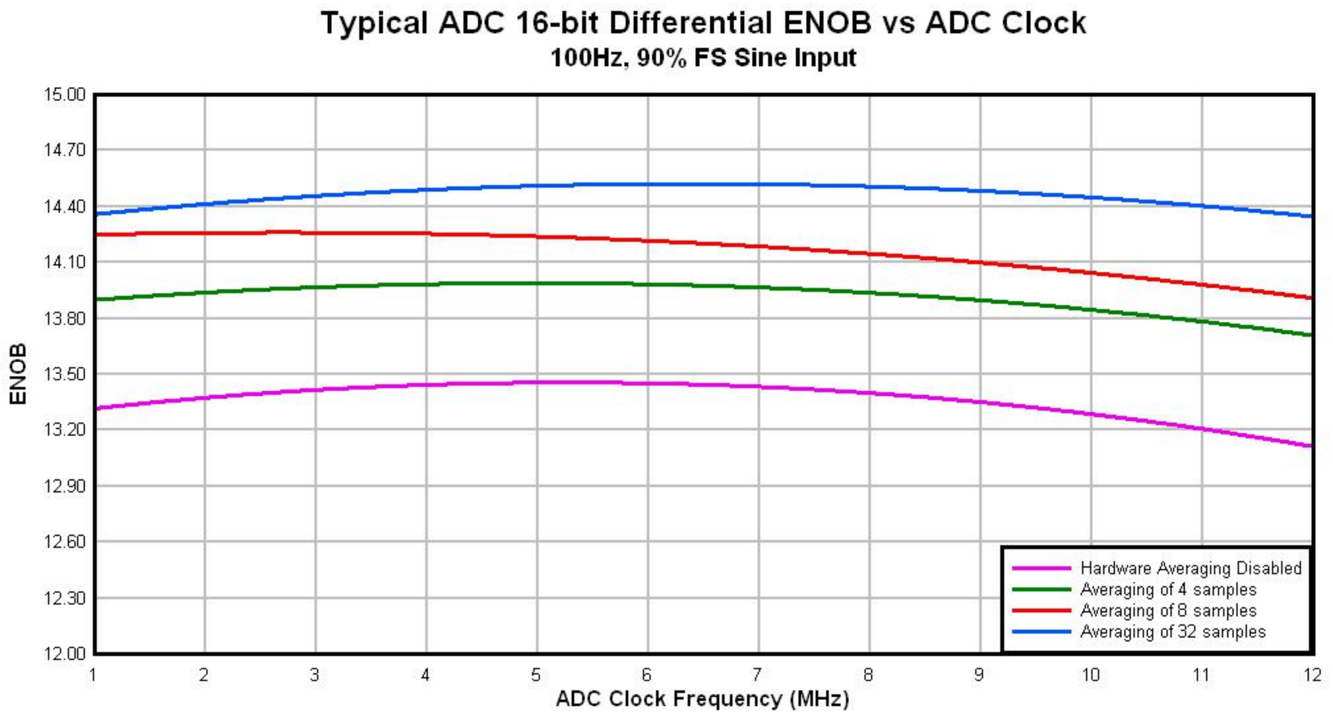


Figure 13. Typical ENOB vs. ADC_CLK for 16-bit differential mode

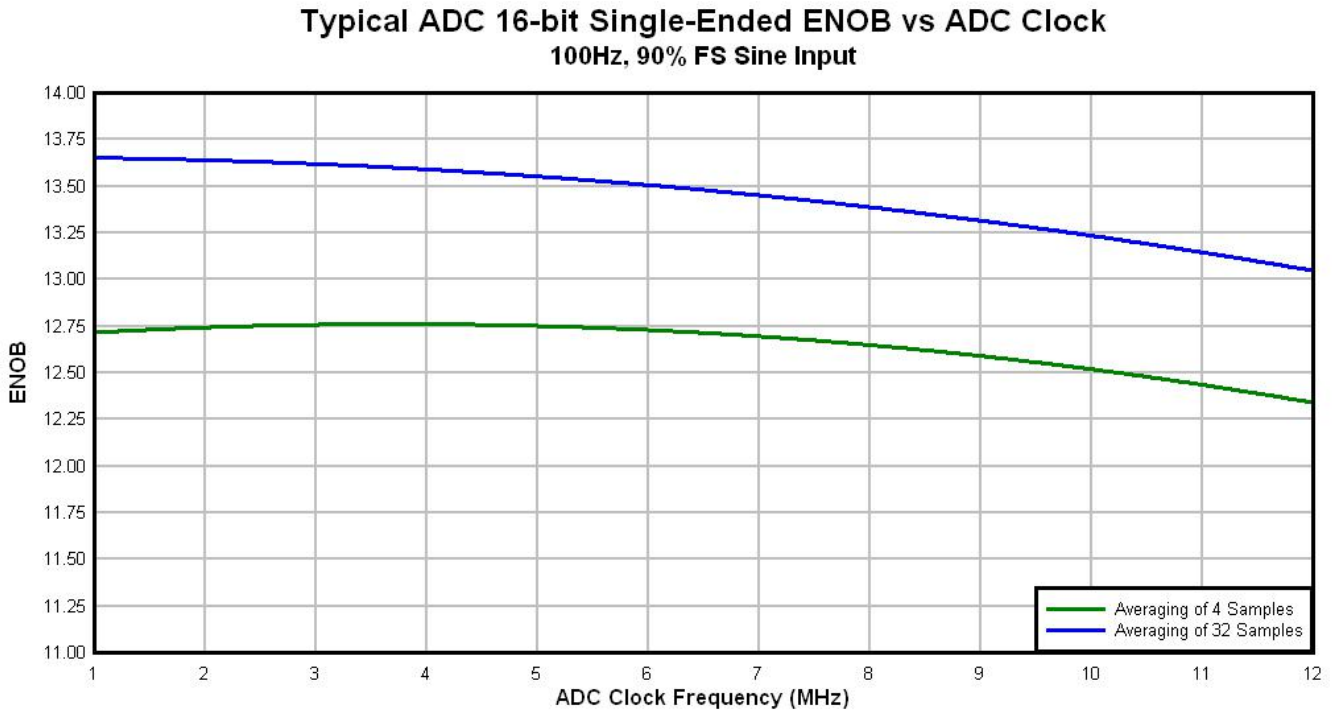


Figure 14. Typical ENOB vs. ADC_CLK for 16-bit single-ended mode

6.6.1.4 16-bit ADC with PGA characteristics with Chop enabled (ADC_PGA[PGACHPb] =0)

Table 27. 16-bit ADC with PGA characteristics

Symbol	Description	Conditions	Min.	Typ.[1]	Max.	Unit	Notes
I_{DDA_PGA}	Supply current	Low power (ADC_PGA[PGALPb]=0)	—	420	644	µA	[2]
I_{DC_PGA}	Input DC current		$\frac{2}{R_{PGAD}}\left(\frac{(V_{REFPGA}\times 0.583)-V_{CM}}{(\mathrm{Gain}+1)}\right)$			A	[3]
		Gain =1, V_{REFPGA}=1.2V, V_{CM}=0.5V	—	1.54	—	µA	
		Gain =64, V_{REFPGA}=1.2V, V_{CM}=0.1V	—	0.57	—	µA	
G	Gain[4]	• PGAG=0 • PGAG=1 • PGAG=2 • PGAG=3 • PGAG=4 • PGAG=5 • PGAG=6	0.95 1.9 3.8 7.6 15.2 30.0 58.8	1 2 4 8 16 31.6 63.3	1.05 2.1 4.2 8.4 16.6 33.2 67.8		$R_{AS} < 100\Omega$
BW	Input signal bandwidth	• 16-bit modes • < 16-bit modes	— —	— —	4 40	kHz kHz	
PSRR	Power supply rejection ratio	Gain=1	—	-84	—	dB	V_{DDA}= 3V ±100mV, f_{VDDA}= 50Hz, 60Hz
CMRR	Common mode rejection ratio	• Gain=1 • Gain=64	— —	-84 -85	— —	dB dB	V_{CM}= 500mVpp, f_{VCM}= 50Hz, 100Hz
V_{OFS}	Input offset voltage		—	0.2	—	mV	Output offset = V_{OFS}*(Gain+1)
T_{GSW}	Gain switching settling time		—	—	10	µs	[5]
dG/dT	Gain drift over full temperature range	• Gain=1 • Gain=64	— —	6 31	10 42	ppm/°C ppm/°C	
dG/dV_{DDA}	Gain drift over supply voltage	• Gain=1 • Gain=64	— —	0.07 0.14	0.21 0.31	%/V %/V	V_{DDA} from 1.71 to 3.6V
E_{IL}	Input leakage error	All modes	$I_{In} \times R_{AS}$			mV	I_{In} = leakage current (refer to the MCU's voltage and current operating ratings)

Table continues on the next page...

Table 28. Comparator and 6-bit DAC electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{DDHS}	Supply current, High-speed mode (EN=1, PMODE=1)	—	—	200	μA
I_{DDLS}	Supply current, low-speed mode (EN=1, PMODE=0)	—	—	20	μA
V_{AIN}	Analog input voltage	V_{SS} – 0.3	—	V_{DD}	V
V_{AIO}	Analog input offset voltage	—	—	20	mV
V_H	Analog comparator hysteresis[1]				
	• CR0[HYSTCTR] = 00	—	5	—	mV
	• CR0[HYSTCTR] = 01	—	10	—	mV
	• CR0[HYSTCTR] = 10	—	20	—	mV
	• CR0[HYSTCTR] = 11	—	30	—	mV
V_{CMPOh}	Output high	V_{DD} – 0.5	—	—	V
V_{CMPOl}	Output low	—	—	0.5	V
t_{DHS}	Propagation delay, high-speed mode (EN=1, PMODE=1)	20	50	200	ns
t_{DLS}	Propagation delay, low-speed mode (EN=1, PMODE=0)	80	250	600	ns
	Analog comparator initialization delay[2]	—	—	40	μs
I_{DAC6b}	6-bit DAC current adder (enabled)	—	7	—	μA
INL	6-bit DAC integral non-linearity	–0.5	—	0.5	LSB[3]
DNL	6-bit DAC differential non-linearity	–0.3	—	0.3	LSB

1. Typical hysteresis is measured with input voltage range limited to 0.6 to V_{DD}-0.6V.
2. Comparator initialization delay is defined as the time between software writes to change control inputs (Writes to DACEN, VRSEL, PSEL, MSEL, VOSEL) and the comparator output settling to a stable level.
3. 1 LSB = $V_{reference}/64$

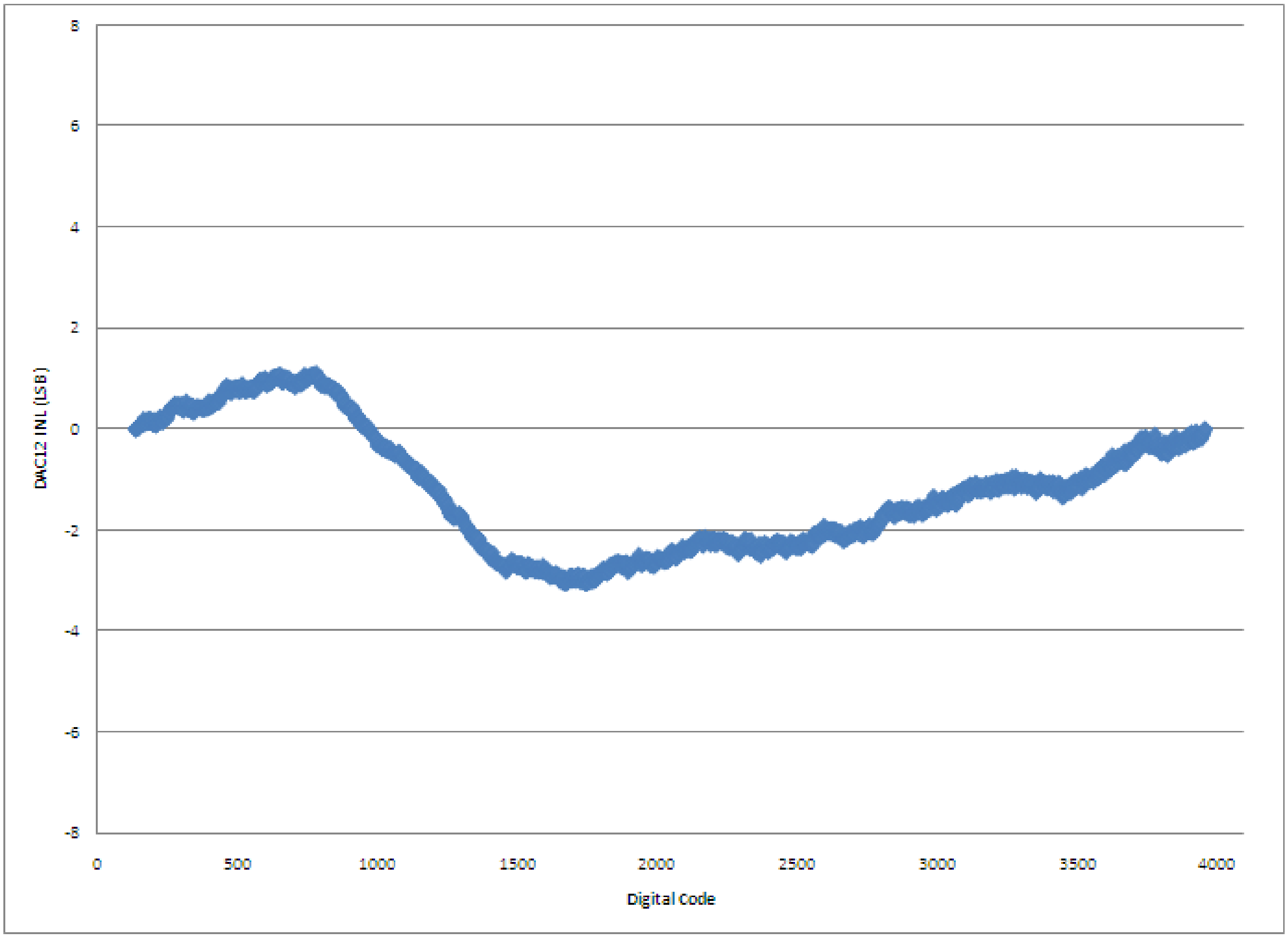


Figure 17. Typical INL error vs. digital code

Table 31. Op-amp electrical specifications (continued)

Symbol	Description	Min.	Typ.	Max.	Unit
I_{BIAS}	Typical input bias current across the following temp range (0–50°C)	—	±500	—	pA
I_{BIAS}	Typical input bias current across the following temp range (-40–105°C)	—	±4	—	nA
V_{CML}	Input common mode voltage low	0	—	—	V
V_{CMH}	Input common mode voltage high	—	—	VDD	V
R_{IN}	Input resistance	—	500	—	MΩ
C_{IN}	Input capacitance	—	17[1]	—	pF
$\lvert X_{IN} \rvert$	AC input impedance (f_{IN}=100kHz)	—	50	—	MΩ
CMRR	Input common mode rejection ratio	60	—	—	dB
PSRR	Power supply rejection ratio	60	—	—	dB
SR	Slew rate (ΔV_{IN}=500mV), low-power mode	0.1	—	—	V/µs
SR	Slew rate (ΔV_{IN}=500mV), high-speed mode	1.5	4	—	V/µs
GBW	Unity gain bandwidth, low-power mode	0.15	—	—	MHz
GBW	Unity gain bandwidth, high-speed mode	1	—	—	MHz
A_V	DC open-loop voltage gain	80	90	—	dB
CL(max)	Load capacitance driving capability	—	100	—	pF
R_{OUT}	Output resistance @ 100 kHz, high speed mode	—	1500	—	Ω
V_{OUT}	Output voltage range	0.12	—	VDD - 0.12	V
I_{OUT}	Output load current	—	±0.5	—	mA
GM	Gain margin	—	20	—	dB
PM	Phase margin	45	56	—	deg
T_{settle}	Settling time[2] (Buffer mode, low-power mode) (To<0.1%, V_{in}=1.65V)	—	5.7	—	µs
T_{settle}	Settling time[2] (Buffer mode, high-speed mode) (To<0.1%, V_{in}=1.65V)	—	3.0	—	µs
Vn	Voltage noise density (noise floor) 1kHz	—	350	—	nV/√Hz
Vn	Voltage noise density (noise floor) 10kHz	—	90	—	nV/√Hz

1. The input capacitance is dependant on the package type used.
2. Settling time is measured from the time the Op-amp is enabled until the output settles to within 0.1% of final value. This time includes Op-amp startup time, output slew, and settle time.

6.6.5 Transimpedance amplifier electrical specifications — full range

Table 32. TRIAMP full range operating requirements

Symbol	Description	Min.	Max.	Unit	Notes
V_{DDA}	Supply voltage	1.71	3.6	V	
V_{IN}	Input voltage range	-0.1	V_{DDA}-1.4	V	
C_L	Output load capacitance	—	100	pf	

Table 44. Master mode DSPI timing (full voltage range) (continued)

Num	Description	Min.	Max.	Unit	Notes
DS4	DSPI_SCK to DSPI_PCS*n* invalid delay	$(t_{BUS} \times 2) - 4$	—	ns	3
DS5	DSPI_SCK to DSPI_SOUT valid	—	10	ns	
DS6	DSPI_SCK to DSPI_SOUT invalid	-4.5	—	ns	
DS7	DSPI_SIN to DSPI_SCK input setup	20.5	—	ns	
DS8	DSPI_SCK to DSPI_SIN input hold	0	—	ns	

1. The DSPI module can operate across the entire operating voltage for the processor, but to run across the full voltage range the maximum frequency of operation is reduced.
2. The delay is programmable in SPIx_CTARn[PSSCK] and SPIx_CTARn[CSSCK].
3. The delay is programmable in SPIx_CTARn[PASC] and SPIx_CTARn[ASC].

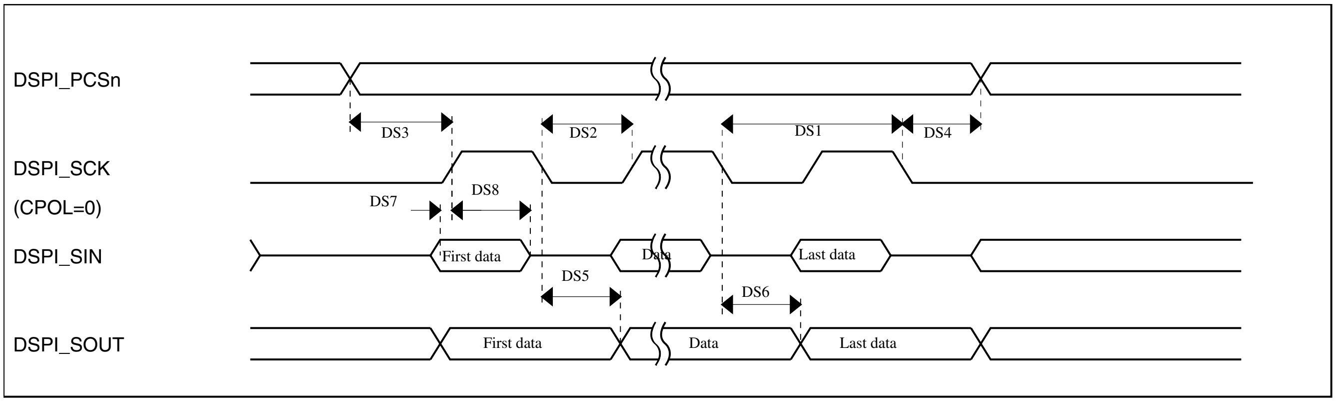


Figure 21. DSPI classic SPI timing — master mode

Table 45. Slave mode DSPI timing (full voltage range)

Num	Description	Min.	Max.	Unit
	Operating voltage	1.71	3.6	V
	Frequency of operation	—	6.25	MHz
DS9	DSPI_SCK input cycle time	$8 \times t_{BUS}$	—	ns
DS10	DSPI_SCK input high/low time	$(t_{SCK}/2) - 4$	$(t_{SCK/2}) + 4$	ns
DS11	DSPI_SCK to DSPI_SOUT valid	—	20	ns
DS12	DSPI_SCK to DSPI_SOUT invalid	0	—	ns
DS13	DSPI_SIN to DSPI_SCK input setup	2	—	ns
DS14	DSPI_SCK to DSPI_SIN input hold	7	—	ns
DS15	$\overline{\text{DSPI\_SS}}$ active to DSPI_SOUT driven	—	19	ns
DS16	$\overline{\text{DSPI\_SS}}$ inactive to DSPI_SOUT not driven	—	19	ns

Table 49. I2S/SAI slave mode timing in VLPR, VLPW, and VLPS modes (full voltage range) (continued)

Num.	Characteristic	Min.	Max.	Unit
S17	I2S_RXD setup before I2S_RX_BCLK	30	—	ns
S18	I2S_RXD hold after I2S_RX_BCLK	6.5	—	ns
S19	I2S_TX_FS input assertion to I2S_TXD output valid[1]	—	72	ns

1. Applies to first bit in each frame and only if the TCR4[FSE] bit is clear

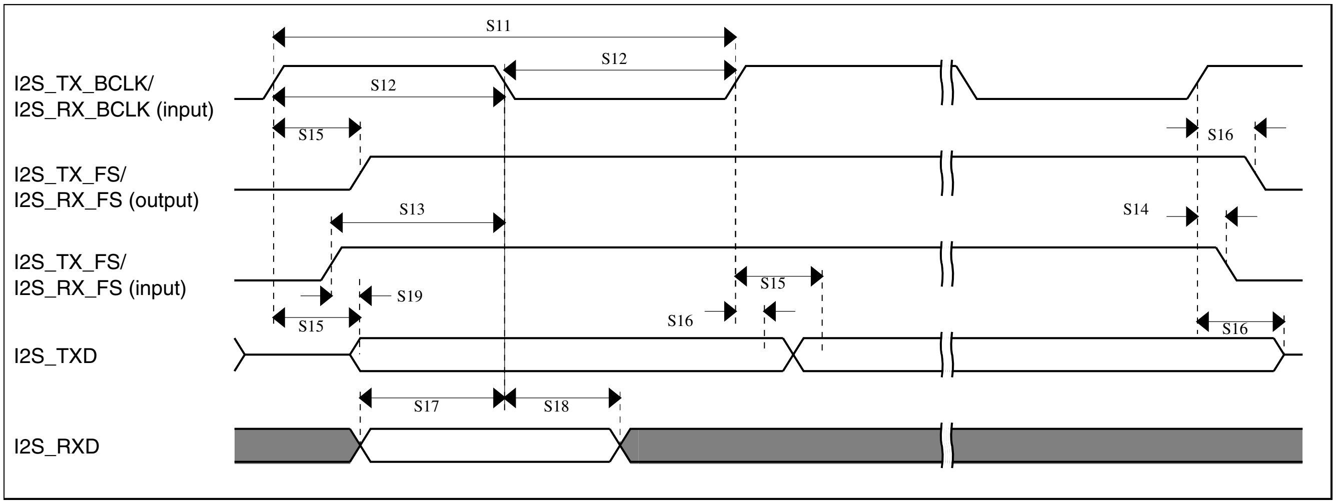


Figure 26. I2S/SAI timing — slave modes

6.9 Human-machine interfaces (HMI)

6.9.1 TSI electrical specifications

Table 50. TSI electrical specifications

Symbol	Description	Min.	Typ.	Max.	Unit	Notes
V_{DDTSI}	Operating voltage	1.71	—	3.6	V	
C_{ELE}	Target electrode capacitance range	1	20	500	pF	1
f_{REFmax}	Reference oscillator frequency	—	8	15	MHz	2, 3
f_{ELEmax}	Electrode oscillator frequency	—	1	1.8	MHz	2, 4
C_{REF}	Internal reference capacitor	—	1	—	pF	
V_{DELTA}	Oscillator delta voltage	—	500	—	mV	2, 5
I_{REF}	Reference oscillator current source base current • 2 μA setting (REFCHRG = 0) • 32 μA setting (REFCHRG = 15)	 — —	 2 36	 3 50	μA	2, 6

Table continues on the next page...

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
L1	19	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3	PGA1_DP/ ADC1_DP0/ ADC0_DP3								
L2	20	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3	PGA1_DM/ ADC1_DM0/ ADC0_DM3								
F5	21	VDDA	VDDA	VDDA								
G5	22	VREFH	VREFH	VREFH								
G6	23	VREFL	VREFL	VREFL								
F6	24	VSSA	VSSA	VSSA								
J3	25	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2	ADC1_SE16/ OP1_OUT/ CMP2_IN2/ ADC0_SE22/ OP0_DP2/ OP1_DP2								
H3	26	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1	ADC0_SE16/ OP0_OUT/ CMP1_IN2/ ADC0_SE21/ OP0_DP1/ OP1_DP1								
L3	27	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18	VREF_OUT/ CMP1_IN5/ CMP0_IN5/ ADC1_SE18								
K3	28	TRI0_OUT/ OP1_DM2	TRI0_OUT/ OP1_DM2	TRI0_OUT/ OP1_DM2								
H4	29	TRI0_DM	TRI0_DM	TRI0_DM								
J4	30	TRI0_DP	TRI0_DP	TRI0_DP								
H5	31	NC	NC	NC								
J5	32	NC	NC	NC								
H6	33	CMP2_IN5/ ADC1_SE22	CMP2_IN5/ ADC1_SE22	CMP2_IN5/ ADC1_SE22								
K5	34	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4	DAC0_OUT/ CMP1_IN3/ ADC0_SE23/ OP0_DP4/ OP1_DP4								
K4	35	CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5	CMP0_IN4/ CMP2_IN3/ ADC1_SE23/ OP0_DP5/ OP1_DP5								
L7	—	RTC_ WAKEUP_B	RTC_ WAKEUP_B	RTC_ WAKEUP_B								
L4	36	XTAL32	XTAL32	XTAL32								
L5	37	EXTAL32	EXTAL32	EXTAL32								

121 MAP BGA	100 LQFP	Pin Name	Default	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6	ALT7	EzPort
B5	—	NC	NC	NC								
B1	—	NC	NC	NC								
C2	—	NC	NC	NC								
C1	—	NC	NC	NC								
D2	—	NC	NC	NC								
D1	—	NC	NC	NC								
E1	—	NC	NC	NC								

8.2 K51 Pinouts

The below figure shows the pinout diagram for the devices supported by this document. Many signals may be multiplexed onto a single pin. To determine what signals can be used on which pin, see the previous section.

Table 52. Revision History (continued)

Rev. No.	Date	Substantial Changes
2	4/2012	• Replaced TBDs throughout. • Updated "Power consumption operating behaviors" table. • Updated "ADC electrical specifications" section. • Updated "VREF full-range operating behaviors" table. • Updated "I2S/SAI Switching Specifications" section. • Updated "TSI electrical specifications" table.
3	11/2012	• Updated orderable part numbers. • Updated the maximum input voltage (V_{ADIN}) specification in the "16-bit ADC operating conditions" section. • Updated the maximum I_{DDstby} specification in the "USB VREG electrical specifications" section.