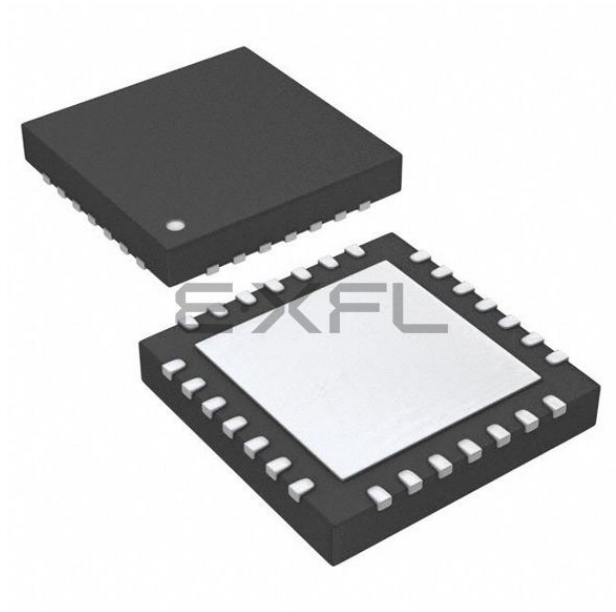

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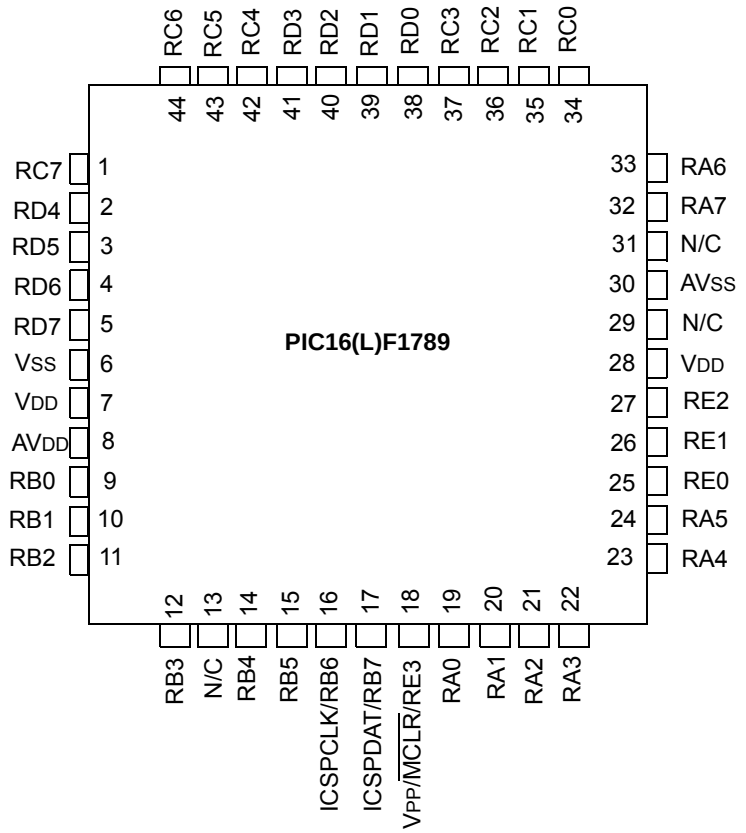
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1788-e-ml

Pin Diagram – 44-Pin QFN



Note: See Table 2 for the location of all peripheral functions.

TABLE 1-3: PIC16(L)F1789 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RC4/PSMC1E/SDI/SDA	RC4	TTL/ST	CMOS	General purpose I/O.
	PSMC1E	—	CMOS	PSMC1 output E.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C data input/output.
RC5/PSMC1F/SDO	RC5	TTL/ST	CMOS	General purpose I/O.
	PSMC1F	—	CMOS	PSMC1 output F.
	SDO	—	CMOS	SPI data output.
RC6/PSMC2A/TX/CK	RC6	TTL/ST	CMOS	General purpose I/O.
	PSMC2A	—	CMOS	PSMC2 output A.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
RC7/PSMC2B/RX/DT	RC7	TTL/ST	CMOS	General purpose I/O.
	PSMC2B	—	CMOS	PSMC2 output B.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.
RD0/OPA3IN+	RD0	TTL/ST	CMOS	General purpose I/O.
	OPA3IN+	AN	—	Operational Amplifier 3 non-inverting input.
RD1/AN21/C1IN4-/C2IN4-/ C3IN4-/C4IN4-/OPA3OUT	RD1	TTL/ST	CMOS	General purpose I/O.
	AN21	AN	—	ADC Channel 21 input.
	C1IN4-	AN	—	Comparator C4 negative input.
	C2IN4-	AN	—	Comparator C4 negative input.
	C3IN4-	AN	—	Comparator C4 negative input.
	C4IN4-	AN	—	Comparator C4 negative input.
	OPA3OUT	—	AN	Operational Amplifier 3 output.
RD2/OPA3IN-/DAC4OUT1	RD2	TTL/ST	CMOS	General purpose I/O.
	OPA3IN-	AN	—	Operational Amplifier 3 inverting input.
	DAC4OUT1	—	AN	Digital-to-Analog Converter output.
RD3/PSMC4A	RD3	TTL/ST	CMOS	General purpose I/O.
	PSMC4A	—	CMOS	PSMC4 output A.
RD4/PSMC3F	RD4	TTL/ST	CMOS	General purpose I/O.
	PSMC3F	—	CMOS	PSMC3 output F.
RD5/PSMC3E	RD5	TTL/ST	CMOS	General purpose I/O.
	PSMC3E	—	CMOS	PSMC3 output E.
RD6/C3OUT/PSMC3D	RD6	TTL/ST	CMOS	General purpose I/O.
	C3OUT	—	CMOS	Comparator C3 output.
	PSMC3D	—	CMOS	PSMC3 output D.
RD7/C4OUT/PSMC3C	RD7	TTL/ST	CMOS	General purpose I/O.
	C4OUT	—	CMOS	Comparator C4 output.
	PSMC3C	—	CMOS	PSMC3 output C.
RE0/AN5/CCP3/PSMC4B	RE0	TTL/ST	—	General purpose input.
	AN5	AN	—	ADC Channel 5 input.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	PSMC4B	—	CMOS	PSMC4 output B.

Legend: AN = Analog input or output; CMOS = CMOS compatible input or output; OD = Open-Drain
TTL = TTL compatible input; ST = Schmitt Trigger input with CMOS levels; I^2C = Schmitt Trigger input with I^2C levels
HV = High Voltage; XTAL = Crystal

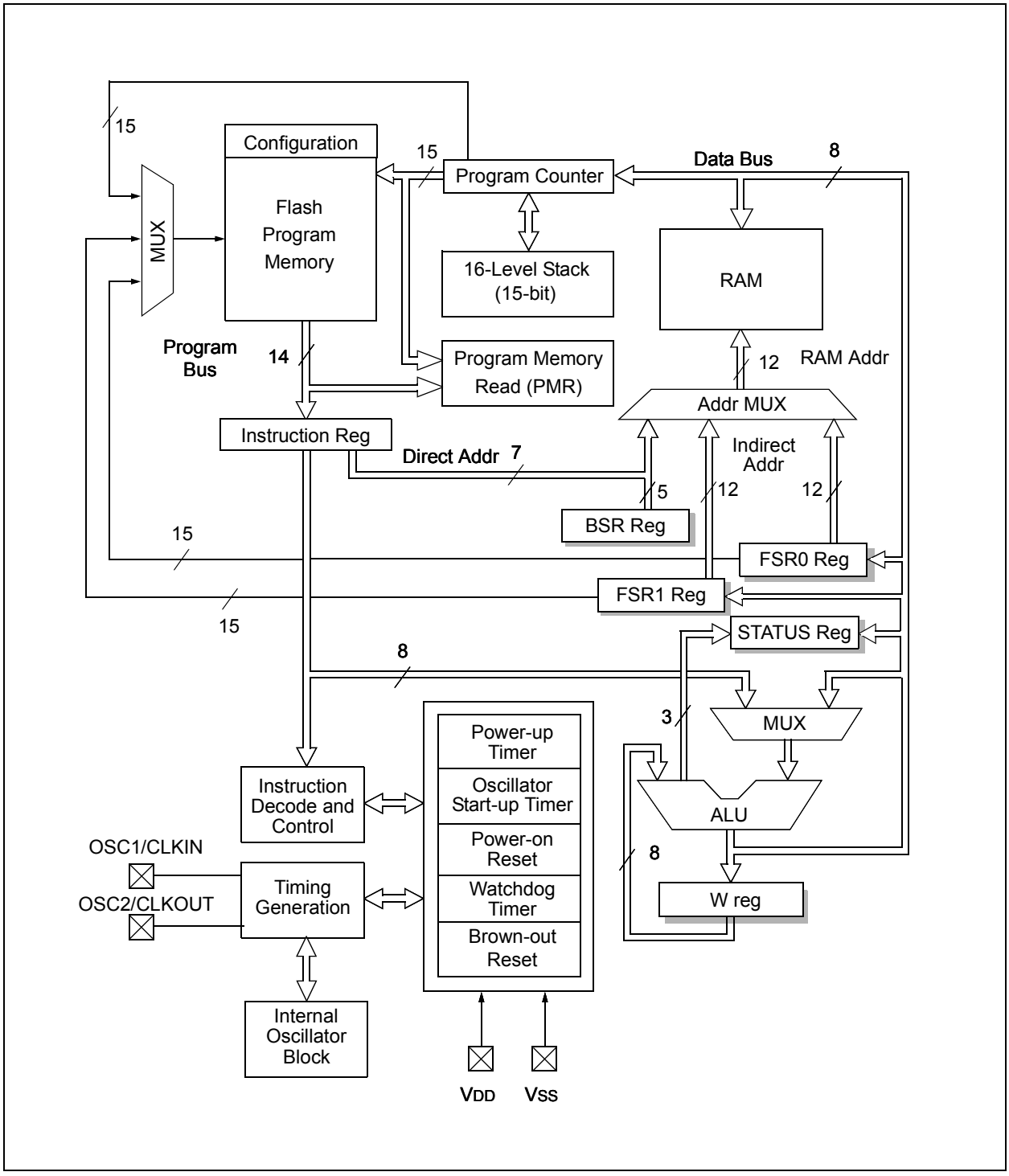
Note 1: Pin functions can be assigned to one of two locations via software. See **Register 13-1**.
2: All pins have interrupt-on-change functionality.

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM



EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    DW      DATA0   ;First constant
    DW      DATA1   ;Second constant
    DW      DATA2
    DW      DATA3
my_function
    ;… LOTS OF CODE…
    MOVLW   DATA_INDEX
    ADDLW   LOW constants
    MOVWF   FSR1L
    MOVLW   HIGH constants ;MSb is set
automatically
    MOVWF   FSR1H
    BTFSC   STATUS,C    ;carry from ADDLW?
    INCF    FSR1H,f     ;yes
    MOVIW   0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 4											
20Ch	WPUA	WPUA7	WPUA6	WPUA5	WPUA4	WPUA3	WPUA2	WPUA1	WPUA0	1111 1111	1111 1111
20Dh	WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	1111 1111	1111 1111
20Eh	WPUC	WPUC7	WPUC6	WPUC5	WPUC4	WPUC3	WPUC2	WPUC1	WPUC0	1111 1111	1111 1111
20Fh	WPUD(3)	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	1111 1111	1111 1111
210h	WPUE	—	—	—	—	WPUE3	WPUE2(3)	WPUE1(3)	WPUE0(3)	---- 1111	---- 1111
211h	SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
212h	SSP1ADD	ADD<7:0>								0000 0000	0000 0000
213h	SSP1MSK	MSK<7:0>								1111 1111	1111 1111
214h	SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	0000 0000	0000 0000
215h	SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				0000 0000	0000 0000
216h	SSP1CON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	0000 0000
217h	SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000 0000	0000 0000
218h — 21Fh	—	Unimplemented								—	—
Bank 5											
28Ch	ODCONA	Open-Drain Control for PORTA								0000 0000	0000 0000
28Dh	ODCONB	Open-Drain Control for PORTB								0000 0000	0000 0000
28Eh	ODCONC	Open-Drain Control for PORTC								0000 0000	0000 0000
28Fh	ODCOND(3)	Open-Drain Control for PORTD								0000 0000	0000 0000
290h	ODCONE(3)	—	—	—	—	—	ODE2	ODE1	ODE0	---- -000	---- -uuu
291h	CCPR1L	Capture/Compare/PWM Register 1 (LSB)								xxxx xxxx	uuuu uuuu
292h	CCPR1H	Capture/Compare/PWM Register 1 (MSB)								xxxx xxxx	uuuu uuuu
293h	CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				--00 0000	--00 0000
294h — 297h	—	Unimplemented								—	—
298h	CCPR2L	Capture/Compare/PWM Register 2 (LSB)								xxxx xxxx	uuuu uuuu
299h	CCPR2H	Capture/Compare/PWM Register 2 (MSB)								xxxx xxxx	uuuu uuuu
29Ah	CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				--00 0000	--00 0000
29Bh — 29Fh	—	Unimplemented								—	—
Bank 6											
30Ch	SLRCONA	Slew Rate Control for PORTA								0000 0000	0000 0000
30Dh	SLRCONB	Slew Rate Control for PORTB								0000 0000	0000 0000
30Eh	SLRCONC	Slew Rate Control for PORTC								0000 0000	0000 0000
30Fh	SLRCOND(3)	Slew Rate Control for PORTD								0000 0000	0000 0000
310h	SLRCONE(3)	—	—	—	—	—	SLRE2	SLRE1	SLRE0	---- -111	---- -111
311h	CCPR3L	Capture/Compare/PWM Register 3 (LSB)								xxxx xxxx	uuuu uuuu
312h	CCPR3H	Capture/Compare/PWM Register 3 (MSB)								xxxx xxxx	uuuu uuuu
313h	CCP3CON	—	—	DC3B<1:0>		CCP3M<3:0>				--00 0000	--00 0000
314h — 31Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Words. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.4 "Write Protection"** for more information.

4.3.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the $\overline{CPD}$ bit. When $\overline{CPD}$ = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 12.5 "User ID, Device ID and Configuration Word Access"**for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F178X Memory Programming Specification"* (DS41457).

6.4 Two-Speed Clock Start-up Mode

Two-Speed Start-up mode provides additional power savings by minimizing the latency between external oscillator start-up and code execution. In applications that make heavy use of the Sleep mode, Two-Speed Start-up will remove the external oscillator start-up time from the time spent awake and can reduce the overall power consumption of the device. This mode allows the application to wake-up from Sleep, perform a few instructions using the INTOSC internal oscillator block as the clock source and go back to Sleep without waiting for the external oscillator to become stable.

Two-Speed Start-up provides benefits when the oscillator module is configured for LP, XT or HS modes. The Oscillator Start-up Timer (OST) is enabled for these modes and must count 1024 oscillations before the oscillator can be used as the system clock source.

If the oscillator module is configured for any mode other than LP, XT or HS mode, then Two-Speed Start-up is disabled. This is because the external clock oscillator does not require any stabilization time after POR or an exit from Sleep.

If the OST count reaches 1024 before the device enters Sleep mode, the OSTS bit of the OSCSTAT register is set and program execution switches to the external oscillator. However, the system may never operate from the external oscillator if the time spent awake is very short.

Note:	Executing a SLEEP instruction will abort the oscillator start-up time and will cause the OSTS bit of the OSCSTAT register to remain clear.

6.4.1 TWO-SPEED START-UP MODE CONFIGURATION

Two-Speed Start-up mode is configured by the following settings:

- IESO (of the Configuration Words) = 1; Internal/External Switchover bit (Two-Speed Start-up mode enabled).
- SCS (of the OSCCON register) = 00.
- FOSC<2:0> bits in the Configuration Words configured for LP, XT or HS mode.

Two-Speed Start-up mode is entered after:

- Power-on Reset (POR) and, if enabled, after Power-up Timer (PWRT) has expired, or
- Wake-up from Sleep.

TABLE 6-1: OSCILLATOR SWITCHING DELAYS

Switch From	Switch To	Frequency	Oscillator Delay
Sleep	LFINTOSC(1) MFINTOSC(1) HFINTOSC(1)	31 kHz 31.25 kHz-500 kHz 31.25 kHz-16 MHz	Oscillator Warm-up Delay TWARM(2)
Sleep/POR	EC, RC(1)	DC – 32 MHz	2 cycles
LFINTOSC	EC, RC(1)	DC – 32 MHz	1 cycle of each
Sleep/POR	Timer1 Oscillator LP, XT, HS(1)	32 kHz-20 MHz	1024 Clock Cycles (OST)
Any clock source	MFINTOSC(1) HFINTOSC(1)	31.25 kHz-500 kHz 31.25 kHz-16 MHz	2 μs (approx.)
Any clock source	LFINTOSC(1)	31 kHz	1 cycle of each
Any clock source	Timer1 Oscillator	32 kHz	1024 Clock Cycles (OST)
PLL inactive	PLL active	16-32 MHz	2 ms (approx.)

Note 1: PLL inactive.

2: See **Section 31.0 “Electrical Specifications”**.

REGISTER 6-2: OSCSTAT: OSCILLATOR STATUS REGISTER

R-1/q	R-0/q	R-q/q	R-0/q	R-0/q	R-q/q	R-0/0	R-0/q
T1OSCR	PLLR	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	q = Conditional

bit 7 **T1OSCR:** Timer1 Oscillator Ready bit
If T1OSCEN = 1:
1 = Timer1 oscillator is ready
0 = Timer1 oscillator is not ready
If T1OSCEN = 0:
1 = Timer1 clock source is always ready

bit 6 **PLLR** 4x PLL Ready bit
1 = 4x PLL is ready
0 = 4x PLL is not ready

bit 5 **OSTS:** Oscillator Start-up Timer Status bit
1 = Running from the clock defined by the FOSC<2:0> bits of the Configuration Words
0 = Running from an internal oscillator (FOSC<2:0> = 100)

bit 4 **HFIOFR:** High-Frequency Internal Oscillator Ready bit
1 = HFINTOSC is ready
0 = HFINTOSC is not ready

bit 3 **HFIOFL:** High-Frequency Internal Oscillator Locked bit
1 = HFINTOSC is at least 2% accurate
0 = HFINTOSC is not 2% accurate

bit 2 **MFIOFR:** Medium-Frequency Internal Oscillator Ready bit
1 = MFINTOSC is ready
0 = MFINTOSC is not ready

bit 1 **LFIOFR:** Low-Frequency Internal Oscillator Ready bit
1 = LFINTOSC is ready
0 = LFINTOSC is not ready

bit 0 **HFIOFS:** High-Frequency Internal Oscillator Stable bit
1 = HFINTOSC is at least 0.5% accurate
0 = HFINTOSC is not 0.5% accurate

13.10 Register Definitions: PORTD

REGISTER 13-26: PORTD: PORTD REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **RD<7:0>**: PORTD General Purpose I/O Pin bits(1)
1 = Port pin is ≥ VIH
0 = Port pin is ≤ VIL

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

REGISTER 13-27: TRISD: PORTD TRI-STATE REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **TRISD<7:0>:** PORTD Tri-State Control bits
1 = PORTD pin configured as an input (tri-stated)
0 = PORTD pin configured as an output

REGISTER 13-28: LATD: PORTD DATA LATCH REGISTER

R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u	R/W-x/u
LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **LATD<7:0>**: PORTD Output Latch Value bits(1)

Note 1: Writes to PORTD are actually written to corresponding LATD register. Reads from PORTD register is return of actual I/O pin values.

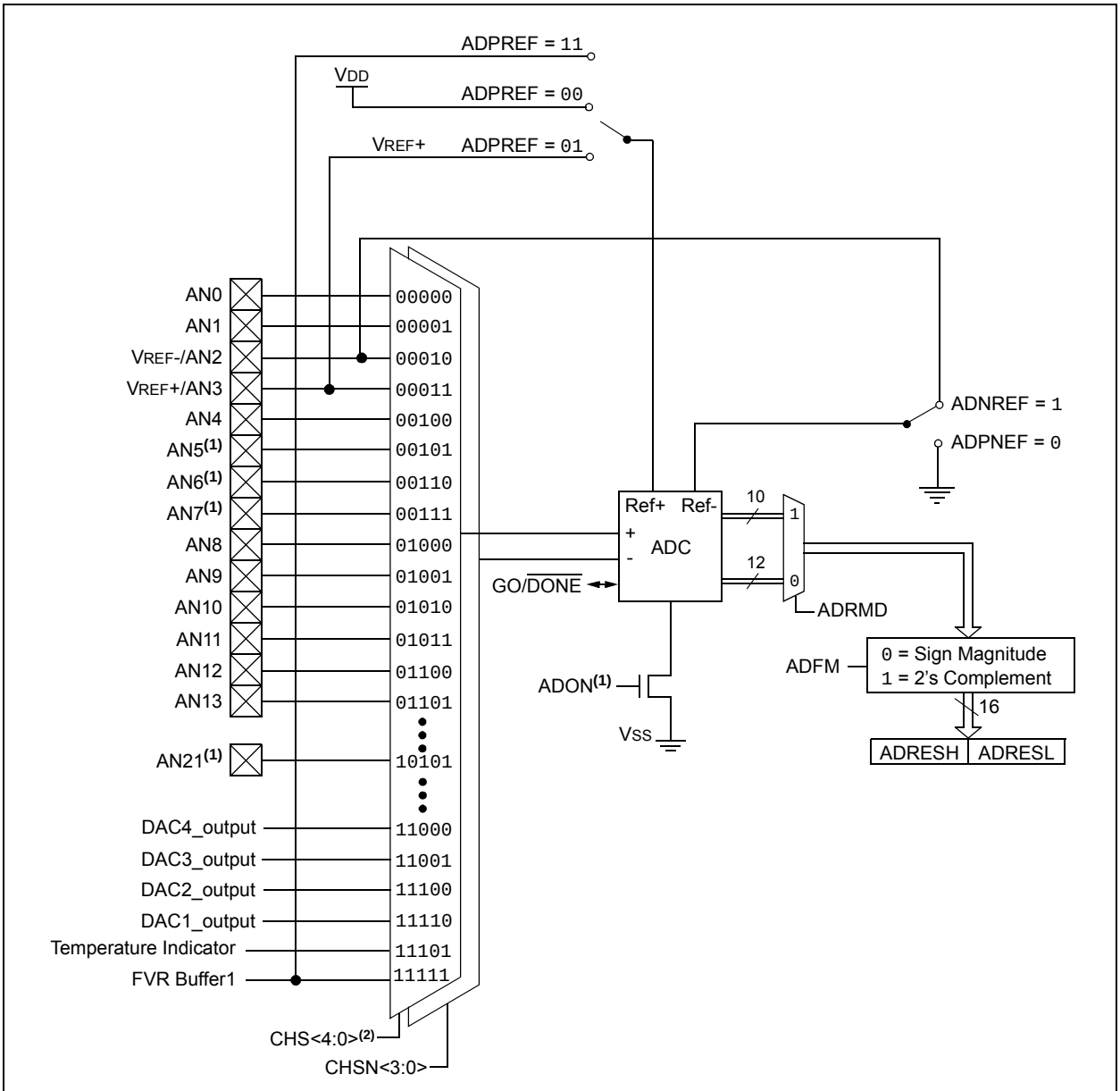
17.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of a single-ended and differential analog input signals to a 12-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 12-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 17-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

FIGURE 17-1: ADC BLOCK DIAGRAM



Note 1: When ADON = 0, all multiplexer inputs are disconnected. PIC16(L)F1789 only.

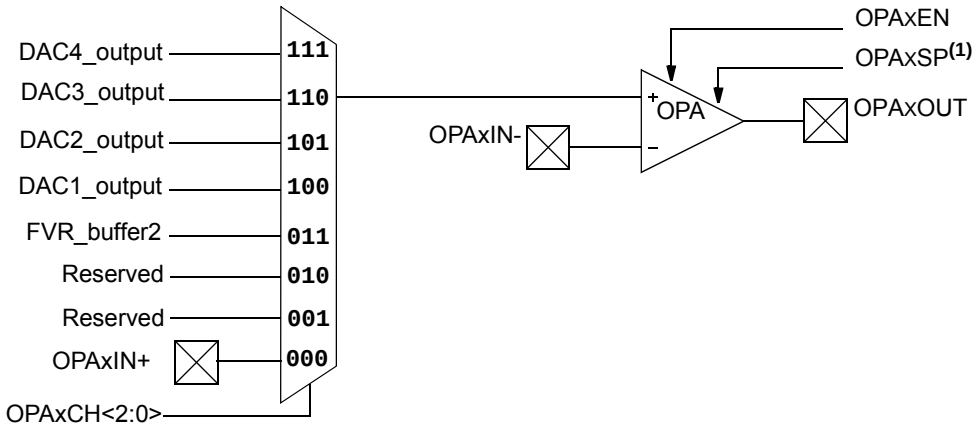
2: See ADCON0 register (Register 17-1) and ADCON2 register (Register 17-3) for detailed analog channel selection per device.

18.0 OPERATIONAL AMPLIFIER (OPA) MODULES

The Operational Amplifier (OPA) is a standard three-terminal device requiring external feedback to operate. The OPA module has the following features:

- External connections to I/O ports
- Low leakage inputs
- Factory Calibrated Input Offset Voltage

FIGURE 18-1: OPAx MODULE BLOCK DIAGRAM



Note 1: The OPAxSP bit must be set to '1'. Low-Power mode is not supported.

21.0 COMPARATOR MODULE

Comparators are used to interface analog circuits to a digital circuit by comparing two analog voltages and providing a digital indication of their relative magnitudes. Comparators are very useful mixed signal building blocks because they provide analog functionality independent of program execution. The analog comparator module includes the following features:

- Independent comparator control
- Programmable input selection
- Comparator output is available internally/externally
- Programmable output polarity
- Interrupt-on-change
- Wake-up from Sleep
- Programmable Speed/Power optimization
- PWM shutdown
- Programmable and fixed voltage reference

21.1 Comparator Overview

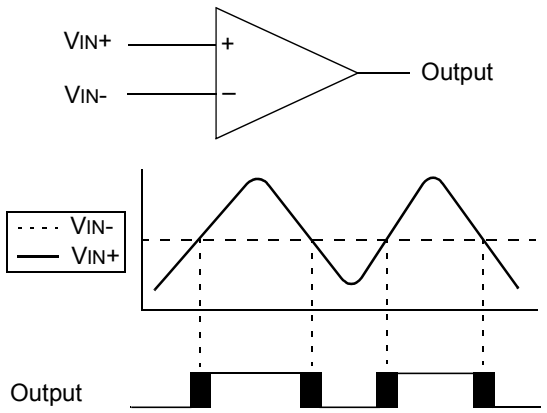
A single comparator is shown in Figure 21-1 along with the relationship between the analog input levels and the digital output. When the analog voltage at VIN+ is less than the analog voltage at VIN-, the output of the comparator is a digital low level. When the analog voltage at VIN+ is greater than the analog voltage at VIN-, the output of the comparator is a digital high level.

The comparators available for this device are located in Table 21-1.

TABLE 21-1: COMPARATOR AVAILABILITY PER DEVICE

Device	C1	C2	C3	C4
PIC16(L)F1788/9	●	●	●	●

FIGURE 21-1: SINGLE COMPARATOR



Note: The black areas of the output of the comparator represents the uncertainty due to input offsets and response time.

25.3 PWM Overview

Pulse-Width Modulation (PWM) is a scheme that provides power to a load by switching quickly between fully on and fully off states. The PWM signal resembles a square wave where the high portion of the signal is considered the on state and the low portion of the signal is considered the off state. The high portion, also known as the pulse width, can vary in time and is defined in steps. A larger number of steps applied, which lengthens the pulse width, also supplies more power to the load. Lowering the number of steps applied, which shortens the pulse width, supplies less power. The PWM period is defined as the duration of one complete cycle or the total amount of on and off time combined.

PWM resolution defines the maximum number of steps that can be present in a single PWM period. A higher resolution allows for more precise control of the pulse width time and in turn the power that is applied to the load.

The term duty cycle describes the proportion of the on time to the off time and is expressed in percentages, where 0% is fully off and 100% is fully on. A lower duty cycle corresponds to less power applied and a higher duty cycle corresponds to more power applied.

Figure 25-3 shows a typical waveform of the PWM signal.

25.3.1 STANDARD PWM OPERATION

The standard PWM function described in this section is available and identical for all CCP modules.

The standard PWM mode generates a Pulse-Width Modulation (PWM) signal on the CCPx pin with up to ten bits of resolution. The period, duty cycle, and resolution are controlled by the following registers:

- PR2 registers
- T2CON registers
- CCPRxL registers
- CCPxCON registers

Figure 25-4 shows a simplified block diagram of PWM operation.

Note 1:	The corresponding TRIS bit must be cleared to enable the PWM output on the CCPx pin.
2:	Clearing the CCPxCON register will relinquish control of the CCPx pin.

FIGURE 25-3: CCP PWM OUTPUT SIGNAL

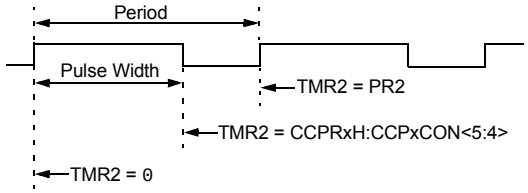
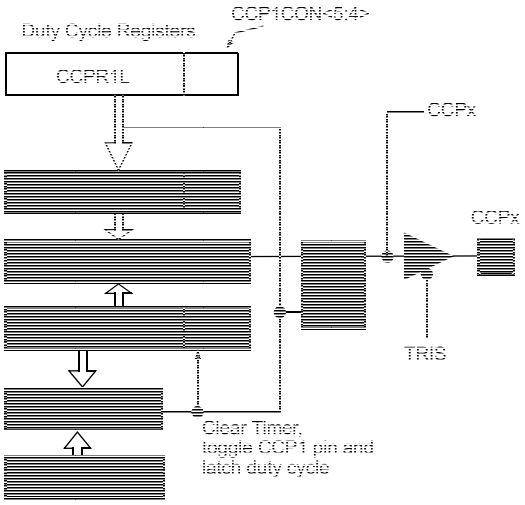


FIGURE 25-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The 8-bit timer TMR2 register is concatenated with the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base.

2: In PWM mode, CCPR1H is a read-only register.

TABLE 25-3: SUMMARY OF REGISTERS ASSOCIATED WITH STANDARD PWM

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	132
APFCON2	—	—	—	—	—	SSSEL<1:0>		CCP3SEL	231
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				231
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				231
CCP33CON	—	—	DC3B<1:0>		CCP3M<3:0>				231
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	97
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	99
PIE3	—	—	—	CCP3IE	—	—	—	—	100
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	103
PIR3	—	—	—	CCP3IF	—	—	—	—	104
PR2	Timer2 Period Register								220*
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		222
TMR2	Timer2 Module Register								220
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	136

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the PWM.

* Page provides register information.

26.3.8 PULSE-SKIPPING PWM WITH COMPLEMENTARY OUTPUTS

The pulse-skipping PWM is used to generate a series of fixed-length pulses that may or not be triggered at each period event. If any of the sources enabled to generate a rising edge event are high when a period event occurs, a pulse will be generated. If the rising edge sources are low at the period event, no pulse will be generated.

The rising edge occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

26.3.8.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM is output on only PSMCxA.
- Complementary PWM is output on only PSMCxB.

26.3.8.2 Waveform Generation

Rising Edge Event

If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:

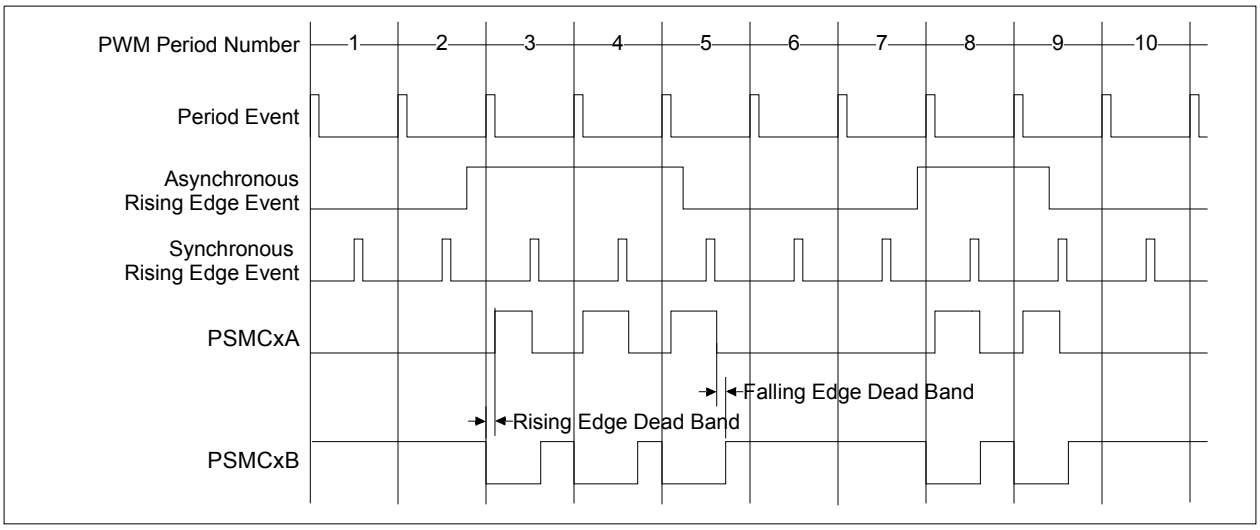
- Complementary output is set inactive
- Dead-band rising is activated (if enabled)
- Primary output is set active

Falling Edge Event

- Primary output is set inactive
- Dead-band falling is activated (if enabled)
- Complementary output is set active

Note:	To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 26-11: PULSE-SKIPPING WITH COMPLEMENTARY OUTPUT PWM WAVEFORM



28.4 EUSART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is an 8-bit or 16-bit timer that is dedicated to the support of both the asynchronous and synchronous EUSART operation. By default, the BRG operates in 8-bit mode. Setting the BRG16 bit of the BAUDCON register selects 16-bit mode.

The SPBRGH, SPBRGL register pair determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by both the BRGH bit of the TXSTA register and the BRG16 bit of the BAUDCON register. In Synchronous mode, the BRGH bit is ignored.

Table 28-3 contains the formulas for determining the baud rate. Example 28-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 28-3. It may be advantageous to use the high baud rate (BRGH = 1), or the 16-bit BRG (BRG16 = 1) to reduce the baud rate error. The 16-bit BRG mode is used to achieve slow baud rates for fast oscillator frequencies.

Writing a new value to the SPBRGH, SPBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RCIDL bit to make sure that the receive operation is idle before changing the system clock.

EXAMPLE 28-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

$$Desired\ Baud\ Rate = \frac{FOSC}{64([SPBRGH:SPBRGL] + 1)}$$

Solving for SPBRGH:SPBRGL:

$$X = \frac{\frac{FOSC}{Desired\ Baud\ Rate}}{64} - 1$$

$$= \frac{\frac{16000000}{9600}}{64} - 1$$

$$= [25.042] = 25$$

$$Calculated\ Baud\ Rate = \frac{16000000}{64(25 + 1)}$$

$$= 9615$$

$$Error = \frac{Calc.\ Baud\ Rate - Desired\ Baud\ Rate}{Desired\ Baud\ Rate}$$

$$= \frac{(9615 - 9600)}{9600} = 0.16\%$$

31.3 DC Characteristics

TABLE 31-1: SUPPLY VOLTAGE

PIC16LF1788/9			Standard Operating Conditions (unless otherwise stated)				
PIC16F1788/9							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D001	VDD	**Supply Voltage (VDDMIN, VDDMAX)**					
			1.8 2.5	— —	3.6 3.6	V V	FOSC ≤ 16 MHz: FOSC ≤ 32 MHz (**Note 2**)
D001			2.3 2.5	— —	5.5 5.5	V V	FOSC ≤ 16 MHz: FOSC ≤ 32 MHz (**Note 2**)
D002*	VDR	**RAM Data Retention Voltage(1)**					
			1.5	—	—	V	Device in Sleep mode
D002*			1.7	—	—	V	Device in Sleep mode
	VPOR*	**Power-on Reset Release Voltage**	—	1.6	—	V	
	VPORR*	**Power-on Reset Rearm Voltage**					
			—	0.8	—	V	Device in Sleep mode
			—	1.5	—	V	Device in Sleep mode
D003	VFVR	**Fixed Voltage Reference Voltage(3)**	-4	—	4	%	1.024V, VDD ≥ 2.5V
			-4	—	4	%	2.048V, VDD ≥ 2.5V
			-5	—	5	%	4.096V, VDD ≥ 4.75V
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 5.1 "Power-On Reset (POR)"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: PLL required for 32 MHz operation.

3: Industrial temperature range only.

TABLE 31-3: POWER-DOWN CURRENTS (I_{PD})(1,2,4) (CONTINUED)

PIC16LF1788/9		Operating Conditions: (unless otherwise stated) Low-Power Sleep Mode						
PIC16F1788/9		Low-Power Sleep Mode, VREGPM = 1						
Param No.	Device Characteristics	Min.	Typ†	Max. +85°C	Max. +125°C	Units	Conditions	
							V_{DD}	Note
	Power-down Base Current (I_{PD})(2)							
D029		—	0.05	2	9	µA	1.8	ADC Current **(Note 3)**, no conversion in progress
		—	0.08	3	10	µA	3.0	
D029		—	0.3	4	12	µA	2.3	ADC Current **(Note 3)**, no conversion in progress
		—	0.4	5	13	µA	3.0	
		—	0.5	7	16	µA	5.0	
D030		—	250	—	—	µA	1.8	ADC Current **(Note 3)**, conversion in progress
		—	280	—	—	µA	3.0	
D030		—	230	—	—	µA	2.3	ADC Current **(Note 3, Note 4, Note 5)**, conversion in progress
		—	250	—	—	µA	3.0	
		—	350	—	—	µA	5.0	
D031		—	250	650	—	µA	3.0	Op Amp (High power)
D031			250	650	—	µA	3.0	Op Amp (High power) **(Note 5)**
		—	350	850	—	µA	5.0	
D032		—	250	650	—	µA	1.8	Comparator, Normal-Power mode
		—	300	700	—	µA	3.0	
D032		—	280	650	—	µA	2.3	Comparator, Normal-Power mode **(Note 5)**
		—	300	700	—	µA	3.0	
		—	310	700	—	µA	5.0	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The peripheral current is the sum of the base I_{PD} and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base I_{DD} or I_{PD} current from this limit. Max values should be used when calculating total current consumption.

2: The power-down current in Sleep mode does not depend on the oscillator type. Power-down current is measured with the part in Sleep mode, with all I/O pins in high-impedance state and tied to V_{SS}.

3: ADC oscillator source is FRC.

4: 0.1 µF capacitor on V_{CAP}.

5: VREGPM = 0.

FIGURE 31-10: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

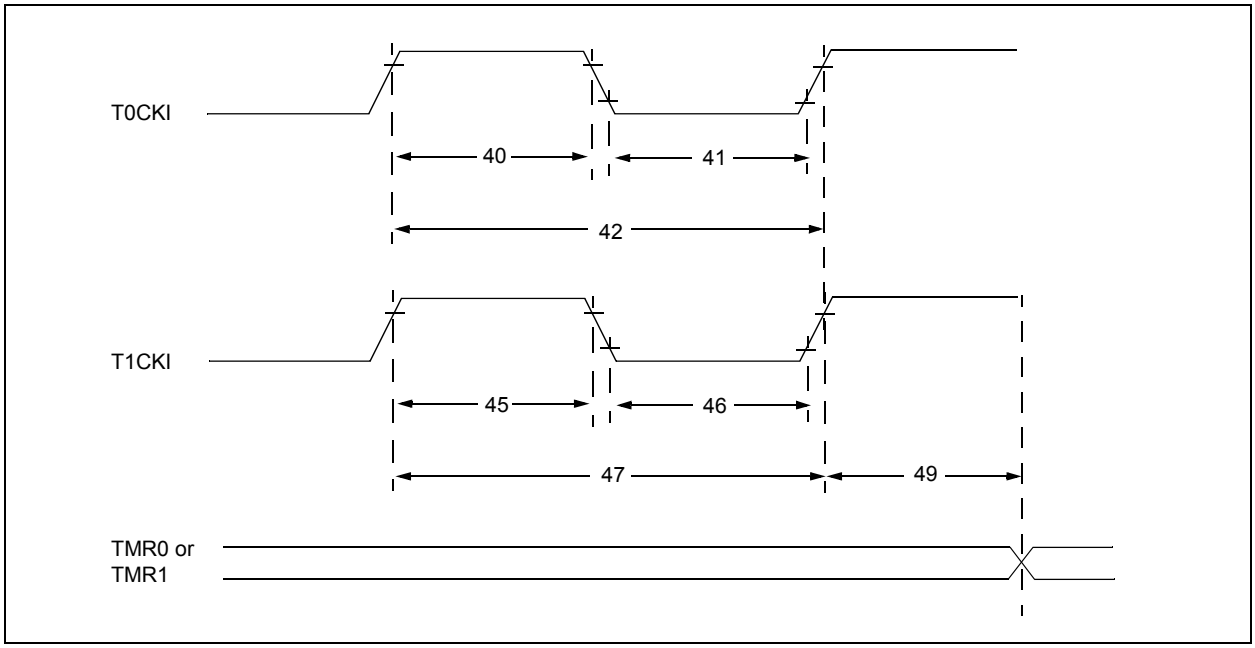


TABLE 31-11: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)									
Param No.	**Sym.**	**Characteristic**		**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
40*	TT0H	T0CKI High Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	TT0L	T0CKI Low Pulse Width	No Prescaler	0.5 TCY + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	TT0P	T0CKI Period		Greater of: 20 or TCY + 40 / N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	TT1H	T1CKI High Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	TT1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 TCY + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	TT1P	T1CKI Input Period	Synchronous	Greater of: 30 or TCY + 40 / N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
48	FT1	Timer1 Oscillator Input Frequency Range (oscillator enabled by setting bit T1OSCEN)		32.4	32.768	33.1	kHz	
49*	TCKEZTMR1	Delay from External Clock Edge to Timer Increment		2 TOSC	—	7 TOSC	—	Timers in Sync mode

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

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