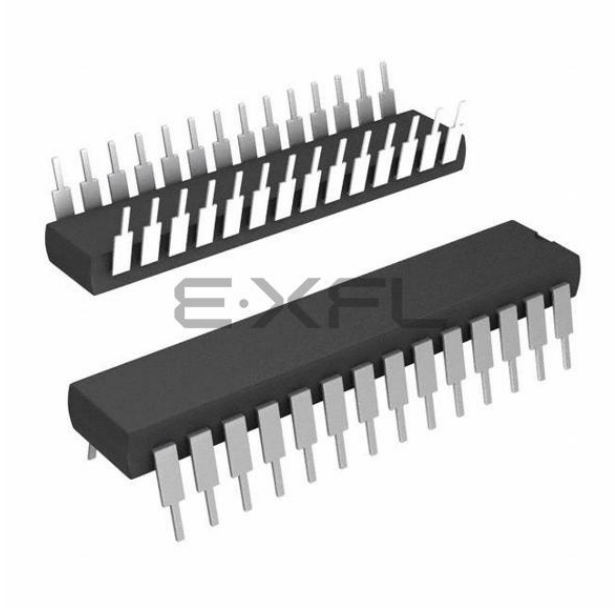

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	28-DIP (0.300", 7.62mm)
Supplier Device Package	28-SPDIP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1788-e-sp

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TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29 (Continued)											
ED1h	PSMC3CON	PSMC3EN	PSMC3LD	P3DBFE	P3DBRE	P3MODE<3:0>				0000 0000	0000 0000
ED2h	PSMC3MDL	P3MDLEN	P3MDLPOL	P3MDLBIT	—	P3MSRC<3:0>				000- 0000	000- 0000
ED3h	PSMC3SYNC	P3POFST	P3PRPOL	P3DCPOL	—	—	P3SYNC<2:0>			000- -000	000- -000
ED4h	PSMC3CLK	—	—	P3CPRE<1:0>		—	—	P3CSRC<1:0>		--00 --00	--00 --00
ED5h	PSMC3OEN	—	—	—	—	—	—	P3OEB	P3OEA	---- --00	---- --00
ED6h	PSMC3POL	—	P3INPOL	—	—	—	—	P3POLB	P3POLA	-0-- --00	-0-- --00
ED7h	PSMC3BLNK	—	—	P3FEBM<1:0>		—	—	P3REBM<1:0>		--00 --00	--00 --00
ED8h	PSMC3REBS	P3REBSIN	—	—	P3REBSC4	P3REBSC3	P3REBSC2	P3REBSC1	—	0--0 000-	0--0 000-
ED9h	PSMC3FEBS	P3FEBSIN	—	—	P3FEBSC4	P3FEBSC3	P3FEBSC2	P3FEBSC1	—	0--0 000-	0--0 000-
EDAh	PSMC3PHS	P3PHSIN	—	—	P3PHSC4	P3PHSC3	P3PHSC2	P3PHSC1	P3PHST	0--0 0000	0--0 0000
EDBh	PSMC3DCS	P3DCSIN	—	—	P3DCSC4	P3DCSC3	P3DCSC2	P3DCSC1	P3DCST	0--0 0000	0--0 0000
EDCh	PSMC3PRS	P3PRSIN	—	—	P3PRSC4	P3PRSC3	P3PRSC2	P3PRSC1	P3PRST	0--0 0000	0--0 0000
EDDh	PSMC3ASDC	P3ASE	P3ASDEN	P3ARSEN	—	—	—	—	P3ASDOV	000- ---0	000- ---0
EDEh	PSMC3ASDL	—	—	—	—	—	—	P3ASDLB	P3ASDLA	---- --00	---- --00
EDFh	PSMC3ASDS	P3ASDSIN	—	—	P3ASDSC4	P3ASDSC3	P3ASDSC2	P3ASDSC1	—	0--0 000-	0--0 000-
EE0h	PSMC3INT	P3TOVIE	P3TPHIE	P3TDCIE	P3TPRIE	P3TOVIF	P3TPHIF	P3TDCIF	P3TPRIF	0000 0000	0000 0000
EE1h	PSMC3PHL	Phase Low Count								0000 0000	0000 0000
EE2h	PSMC3PHH	Phase High Count								0000 0000	0000 0000
EE3h	PSMC3DCL	Duty Cycle Low Count								0000 0000	0000 0000
EE4h	PSMC3DCH	Duty Cycle High Count								0000 0000	0000 0000
EE5h	PSMC3PRL	Period Low Count								0000 0000	0000 0000
EE6h	PSMC3PRH	Period High Count								0000 0000	0000 0000
EE7h	PSMC3TMRL	Time base Low Counter								0000 0001	0000 0001
EE8h	PSMC3TMRH	Time base High Counter								0000 0000	0000 0000
EE9h	PSMC3DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
EEAh	PSMC3DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
EEBh	PSMC3BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
EECh	PSMC3BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
EEDh	PSMC3FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
EEEh	PSMC3STR0	—	—	—	—	—	—	P3STRB	P3STRA	---- --01	---- --01
EEFh	PSMC3STR1	P3SSYNC	—	—	—	—	—	P3LSMEN	P3HSMEN	0--- --00	0--- --00

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

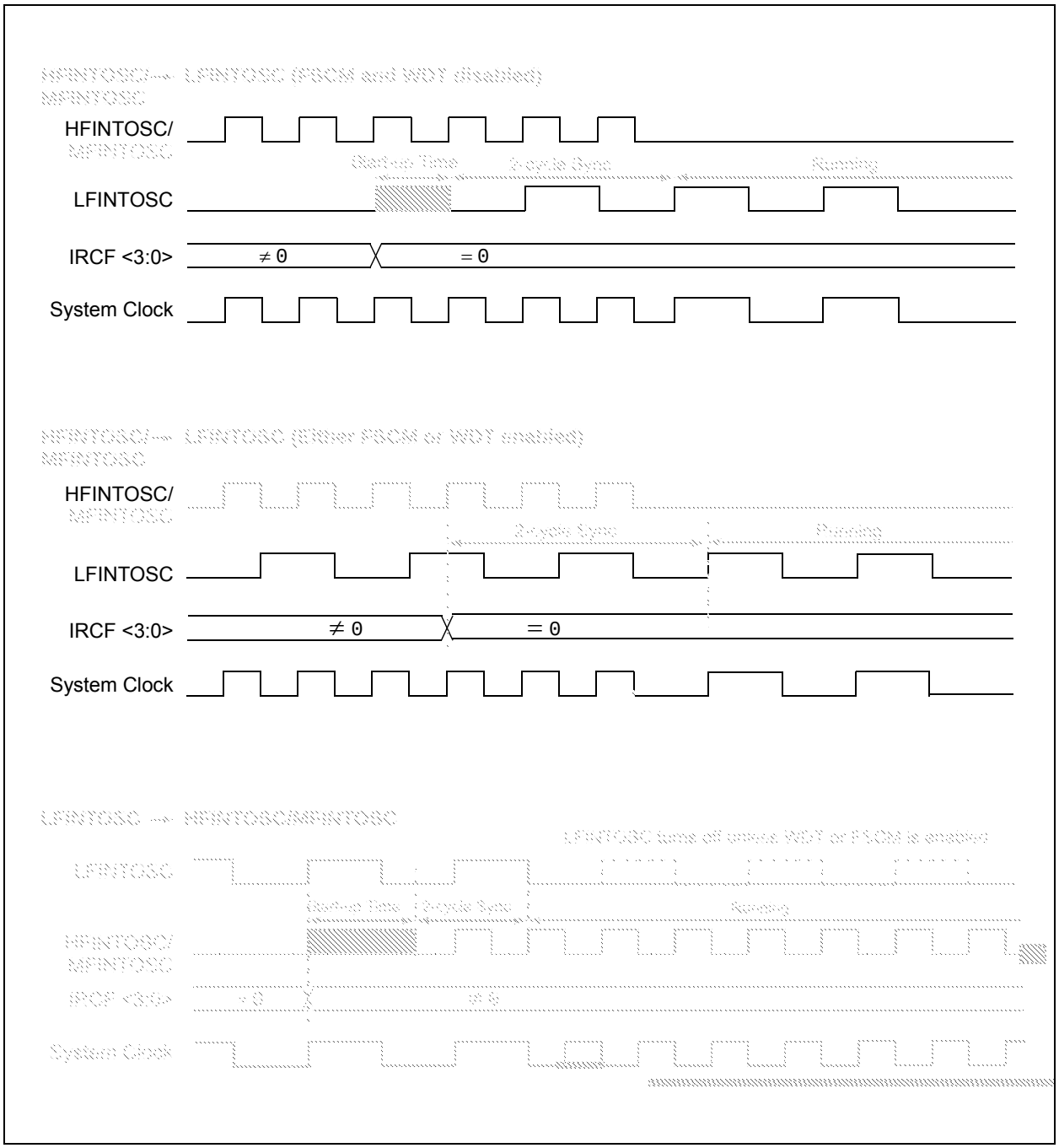
TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 30											
F0Ch — F10h	—	Unimplemented								—	—
F11h	PSMC4CON	PSMC4EN	PSMC4LD	P4DBFE	P4DBRE	P4MODE<3:0>				0000 0000	0000 0000
F12h	PSMC4MDL	P4MDLEN	P4MDLPOL	P4MDLBIT	—	P4MSRC<3:0>				000- 0000	000- 0000
F13h	PSMC4SYNC	P4POFST	P4PRPOL	P4DCPOL	—	—	P4SYNC<2:0>			000- -000	000- -000
F14h	PSMC4CLK	—	—	P4CPRE<1:0>		—	—	P4CSRC<1:0>		--00 --00	--00 --00
F15h	PSMC4OEN	—	—	—	—	—	—	P4OEB	P4OEA	---- --00	---- --00
F16h	PSMC4POL	—	P4INPOL	—	—	—	—	P4POLB	P4POLA	-0-- --00	-0-- --00
F17h	PSMC4BLNK	—	—	P4FEBM<1:0>		—	—	P4REBM<1:0>		--00 --00	--00 --00
F18h	PSMC4REBS	P4REBSIN	—	—	P4REBSC4	P4REBSC3	P4REBSC2	P4REBSC1	—	0--0 000-	0--0 000-
F19h	PSMC4FEBS	P4FEBSIN	—	—	P4FEBSC4	P4FEBSC3	P4FEBSC2	P4FEBSC1	—	0--0 000-	0--0 000-
F1Ah	PSMC4PHS	P4PHSIN	—	—	P4PHSC4	P4PHSC3	P4PHSC2	P4PHSC1	P4PHST	0--0 0000	0--0 0000
F1Bh	PSMC4DCS	P4DCSIN	—	—	P4DCSC4	P4DCSC3	P4DCSC2	P4DCSC1	P4DCST	0--0 0000	0--0 0000
F1Ch	PSMC4PRS	P4PRSIN	—	—	P4PRSC4	P4PRSC3	P4PRSC2	P4PRSC1	P4PRST	0--0 0000	0--0 0000
F1Dh	PSMC4ASDC	P4ASE	P4ASDEN	P4ARSEN	—	—	—	—	P4ASDOV	000- ---0	000- ---0
F1Eh	PSMC4ASDL	—	—	—	—	—	—	P4ASDLB	P4ASDLA	---- --00	---- --00
F1Fh	PSMC4ASDS	P4ASDSIN	—	—	P4ASDSC4	P4ASDSC3	P4ASDSC2	P4ASDSC1	—	0--0 000-	0--0 000-
F20h	PSMC4INT	P4TOVIE	P4TPHIE	P4TDCIE	P4TPRIE	P4TOVIF	P4TPHIF	P4TDCIF	P4TPRIF	0000 0000	0000 0000
F21h	PSMC4PHL	Phase Low Count								0000 0000	0000 0000
F22h	PSMC4PHH	Phase High Count								0000 0000	0000 0000
F23h	PSMC4DCL	Duty Cycle Low Count								0000 0000	0000 0000
F24h	PSMC4DCH	Duty Cycle High Count								0000 0000	0000 0000
F25h	PSMC4PRL	Period Low Count								0000 0000	0000 0000
F26h	PSMC4PRH	Period High Count								0000 0000	0000 0000
F27h	PSMC4TMRL	Time base Low Counter								0000 0001	0000 0001
F28h	PSMC4TMRH	Time base High Counter								0000 0000	0000 0000
F29h	PSMC4DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
F2Ah	PSMC4DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
F2Bh	PSMC4BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
F2Ch	PSMC4BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
F2Dh	PSMC4FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
F2Eh	PSMC4STR0	—	—	—	—	—	—	P4STRB	P4STRA	---- --01	---- --01
F2Fh	PSMC4STR1	P4SSYNC	—	—	—	—	—	P4LSMEN	P4HSMEN	0--- --00	0--- --00

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

FIGURE 6-7: INTERNAL OSCILLATOR SWITCH TIMING



13.3.7 PORTA FUNCTIONS AND OUTPUT PRIORITIES

Each PORTA pin is multiplexed with other functions. The pins, their combined functions and their output priorities are shown in Table 13-2.

When multiple outputs are enabled, the actual pin control goes to the peripheral with the highest priority.

Analog input functions, such as ADC, and comparator inputs, are not shown in the priority lists. These inputs are active when the I/O pin is set for Analog mode using the ANSELx registers. Digital output functions may control the pin when it is in Analog mode with the priority shown in the priority list.

TABLE 13-2: PORTA OUTPUT PRIORITY

Pin Name	Function Priority(1)
RA0	RA0
RA1	OPA1OUT RA1
RA2	DAC1OUT1 RA2
RA3	RA3
RA4	C1OUT RA4
RA5	C2OUT RA5
RA6	CLKOUT C2OUT RA6
RA7	RA7

Note 1: Priority listed from highest to lowest.

19.4 Operation During Sleep

When the device wakes up from Sleep through an interrupt or a Watchdog Timer time-out, the contents of the DAC1CON0 register are not affected. To minimize current consumption in Sleep mode, the voltage reference should be disabled.

19.5 Effects of a Reset

A device Reset affects the following:

- DAC is disabled.
- DAC output voltage is removed from the DAC1OUT pin.
- The DAC1R<7:0> range select bits are cleared.

23.11 Register Definitions: Timer1 Control

T

REGISTER 23-1: T1CON: TIMER1 CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	U-0	R/W-0/u
TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-6 **TMR1CS<1:0>:** Timer1 Clock Source Select bits

11 = Reserved, do not use.
10 = Timer1 clock source is pin or oscillator:
If T1OSCEN = 0:
External clock from T1CKI pin (on the rising edge)
If T1OSCEN = 1:
Crystal oscillator on T1OSI/T1OSO pins
01 = Timer1 clock source is system clock (FOSC)
00 = Timer1 clock source is instruction clock (FOSC/4)

bit 5-4 **T1CKPS<1:0>:** Timer1 Input Clock Prescale Select bits

11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value

bit 3 **T1OSCEN:** LP Oscillator Enable Control bit

1 = Dedicated Timer1 oscillator circuit enabled
0 = Dedicated Timer1 oscillator circuit disabled

bit 2 **$\overline{\text{T1SYNC}}$:** Timer1 Synchronization Control bit

1 = Do not synchronize asynchronous clock input
0 = Synchronize asynchronous clock input with system clock (FOSC)

bit 1 **Unimplemented:** Read as ‘0’

bit 0 **TMR1ON:** Timer1 On bit

1 = Enables Timer1
0 = Stops Timer1 and clears Timer1 gate flip-flop

26.2.6 CLOCK PRESCALER

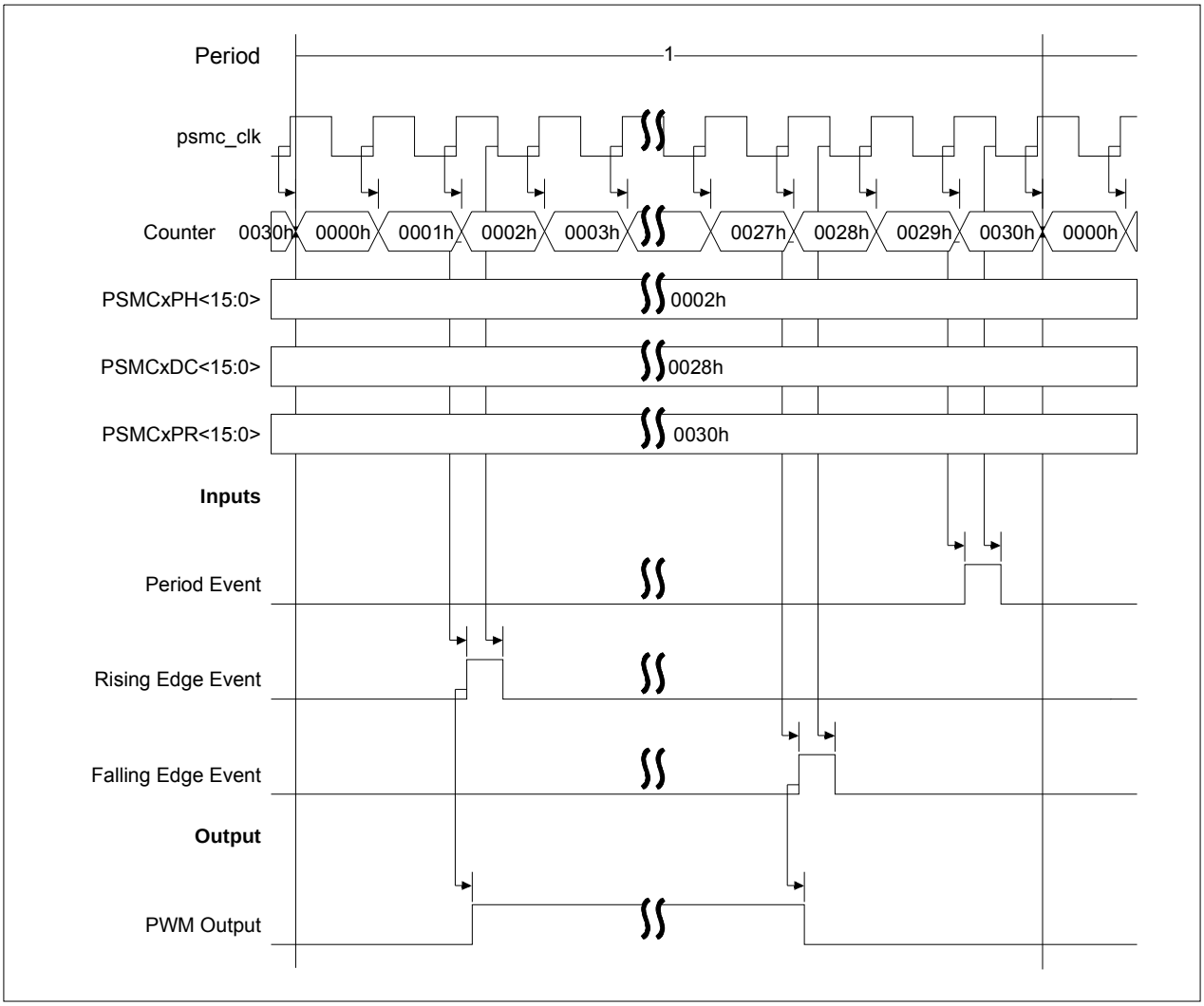
There are four prescaler choices available to be applied to the selected clock:

- Divide by 1
- Divide by 2
- Divide by 4
- Divide by 8

The clock source is selected with the PxCPRE<1:0> bits of the PSMCx Clock Control (PSMCxCLK) register (Register 26-7).

The prescaler output is psmc_clk, which is the clock used by all of the other portions of the PSMC module.

FIGURE 26-3: TIME BASE WAVEFORM GENERATION



26.3.6 PUSH-PULL PWM WITH FOUR FULL-BRIDGE AND COMPLEMENTARY OUTPUTS

The push-pull PWM is used to drive transistor bridge circuits as well as synchronous switches on the secondary side of the bridge. It uses six outputs and generates PWM signals with dead band that alternate between the six outputs in even and odd cycles.

26.3.6.1 Mode Features and Controls

- Dead-band control is available
- No steering control available
- Primary PWM is output on the following four pins:
  - PSMCxA
  - PSMCxB
  - PSMCxC
  - PSMCxD
- Complementary PWM is output on the following two pins:
  - PSMCxE
  - PSMCxF

Note: PSMCxA and PSMCxC are identical waveforms, and PSMCxB and PSMCxD are identical waveforms.

26.3.6.2 Waveform Generation

Push-pull waveforms generate alternating outputs on two sets of pin. Therefore, there are two sets of rising edge events and two sets of falling edge events

Odd numbered period rising edge event:

- PSMCxE is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxA and PSMCxC are set active

Odd numbered period falling edge event:

- PSMCxA and PSMCxC are set inactive
- Dead-band falling is activated (if enabled)
- PSMCxE is set active

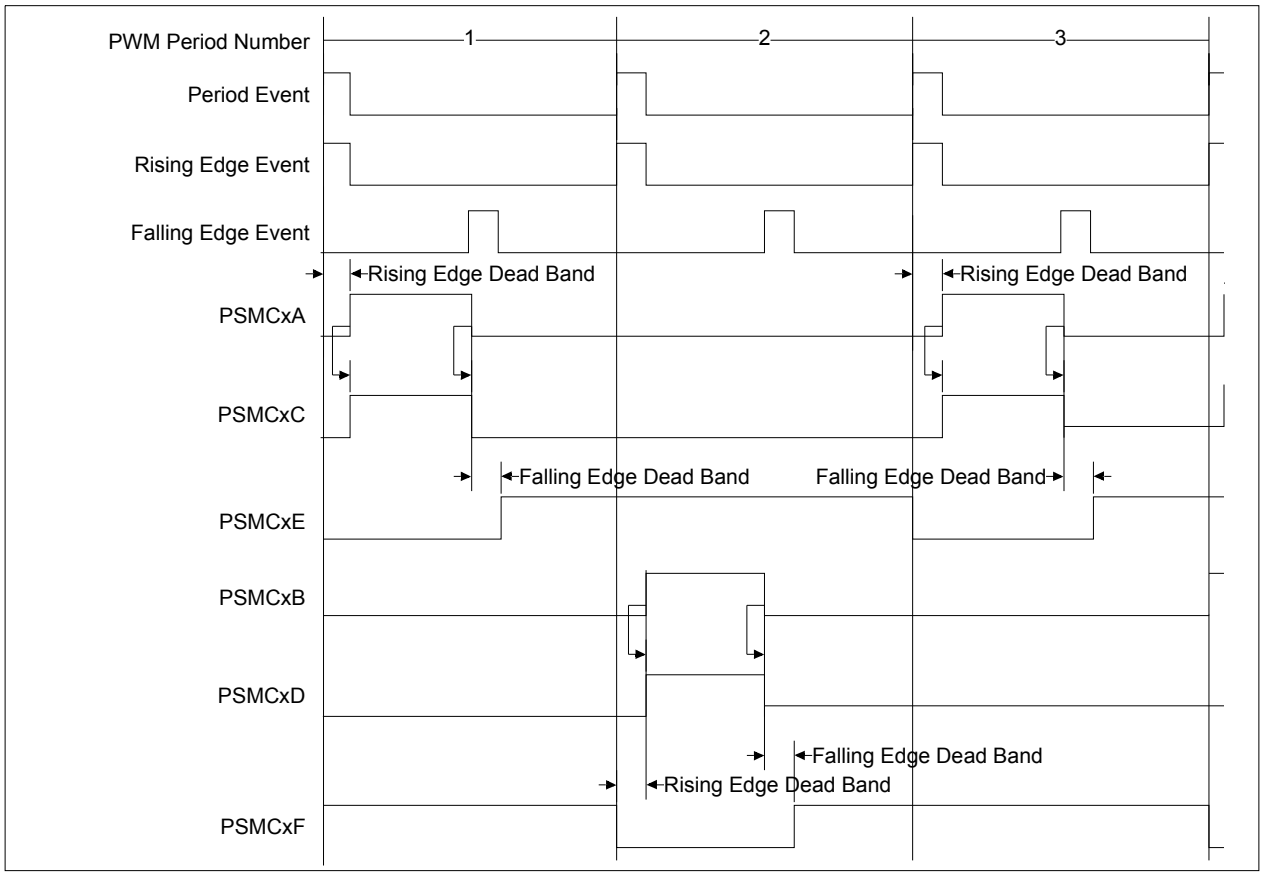
Even numbered period rising edge event:

- PSMCxF is set inactive
- Dead-band rising is activated (if enabled)
- PSMCxB and PSMCxD are set active

Even numbered period falling edge event:

- PSMCxB and PSMCxOUT3 are set inactive
- Dead-band falling is activated (if enabled)
- PSMCxF is set active

FIGURE 26-9: PUSH-PULL 4 FULL-BRIDGE AND COMPLEMENTARY PWM



26.4 Dead-Band Control

The dead-band control provides non-overlapping PWM signals to prevent shoot-through current in series connected power switches. Dead-band control is available only in modes with complementary drive and when changing direction in the ECCP compatible Full-Bridge modes.

The module contains independent 8-bit dead-band counters for rising edge and falling edge dead-band control.

26.4.1 DEAD-BAND TYPES

There are two separate dead-band generators available, one for rising edge events and the other for falling edge events.

26.4.1.1 Rising Edge Dead Band

Rising edge dead-band control is used to delay the turn-on of the primary switch driver from when the complementary switch driver is turned off.

Rising edge dead band is initiated with the rising edge event.

Rising edge dead-band time is adjusted with the PSMC Rising Edge Dead-Band Time (PSMCxDBR) register (Register 26-27).

If the PSMCxDBR register value is changed when the PSMC is enabled, the new value does not take effect until the first period event after the PSMCxLD bit is set.

26.4.1.2 Falling Edge Dead Band

Falling edge dead-band control is used to delay the turn-on of the complementary switch driver from when the primary switch driver is turned off.

Falling edge dead band is initiated with the falling edge event.

Falling edge dead-band time is adjusted with the PSMC Falling Edge Dead-Band Time (PSMCxDBF) register (Register 26-28).

If the PSMCxDBF register value is changed when the PSMC is enabled, the new value does not take effect until the first period event after the PSMCxLD bit is set.

26.4.2 DEAD-BAND ENABLE

When a mode is selected that may use dead-band control, dead-band timing is enabled by setting one of the enable bits in the PSMC Control (PSMCxCON) register (Register 26-1).

Rising edge dead band is enabled with the PxDBRE bit.

Rising edge dead band is enabled with the PxDBFE bit.

Enable changes take effect immediately.

26.4.3 DEAD-BAND CLOCK SOURCE

The dead-band counters are incremented on every rising edge of the psmc_clk signal.

26.4.4 DEAD-BAND UNCERTAINTY

When the rising and falling edge events that trigger the dead-band counters come from asynchronous inputs, there will be uncertainty in the actual dead-band time of each cycle. The maximum uncertainty is equal to one psmc_clk period. The one clock of uncertainty may still be introduced, even when the dead-band count time is cleared to zero.

26.4.5 DEAD-BAND OVERLAP

There are two cases of dead-band overlap and each is treated differently due to system requirements.

26.4.5.1 Rising to Falling Overlap

In this case, the falling edge event occurs while the rising edge dead-band counter is still counting. The following sequence occurs:

1. Dead-band rising count is terminated.
2. Dead-band falling count is initiated.
3. Primary output is suppressed.

26.4.5.2 Falling to Rising Overlap

In this case, the rising edge event occurs while the falling edge dead-band counter is still counting. The following sequence occurs:

1. Dead-band falling count is terminated.
2. Dead-band rising count is initiated.
3. Complementary output is suppressed.

26.4.5.3 Rising Edge-to-Rising Edge or Falling Edge-to-Falling Edge

In cases where one of the two dead-band counters is set for a short period, or disabled all together, it is possible to get rising-to-rising or falling-to-falling overlap. When this is the case, the following sequence occurs:

1. Dead-band count is terminated.
2. Dead-band count is restarted.
3. Output waveform control freezes in the present state.
4. Restarted dead-band count completes.
5. Output control resumes normally.

REGISTER 26-14: PSMCxDCS: PSMC DUTY CYCLE SOURCE REGISTER(1)

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PxDCSIN	—	—	PxDCSC4	PxDCSC3	PxDCSC2	PxDCSC1	PxDCST
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxDCSIN:** PSMCx Falling Edge Event occurs on PSMCxIN pin
- 1 = Falling edge event will occur when PSMCxIN pin goes true
- 0 = PSMCxIN pin will not cause falling edge event

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxDCSC4:** PSMCx Falling Edge Event occurs on sync_C4OUT output
- 1 = Falling edge event will occur when sync_C4OUT output goes true
- 0 = sync_C4OUT will not cause falling edge event

bit 3 **PxDCSC3:** PSMCx Falling Edge Event occurs on sync_C3OUT output
- 1 = Falling edge event will occur when sync_C3OUT output goes true
- 0 = sync_C3OUT will not cause falling edge event

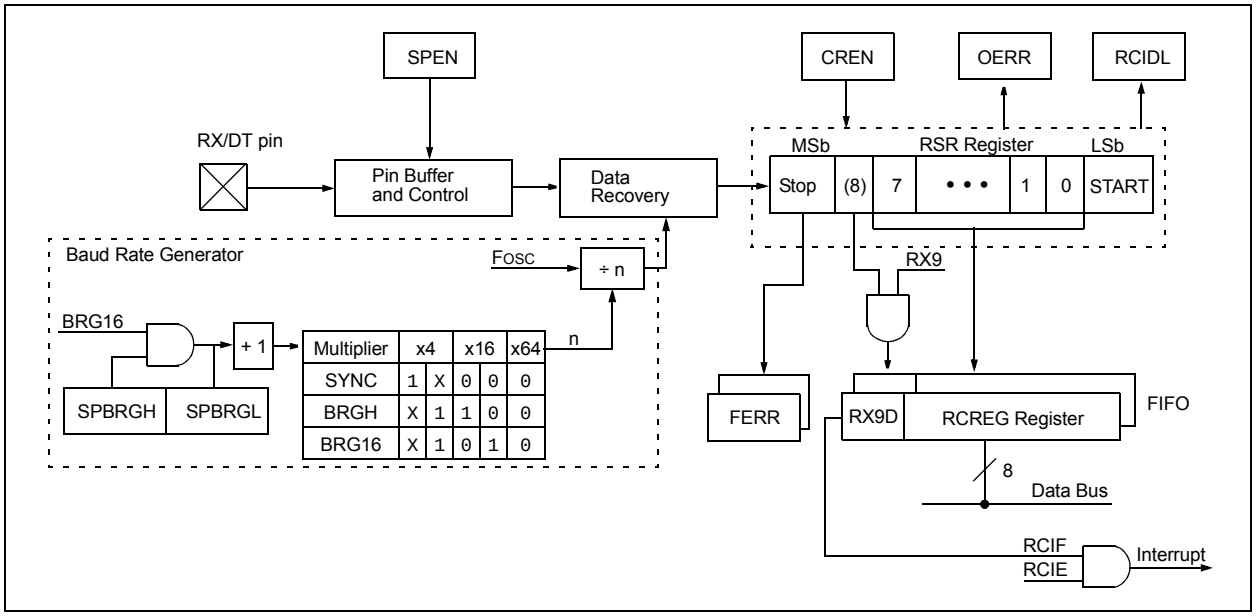
bit 2 **PxDCSC2:** PSMCx Falling Edge Event occurs on sync_C2OUT output
- 1 = Falling edge event will occur when sync_C2OUT output goes true
- 0 = sync_C2OUT will not cause falling edge event

bit 1 **PxDCSC1:** PSMCx Falling Edge Event occurs on sync_C1OUT output
- 1 = Falling edge event will occur when sync_C1OUT output goes true
- 0 = sync_C1OUT will not cause falling edge event

bit 0 **PxDCST:** PSMCx Falling Edge Event occurs on Time Base match
- 1 = Falling edge event will occur when PSMCxTMR = PSMCxDC
- 0 = Time base will not cause falling edge event

Note 1: Sources are not mutually exclusive: more than one source can cause a falling edge event.

FIGURE 28-2: EUSART RECEIVE BLOCK DIAGRAM



The operation of the EUSART module is controlled through three registers:

- Transmit Status and Control (TXSTA)
- Receive Status and Control (RCSTA)
- Baud Rate Control (BAUDCON)

These registers are detailed in Register 28-1, Register 28-2 and Register 28-3, respectively.

When the receiver or transmitter section is not enabled then the corresponding RX or TX pin may be used for general purpose input and output.

TABLE 28-5: BAUD RATES FOR ASYNCHRONOUS MODES

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	1221	1.73	255	1200	0.00	239	1200	0.00	143
2400	2404	0.16	207	2404	0.16	129	2400	0.00	119	2400	0.00	71
9600	9615	0.16	51	9470	-1.36	32	9600	0.00	29	9600	0.00	17
10417	10417	0.00	47	10417	0.00	29	10286	-1.26	27	10165	-2.42	16
19.2k	19.23k	0.16	25	19.53k	1.73	15	19.20k	0.00	14	19.20k	0.00	8
57.6k	55.55k	-3.55	3	—	—	—	57.60k	0.00	7	57.60k	0.00	2
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	300	0.16	207	300	0.00	191	300	0.16	51
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	—	—	—
9600	9615	0.16	12	—	—	—	9600	0.00	5	—	—	—
10417	10417	0.00	11	10417	0.00	5	—	—	—	—	—	—
19.2k	—	—	—	—	—	—	19.20k	0.00	2	—	—	—
57.6k	—	—	—	—	—	—	57.60k	0.00	0	—	—	—
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 0											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	—	—	—	—	—	—	—	—	—
2400	—	—	—	—	—	—	—	—	—	—	—	—
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.82k	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.64k	2.12	16	113.64k	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

28.5 EUSART Synchronous Mode

Synchronous serial communications are typically used in systems with a single master and one or more slaves. The master device contains the necessary circuitry for baud rate generation and supplies the clock for all devices in the system. Slave devices can take advantage of the master clock by eliminating the internal clock generation circuitry.

There are two signal lines in Synchronous mode: a bidirectional data line and a clock line. Slaves use the external clock supplied by the master to shift the serial data into and out of their respective receive and transmit shift registers. Since the data line is bidirectional, synchronous operation is half-duplex only. Half-duplex refers to the fact that master and slave devices can receive and transmit data but not both simultaneously. The EUSART can operate as either a master or slave device.

Start and Stop bits are not used in synchronous transmissions.

28.5.1 SYNCHRONOUS MASTER MODE

The following bits are used to configure the EUSART for synchronous master operation:

- SYNC = 1
- CSRC = 1
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Setting the CSRC bit of the TXSTA register configures the device as a master. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

28.5.1.1 Master Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a master transmits the clock on the TX/CK line. The TX/CK pin output driver is automatically enabled when the EUSART is configured for synchronous transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One clock cycle is generated for each data bit. Only as many clock cycles are generated as there are data bits.

28.5.1.2 Clock Polarity

A clock polarity option is provided for Microwire compatibility. Clock polarity is selected with the SCKP bit of the BAUDCON register. Setting the SCKP bit sets the clock Idle state as high. When the SCKP bit is set, the data changes on the falling edge of each clock. Clearing the SCKP bit sets the Idle state as low. When the SCKP bit is cleared, the data changes on the rising edge of each clock.

28.5.1.3 Synchronous Master Transmission

Data is transferred out of the device on the RX/DT pin. The RX/DT and TX/CK pin output drivers are automatically enabled when the EUSART is configured for synchronous master transmit operation.

A transmission is initiated by writing a character to the TXREG register. If the TSR still contains all or part of a previous character the new character data is held in the TXREG until the last bit of the previous character has been transmitted. If this is the first character, or the previous character has been completely flushed from the TSR, the data in the TXREG is immediately transferred to the TSR. The transmission of the character commences immediately following the transfer of the data to the TSR from the TXREG.

Each data bit changes on the leading edge of the master clock and remains valid until the subsequent leading clock edge.

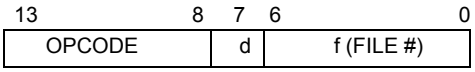
Note:	The TSR register is not mapped in data memory, so it is not available to the user.

28.5.1.4 Synchronous Master Transmission Set-up:

1. Initialize the SPBRGH, SPBRGL register pair and the BRGH and BRG16 bits to achieve the desired baud rate (see **Section 28.4 “EUSART Baud Rate Generator (BRG)”**).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Disable Receive mode by clearing bits SREN and CREN.
4. Enable Transmit mode by setting the TXEN bit.
5. If 9-bit transmission is desired, set the TX9 bit.
6. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
7. If 9-bit transmission is selected, the ninth bit should be loaded in the TX9D bit.
8. Start transmission by loading data to the TXREG register.

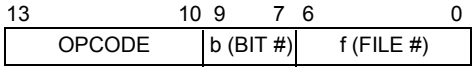
FIGURE 30-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations



d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

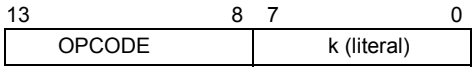
Bit-oriented file register operations



b = 3-bit bit address
f = 7-bit file register address

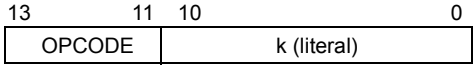
Literal and control operations

General



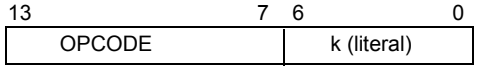
k = 8-bit immediate value

CALL and GOTO instructions only



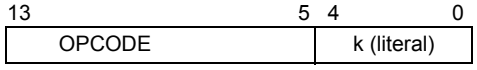
k = 11-bit immediate value

MOVLP instruction only



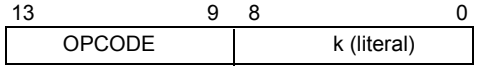
k = 7-bit immediate value

MOVLB instruction only



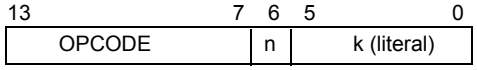
k = 5-bit immediate value

BRA instruction only



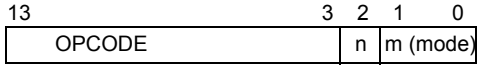
k = 9-bit immediate value

FSR Offset instructions



n = appropriate FSR
k = 6-bit immediate value

FSR Increment instructions



n = appropriate FSR
m = 2-bit mode value

OPCODE only

MOVWF **Move W to f**

Syntax: [*label*] MOVWF f

Operands: $0 \leq f \leq 127$

Operation: (W) → (f)

Status Affected: None

Description: Move data from W register to register 'f'.

Words: 1

Cycles: 1

Example:

```
MOVWF   OPTION_REG
```

Before Instruction
OPTION_REG = 0xFF
W = 0x4F
After Instruction
OPTION_REG = 0x4F
W = 0x4F

MOVWI **Move W to INDFn**

Syntax:
[*label*] MOVWI ++FSRn
[*label*] MOVWI --FSRn
[*label*] MOVWI FSRn++
[*label*] MOVWI FSRn--
[*label*] MOVWI k[FSRn]

Operands:
$n \in [0,1]$
$mm \in [00,01, 10, 11]$
$-32 \leq k \leq 31$

Operation: W → INDFn
Effective address is determined by
- FSR + 1 (preincrement)
- FSR - 1 (predecrement)
- FSR + k (relative offset)

After the Move, the FSR value will be either:
- FSR + 1 (all increments)
- FSR - 1 (all decrements)

Unchanged

Status Affected: None

Mode	Syntax	mm
Preincrement	++FSRn	00
Predecrement	--FSRn	01
Postincrement	FSRn++	10
Postdecrement	FSRn--	11

Description: This instruction is used to move data between W and one of the indirect registers (INDFn). Before/ after this move, the pointer (FSRn) is updated by pre/post incrementing/decrementing it.

Note: The INDFn registers are not physical registers. Any instruction that accesses an INDFn register actually accesses the register at the address specified by the FSRn.

FSRn is limited to the range 0000h - FFFFh. Incrementing/ decrementing it beyond these bounds will cause it to wrap-around.

The increment/decrement operation on FSRn WILL NOT affect any Status bits.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

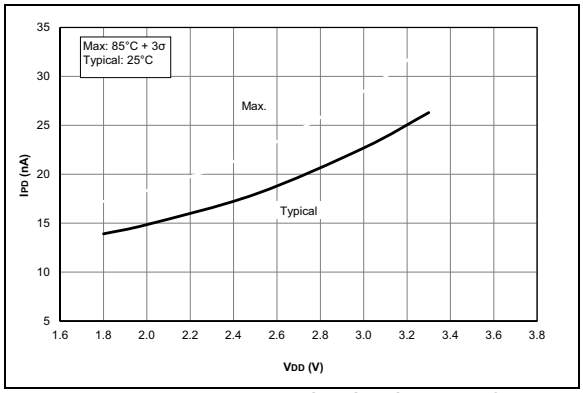


FIGURE 32-37: *IPD, Fixed Voltage Reference (FVR), PIC16LF1788/9 Only.*

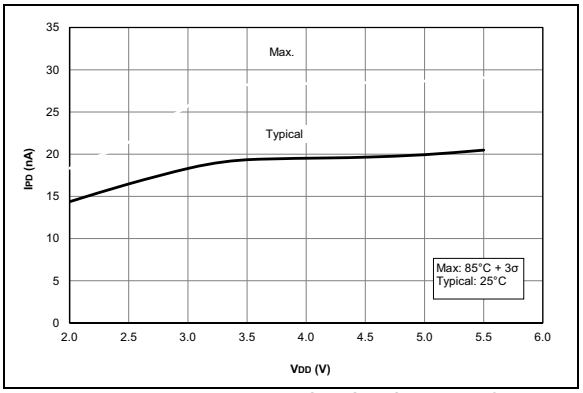


FIGURE 32-38: *IPD, Fixed Voltage Reference (FVR), PIC16F1788/9 Only.*

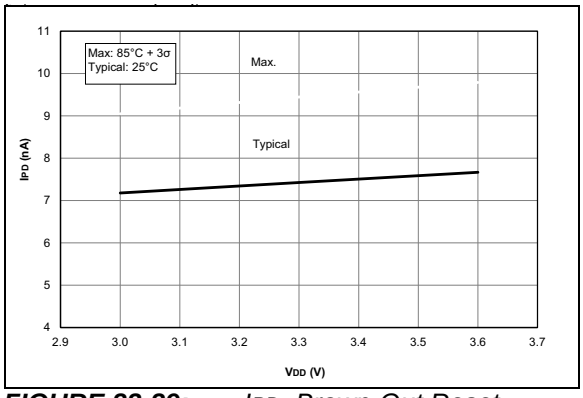


FIGURE 32-39: *IPD, Brown-Out Reset (BOR), BORV = 1, PIC16LF1788/9 Only.*

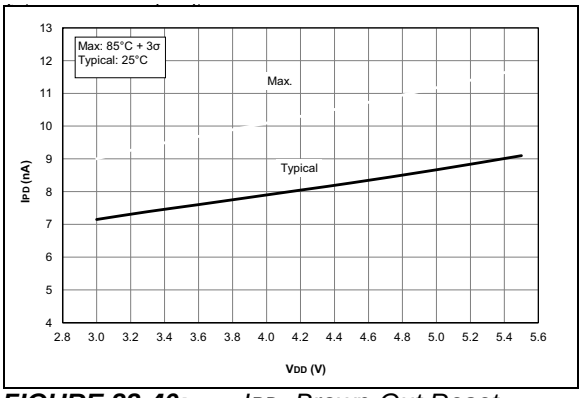


FIGURE 32-40: *IPD, Brown-Out Reset (BOR), BORV = 1, PIC16F1788/9 Only.*

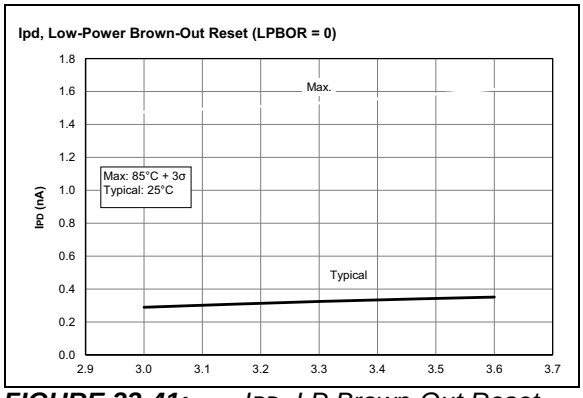


FIGURE 32-41: *IPD, LP Brown-Out Reset (LPBOR = 0), PIC16LF1788/9 Only.*

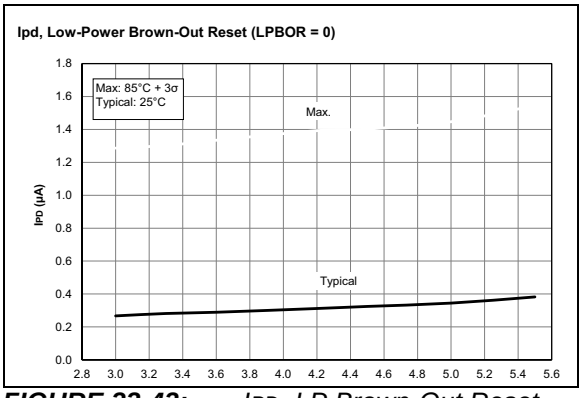
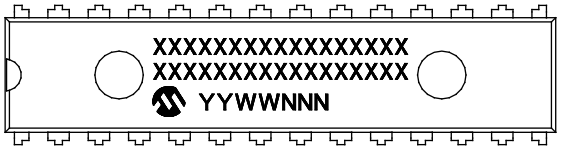


FIGURE 32-42: *IPD, LP Brown-Out Reset (LPBOR = 0), PIC16F1788/9 Only.*

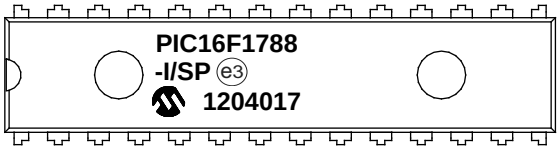
34.0 PACKAGING INFORMATION

34.1 Package Marking Information

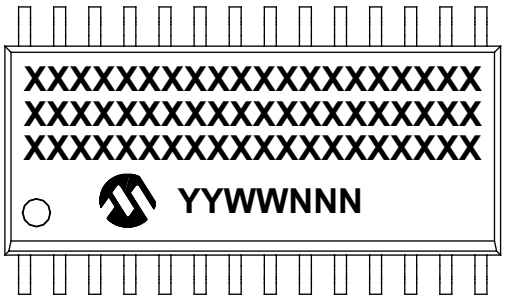
28-Lead SPDIP (.300”)



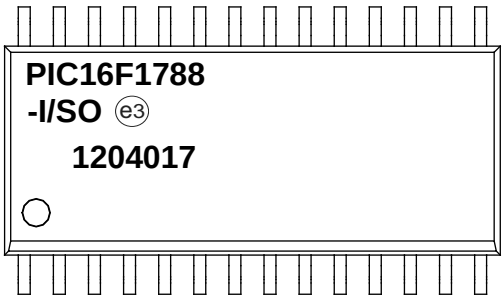
Example



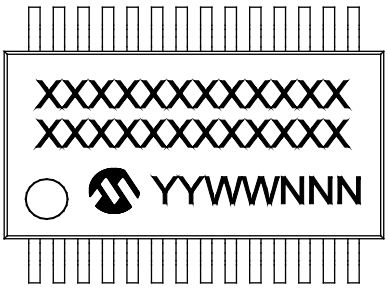
28-Lead SOIC (7.50 mm)



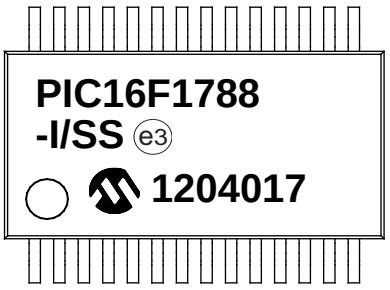
Example



28-Lead SSOP (5.30 mm)



Example

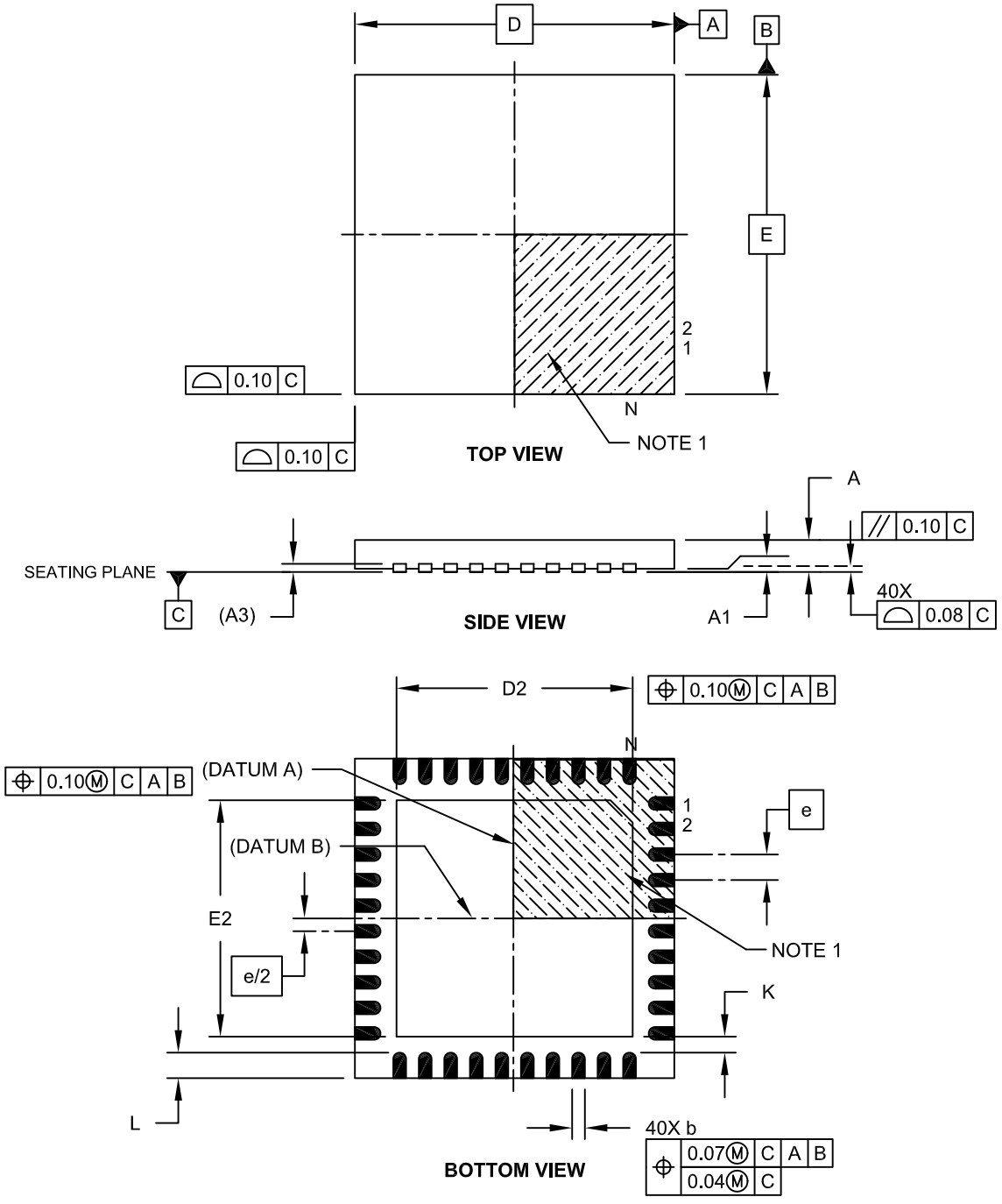


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

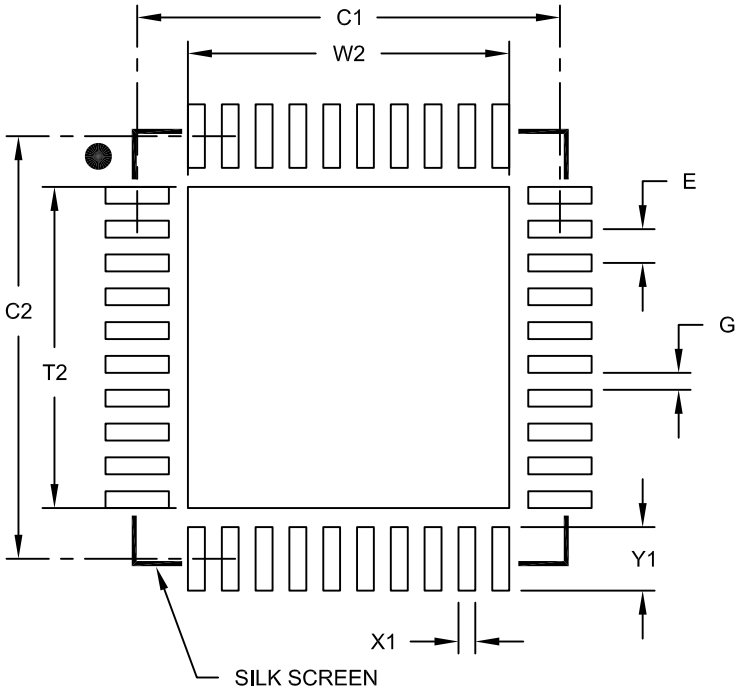
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-156A Sheet 1 of 2

40-Lead Plastic Ultra Thin Quad Flat, No Lead Package (MV) - 5x5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.40 BSC	
Optional Center Pad Width	W2			3.80
Optional Center Pad Length	T2			3.80
Contact Pad Spacing	C1		5.00	
Contact Pad Spacing	C2		5.00	
Contact Pad Width (X40)	X1			0.20
Contact Pad Length (X40)	Y1			0.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2156B