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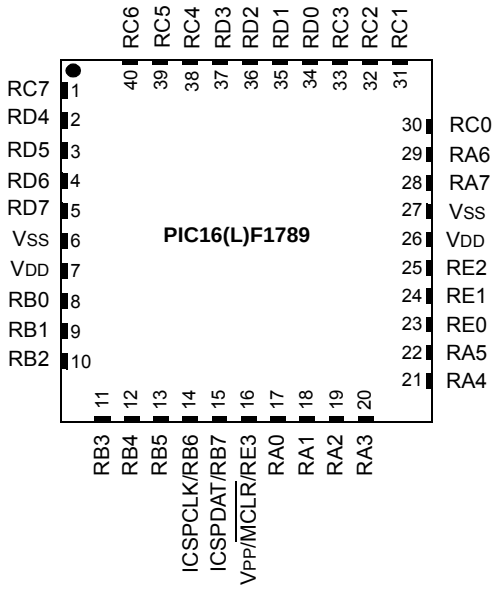
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

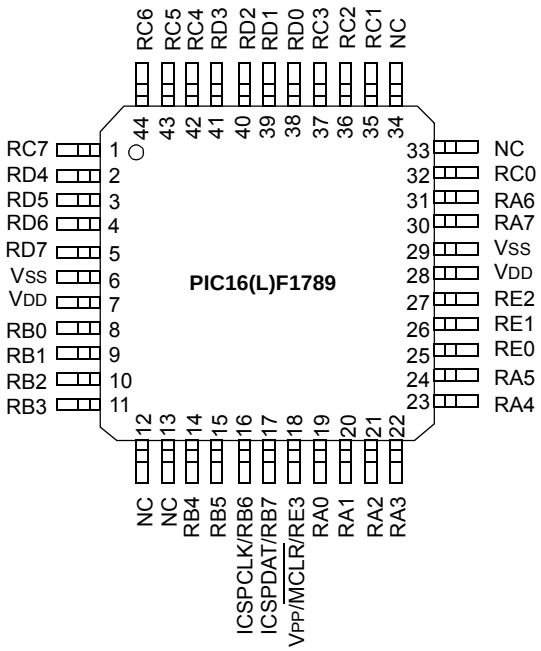
Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1788-e-ss

Pin Diagram – 40-Pin UQFN (5x5)



Note: See Table 2 for the location of all peripheral functions.

Pin Diagram – 44-Pin TQFP



Note: See Table 2 for the location of all peripheral functions.

TABLE 3-5: PIC16(L)F1788/9 MEMORY MAP (BANKS 8-28)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh		48Bh		50Bh		58Bh		60Bh		68Bh		70Bh		78Bh	
40Ch	Unimplemented Read as '0'	48Ch	Unimplemented Read as '0'	50Ch	See Table 3-6	58Ch	See Table 3-7	60Ch	Unimplemented Read as '0'	68Ch	Unimplemented Read as '0'	70Ch	Unimplemented Read as '0'	78Ch	Unimplemented Read as '0'
41Fh		49Fh		51Fh		59Fh		61Fh		69Fh		71Fh		79Fh	
420h	General Purpose Register 80 Bytes	4A0h	General Purpose Register 80 Bytes	520h	General Purpose Register 80 Bytes	5A0h	General Purpose Register 80 Bytes	620h	General Purpose Register 80 Bytes	6A0h	General Purpose Register 80 Bytes	720h	General Purpose Register 80 Bytes	7A0h	General Purpose Register 80 Bytes
46Fh		4EFh		56Fh		5EFh		66Fh		6EFh		76Fh		7EFh	
470h	Common RAM (Accesses 70h – 7Fh)	4F0h	Common RAM (Accesses 70h – 7Fh)	570h	Common RAM (Accesses 70h – 7Fh)	5F0h	Common RAM (Accesses 70h – 7Fh)	670h	Common RAM (Accesses 70h – 7Fh)	6F0h	Common RAM (Accesses 70h – 7Fh)	770h	Common RAM (Accesses 70h – 7Fh)	7F0h	Common RAM (Accesses 70h – 7Fh)
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	

BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh		88Bh		90Bh		98Bh		A0Bh		A8Bh		B0Bh		B8Bh	
80Ch	Unimplemented Read as '0'	88Ch	Unimplemented Read as '0'	90Ch	Unimplemented Read as '0'	98Ch	Unimplemented Read as '0'	A0Ch	Unimplemented Read as '0'	A8Ch	Unimplemented Read as '0'	B0Ch	Unimplemented Read as '0'	B8Ch	Unimplemented Read as '0'
81Fh		89Fh		91Fh		99Fh		A1Fh		A9Fh		B1Fh		B9Fh	
820h	General Purpose Register 80 Bytes	8A0h	General Purpose Register 80 Bytes	920h	General Purpose Register 80 Bytes	9A0h	General Purpose Register 80 Bytes	A20h	General Purpose Register 80 Bytes	AA0h	General Purpose Register 80 Bytes	B20h	General Purpose Register 80 Bytes	BA0h	General Purpose Register 80 Bytes
86Fh		8EFh		96Fh		9EFh		A6Fh		AEFh		B6Fh		BEFh	
870h	Common RAM (Accesses 70h – 7Fh)	8F0h	Common RAM (Accesses 70h – 7Fh)	970h	Common RAM (Accesses 70h – 7Fh)	9F0h	Common RAM (Accesses 70h – 7Fh)	A70h	Common RAM (Accesses 70h – 7Fh)	AF0h	Common RAM (Accesses 70h – 7Fh)	B70h	Common RAM (Accesses 70h – 7Fh)	BF0h	Common RAM (Accesses 70h – 7Fh)
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	

BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh		C8Bh		D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch	Unimplemented Read as '0'	C8Ch	Unimplemented Read as '0'	D0Ch	Unimplemented Read as '0'	D8Ch	Unimplemented Read as '0'	E0Ch	Unimplemented Read as '0'	E8Ch	See Figure 3-9	F0Ch	See Figure 3-10	F8Ch	See Figure 3-8
C1Fh		C9Fh													
C20h	General Purpose Register 80 Bytes	CA0h	General Purpose Register 32 Bytes												
C6Fh		CBFh													
C70h	Common RAM (Accesses 70h – 7Fh)	CC0h	Unimplemented Read as '0'	D6Fh	Common RAM (Accesses 70h – 7Fh)	DEFh	Common RAM (Accesses 70h – 7Fh)	E6Fh	Common RAM (Accesses 70h – 7Fh)	EEFh	Common RAM (Accesses 70h – 7Fh)	F6Fh	Common RAM (Accesses 70h – 7Fh)	FEFh	Common RAM (Accesses 70h – 7Fh)
C7Fh		CEFh		D70h		DF0h		E70h		EF0h		F70h		FF0h	
		CF0h		D7Fh		DFFh		E7Fh		EFFh		F7Fh		FFFh	
		CFFh													

Legend: = Unimplemented data memory locations, read as '0'

4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Words. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.4 "Write Protection"** for more information.

4.3.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the $\overline{CPD}$ bit. When $\overline{CPD}$ = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 12.5 "User ID, Device ID and Configuration Word Access"**for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F178X Memory Programming Specification"* (DS41457).

REGISTER 8-8: PIR3: PERIPHERAL INTERRUPT REQUEST REGISTER 3

U-0	U-0	U-0	R/W-0/0	U-0	U-0	U-0	U-0
—	—	—	CCP3IF	—	—	—	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-5 **Unimplemented:** Read as ‘0’

bit 4 **CCP3IF:** CCP3 Interrupt Flag bit
1 = Interrupt is pending
0 = Interrupt is not pending

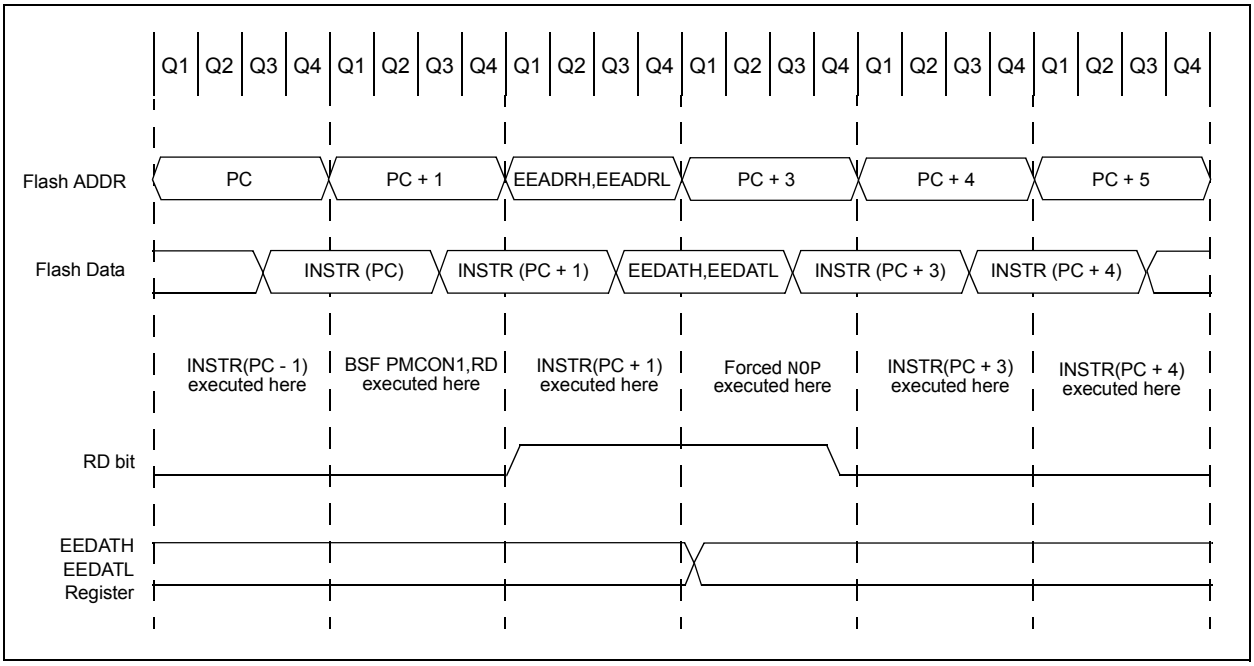
bit 3-0 **Unimplemented:** Read as ‘0’

EXAMPLE 12-2: DATA EEPROM WRITE

```
        BANKSEL  EEADRL          ;
        MOVLW    DATA_EE_ADDR    ;
        MOVWF    EEADRL          ;Data Memory Address to write
        MOVLW    DATA_EE_DATA    ;
        MOVWF    EEDATL          ;Data Memory Value to write
        BCF      EECON1, CFGS    ;Deselect Configuration space
        BCF      EECON1, EEPGD   ;Point to DATA memory
        BSF      EECON1, WREN    ;Enable writes

        BCF      INTCON, GIE     ;Disable INTs.
Required
Sequence
        MOVLW    55h             ;
        MOVWF    EECON2          ;Write 55h
        MOVLW    0AAh            ;
        MOVWF    EECON2          ;Write AAh
        BSF      EECON1, WR      ;Set WR bit to begin write
        BSF      INTCON, GIE     ;Enable Interrupts
        BCF      EECON1, WREN    ;Disable writes
        BTFSC    EECON1, WR      ;Wait for write to complete
        GOTO     $-2             ;Done
```

FIGURE 12-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION



18.1 Effects of Reset

A device Reset forces all registers to their Reset state. This disables the OPA module.

18.2 OPA Module Performance

Common AC and DC performance specifications for the OPA module:

- Common Mode Voltage Range
- Leakage Current
- Input Offset Voltage
- Open Loop Gain
- Gain Bandwidth Product

Common mode voltage range is the specified voltage range for the OPA+ and OPA- inputs, for which the OPA module will perform to within its specifications. The OPA module is designed to operate with input voltages between VSS and VDD. Behavior for Common mode voltages greater than VDD, or below VSS, are not guaranteed.

Leakage current is a measure of the small source or sink currents on the OPA+ and OPA- inputs. To minimize the effect of leakage currents, the effective impedances connected to the OPA+ and OPA- inputs should be kept as small as possible and equal.

Input offset voltage is a measure of the voltage difference between the OPA+ and OPA- inputs in a closed loop circuit with the OPA in its linear region. The offset voltage will appear as a DC offset in the output equal to the input offset voltage, multiplied by the gain of the circuit. The input offset voltage is also affected by the Common mode voltage. The OPA is factory calibrated to minimize the input offset voltage of the module.

Open loop gain is the ratio of the output voltage to the differential input voltage, (OPA+) - (OPA-). The gain is greatest at DC and falls off with frequency.

Gain Bandwidth Product or GBWP is the frequency at which the open loop gain falls off to 0 dB.

18.3 OPAxCON Control Register

The OPAxCON register, shown in Register 18-1, controls the OPA module.

The OPA module is enabled by setting the OPAxEN bit of the OPAxCON register. When enabled, the OPA forces the output driver of OPAxOUT pin into tri-state to prevent contention between the driver and the OPA output.

Note:	When the OPA module is enabled, the OPAxOUT pin is driven by the op amp output, not by the PORT digital driver. Refer to the Electrical specifications for the op amp output drive capability.

FIGURE 19-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

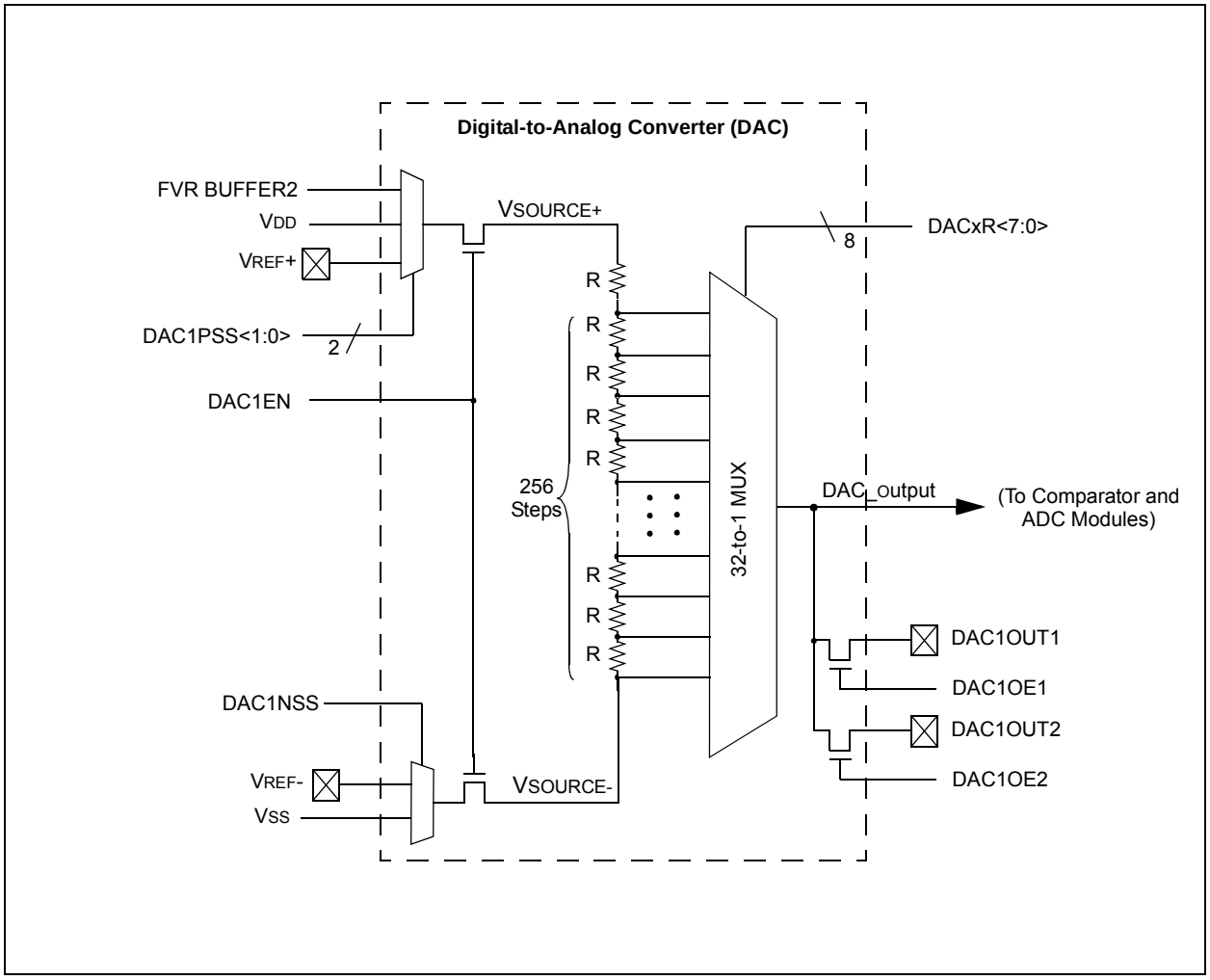
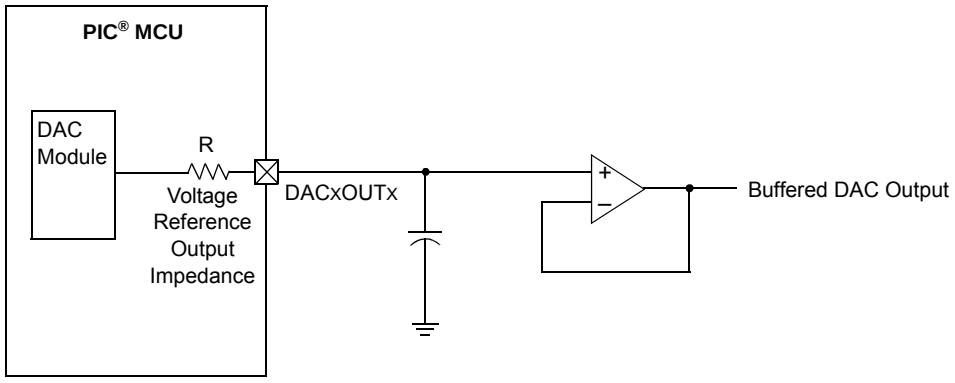


FIGURE 19-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



26.0 PROGRAMMABLE SWITCH MODE CONTROL (PSMC)

The Programmable Switch Mode Controller (PSMC) is a high-performance Pulse Width Modulator (PWM) that can be configured to operate in one of several modes to support single or multiple phase applications.

A simplified block diagram indicating the relationship between inputs, outputs, and controls is shown in Figure 26-1.

This section begins with the fundamental aspects of the PSMC operation. A more detailed description of operation for each mode is located later in **Section 26.3 "Modes of Operation"**

Modes of operation include:

- Single-phase
- Complementary Single-phase
- Push-Pull
- Push-Pull 4-Bridge
- Complementary Push-Pull 4-Bridge
- Pulse Skipping
- Variable Frequency Fixed Duty Cycle
- Complementary Variable Frequency Fixed Duty Cycle
- ECCP Compatible modes
  - Full-Bridge
  - Full-Bridge Reverse
- 3-Phase 6-Step PWM

26.3.11 VARIABLE FREQUENCY - FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS

This mode is the same as the single output Fixed Duty Cycle mode except a complementary output with dead-band control is generated.

The rising edge and falling edge events are unused in this mode. Therefore, a different triggering mechanism is required for the dead-band counters.

A period events that generate a rising edge on PSMCxA use the rising edge dead-band counters.

A period events that generate a falling edge on PSMCxA use the falling edge dead-band counters.

26.3.11.1 Mode Features

- Dead-band control is available
- No steering control available
- Fractional Frequency Adjust
  - Fine period adjustments are made with the PSMC Fractional Frequency Adjust (PSMCxFFA) register (Register 26-29)
- Primary PWM is output to the following pin:
  - PSMCxA
- Complementary PWM is output to the following pin:
  - PSMCxB

26.3.11.2 Waveform Generation

Period Event

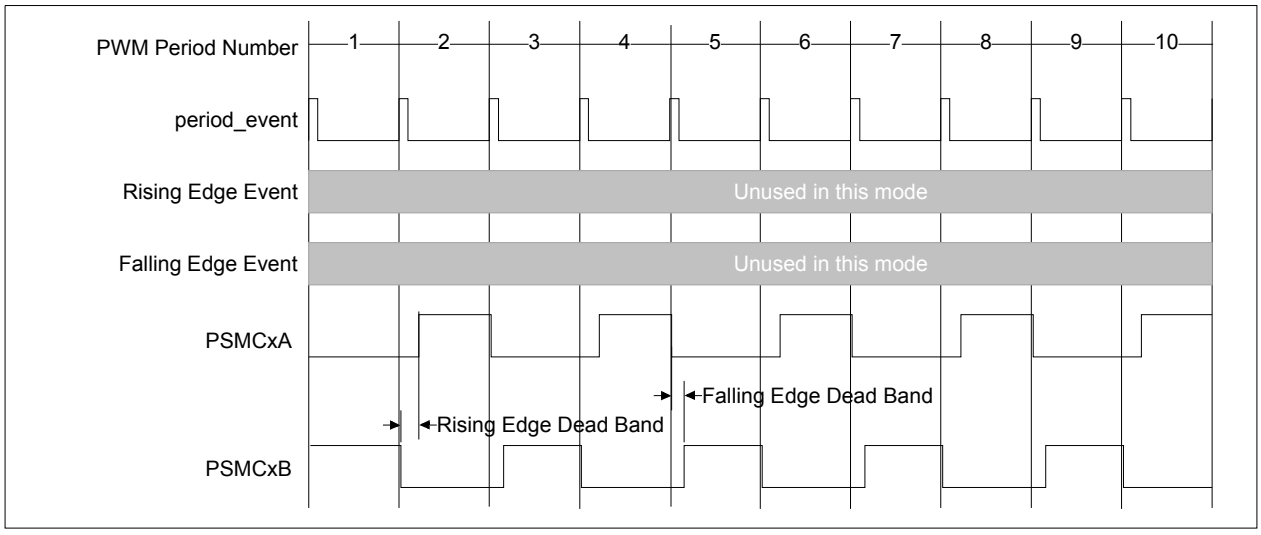
When output is going inactive to active:

- Complementary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register.
- Dead-band rising is activated (if enabled)
- Primary output is set active

When output is going active to inactive:

- Primary output is set inactive
- FFA counter is incremented by the 4-bit value in PSMCFFA register
- Dead-band falling is activated (if enabled)
- Complementary output is set active

FIGURE 26-14: VARIABLE FREQUENCY – FIXED DUTY CYCLE PWM WITH COMPLEMENTARY OUTPUTS WAVEFORM



26.5 Output Steering

Output steering allows for PWM signals generated by the PSMC module to be placed on different pins under software control. Synchronized steering will hold steering changes until the first period event after the PSMCxLD bit is set. Unsynchronized steering changes will take place immediately.

Output steering is available in the following modes:

- 3-phase PWM
- Single PWM
- Complementary PWM

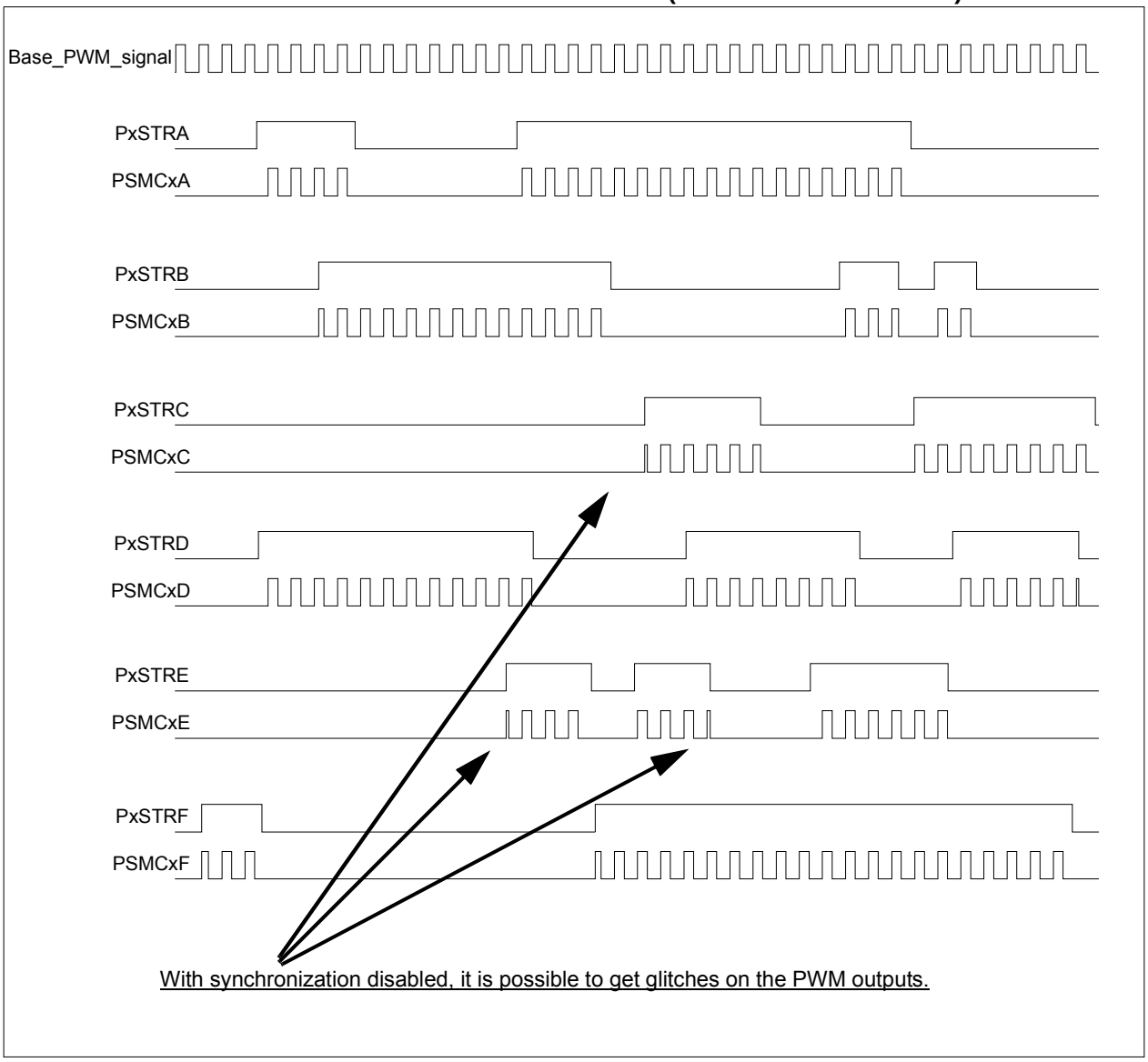
26.5.1 3-PHASE STEERING

3-phase steering is available in the 3-Phase Modulation mode only. For more details on 3-phase steering refer to **Section 26.3.12 "3-Phase PWM"**.

26.5.2 SINGLE PWM STEERING

In Single PWM Steering mode, the single PWM signal can be routed to any combination of the PSMC output pins. Examples of unsynchronized single PWM steering are shown in Figure 26-16.

FIGURE 26-16: SINGLE PWM STEERING WAVEFORM (NO SYNCHRONIZATION)



REGISTER 26-19: PSMCxTMRL: PSMC TIME BASE COUNTER LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxTMRL<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PSMCxTMRL<7:0>:** 16-bit PSMCx Time Base Counter Least Significant bits
= PSMCxTMR<7:0>

REGISTER 26-20: PSMCxTMRH: PSMC TIME BASE COUNTER HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1
PSMCxTMRH<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PSMCxTMRH<7:0>:** 16-bit PSMCx Time Base Counter Most Significant bits
= PSMCxTMR<15:8>

27.6.5 I²C MASTER MODE REPEATED START CONDITION TIMING

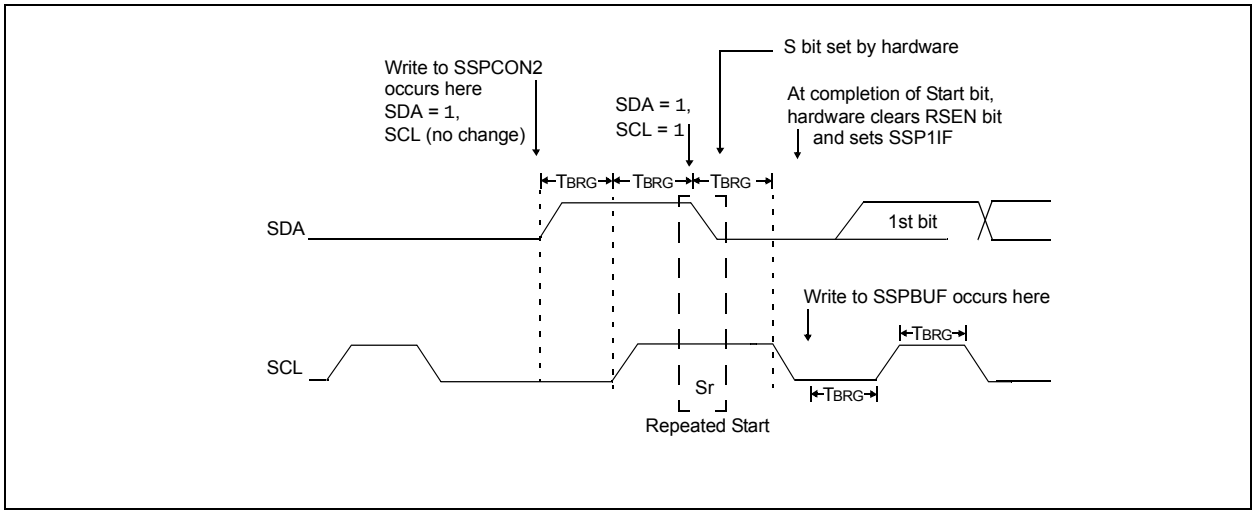
A Repeated Start condition occurs when the RSEN bit of the SSPCON2 register is programmed high and the master state machine is no longer active. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the Baud Rate Generator is loaded and begins counting. The SDA pin is released (brought high) for one Baud Rate Generator count (TBRG). When the Baud Rate Generator times out, if SDA is sampled high, the SCL pin will be deasserted (brought high). When SCL is sampled high, the Baud Rate Generator is reloaded and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG while SCL is high. SCL is asserted low. Following this, the RSEN bit of the SSPCON2 register will be automatically cleared and the Baud Rate Generator will not be reloaded, leaving the SDA pin held low. As soon as a Start condition is detected on the SDA and SCL pins, the S bit of the SSPSTAT register will be set. The SSP1IF bit will not be set until the Baud Rate Generator has timed out.

Note 1: If RSEN is programmed while any other event is in progress, it will not take effect.

2: A bus collision during the Repeated Start condition occurs if:

- SDA is sampled low when SCL goes from low-to-high.
- SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data '1'.

FIGURE 27-27: REPEAT START CONDITION WAVEFORM



28.3 Register Definitions: EUSART Control

REGISTER 28-1: TXSTA: TRANSMIT STATUS AND CONTROL REGISTER

R/W-/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-1/1	R/W-0/0
CSRC	TX9	TXEN(1)	SYNC	SENDB	BRGH	TRMT	TX9D
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CSRC:** Clock Source Select bit
Asynchronous mode:
Don't care
Synchronous mode:
1 = Master mode (clock generated internally from BRG)
0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit
1 = Selects 9-bit transmission
0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit(1)
1 = Transmit enabled
0 = Transmit disabled

bit 4 **SYNC:** EUSART Mode Select bit
1 = Synchronous mode
0 = Asynchronous mode

bit 3 **SENDB:** Send Break Character bit
Asynchronous mode:
1 = Send Sync Break on next transmission (cleared by hardware upon completion)
0 = Sync Break transmission completed
Synchronous mode:
Don't care

bit 2 **BRGH:** High Baud Rate Select bit
Asynchronous mode:
1 = High speed
0 = Low speed
Synchronous mode:
Unused in this mode

bit 1 **TRMT:** Transmit Shift Register Status bit
1 = TSR empty
0 = TSR full

bit 0 **TX9D:** Ninth bit of Transmit Data
Can be address/data bit or a parity bit.

Note 1: SREN/CREN overrides TXEN in Sync mode.

NOP	No Operation
Syntax:	[*label*] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.
Words:	1
Cycles:	1
Example:	`NOP`

OPTION	Load OPTION_REG Register with W
Syntax:	[*label*] OPTION
Operands:	None
Operation:	(W) → OPTION_REG
Status Affected:	None
Description:	Move data from W register to OPTION_REG register.

RESET	Software Reset
Syntax:	[*label*] RESET
Operands:	None
Operation:	Execute a device Reset. Resets the $\overline{RI}$ flag of the PCON register.
Status Affected:	None
Description:	This instruction provides a way to execute a hardware Reset by software.

RETFIE	Return from Interrupt
Syntax:	[*label*] RETFIE
Operands:	None
Operation:	TOS → PC, 1 → GIE
Status Affected:	None
Description:	Return from Interrupt. Stack is POPed and Top-of-Stack (TOS) is loaded in the PC. Interrupts are enabled by setting Global Interrupt Enable bit, GIE (INTCON<7>). This is a 2-cycle instruction.
Words:	1
Cycles:	2
Example:	`RETFIE` After Interrupt PC = TOS GIE = 1

RETLW	Return with literal in W
Syntax:	[*label*] RETLW k
Operands:	0 ≤ k ≤ 255
Operation:	k → (W); TOS → PC
Status Affected:	None
Description:	The W register is loaded with the 8-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a 2-cycle instruction.
Words:	1
Cycles:	2

Example:	`CALL TABLE;W contains table`
	`;offset value`
	`TABLE ;W now has table value`
	`•`
	`•`
	`•`
	`ADDWF PC ;W = offset`
	`RETLW k1 ;Begin table`
	`RETLW k2 ;`
	`•`
	`•`
	`•`
	`RETLW kn ; End of table`
	
	Before Instruction
	W = 0x07
	After Instruction
	W = value of k8

31.4 Thermal Considerations

Standard Operating Conditions (unless otherwise stated)					
Param No.	**Sym.**	**Characteristic**	**Typ.**	**Units**	**Conditions**
TH01	θ_{JA}	Thermal Resistance Junction to Ambient	60	°C/W	28-pin SPDIP package
			80	°C/W	28-pin SOIC package
			90	°C/W	28-pin SSOP package
			27.5	°C/W	28-pin QFN 6x6mm package
			47.2	°C/W	40-pin DIP package
			41	°C/W	40-pin UQFN 5x5
			46	°C/W	44-pin TQFP package
			24.4	°C/W	44-pin QFN 8x8mm package
TH02	θ_{JC}	Thermal Resistance Junction to Case	31.4	°C/W	28-pin SPDIP package
			24	°C/W	28-pin SOIC package
			24	°C/W	28-pin SSOP package
			24	°C/W	28-pin QFN 6x6mm package
			24.7	°C/W	40-pin DIP package
			5.5	°C/W	40-pin UQFN 5x5
			14.5	°C/W	44-pin TQFP package
			20	°C/W	44-pin QFN 8x8mm package
TH03	T_{JMAX}	Maximum Junction Temperature	150	°C	
TH04	PD	Power Dissipation	—	W	$PD = P_{INTERNAL} + P_{I/O}$
TH05	$P_{INTERNAL}$	Internal Power Dissipation	—	W	$P_{INTERNAL} = I_{DD} \times V_{DD}$ (1)
TH06	$P_{I/O}$	I/O Power Dissipation	—	W	$P_{I/O} = \Sigma (I_{OL} * V_{OL}) + \Sigma (I_{OH} * (V_{DD} - V_{OH}))$
TH07	P_{DER}	Derated Power	—	W	$P_{DER} = PD_{MAX} (T_J - T_A)/\theta_{JA}$ (2)

Note 1: I_{DD} is current to run the chip alone without driving any load on the output pins.
2: T_A = Ambient Temperature
3: T_J = Junction Temperature

TABLE 31-8: PLL CLOCK TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
F10	FOSC	Oscillator Frequency Range	4	—	8	MHz	
F11	FSYS	On-Chip VCO System Frequency	16	—	32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%	—	+0.25%	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 31-7: CLKOUT AND I/O TIMING

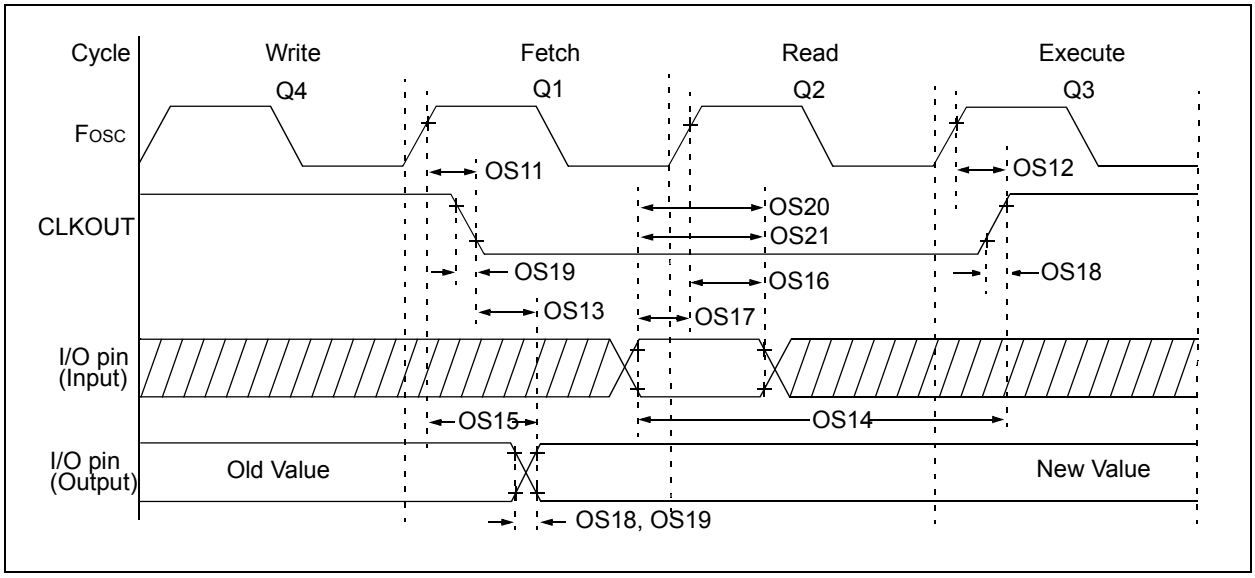
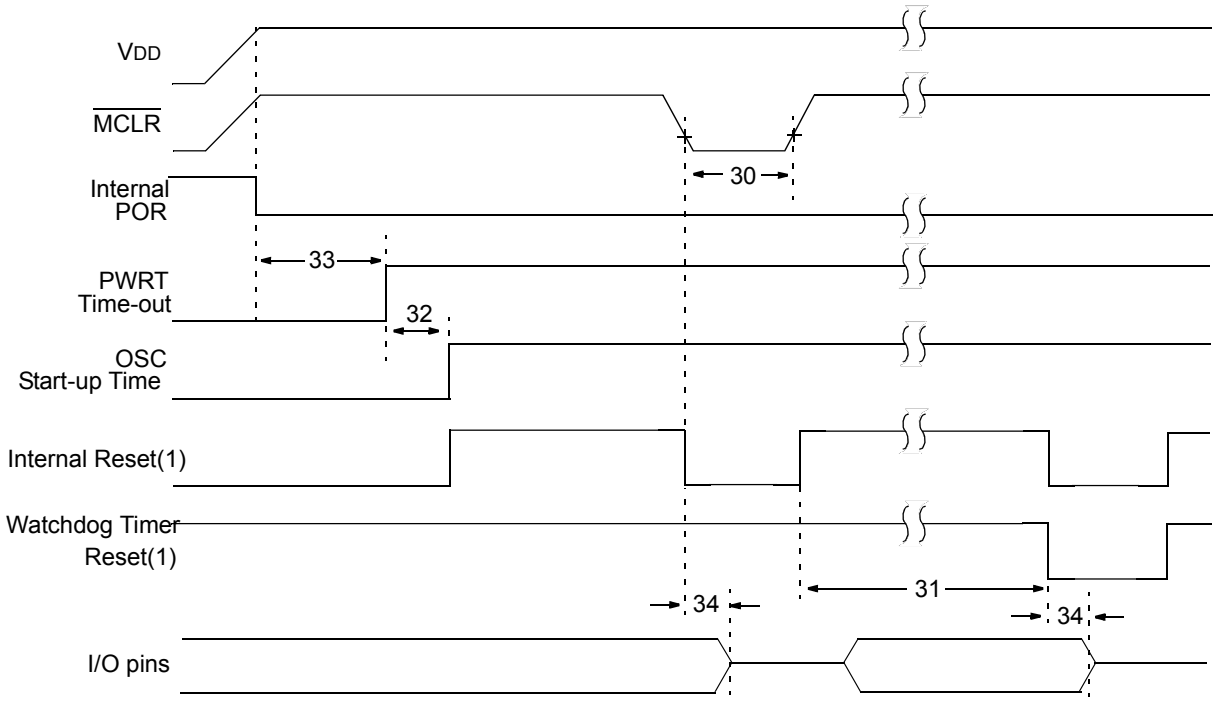
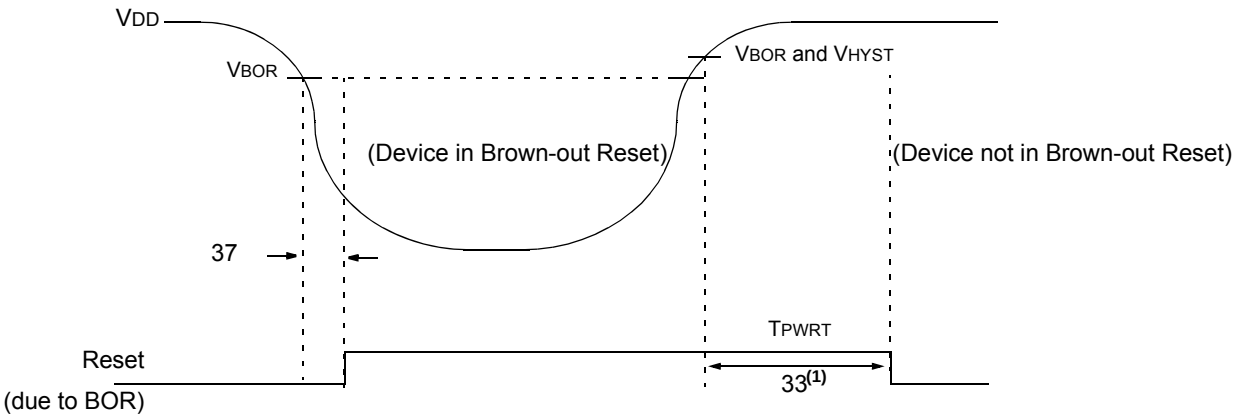


FIGURE 31-8: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING



Note 1: Asserted low.

FIGURE 31-9: BROWN-OUT RESET TIMING AND CHARACTERISTICS



Note 1: The delay, (TPWRT) releasing Reset, only occurs when the Power-up Timer is enabled, ($\overline{PWRTE}$ = 0).

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

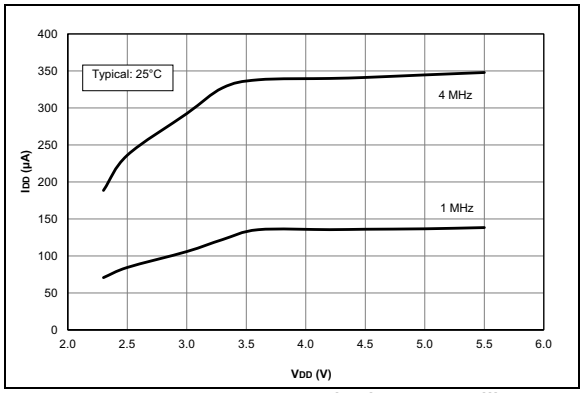


FIGURE 32-13: *IDD Typical, EC Oscillator MP Mode, PIC16F1788/9 Only.*

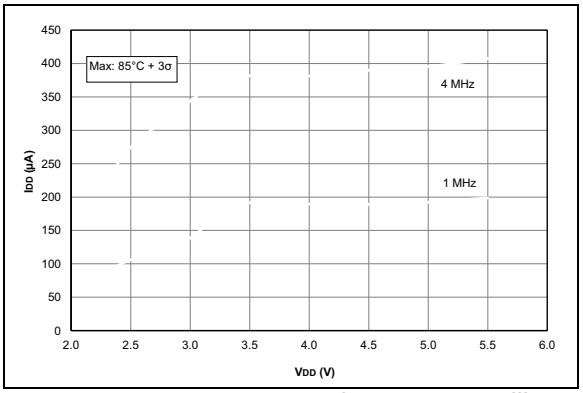


FIGURE 32-14: *IDD Maximum, EC Oscillator MP Mode, PIC16F1788/9 Only.*

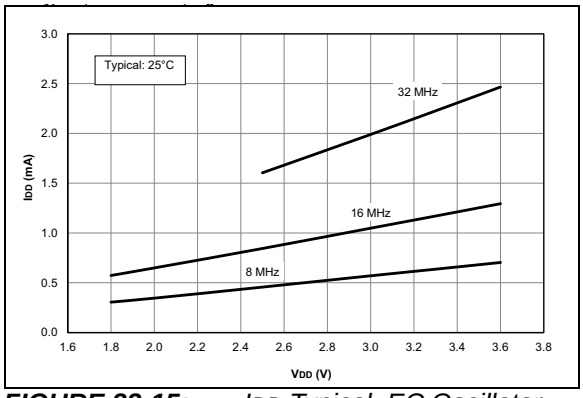


FIGURE 32-15: *IDD Typical, EC Oscillator HP Mode, PIC16LF1788/9 Only.*

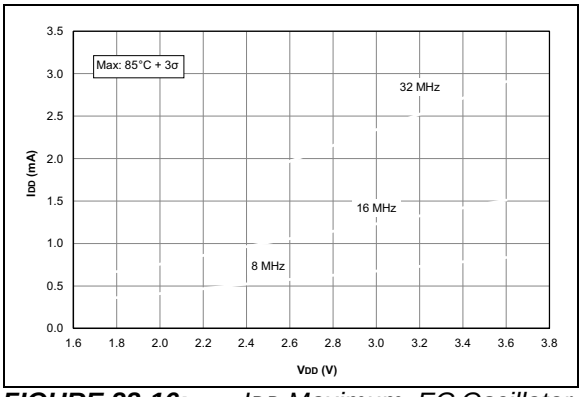


FIGURE 32-16: *IDD Maximum, EC Oscillator HP Mode, PIC16LF1788/9 Only.*

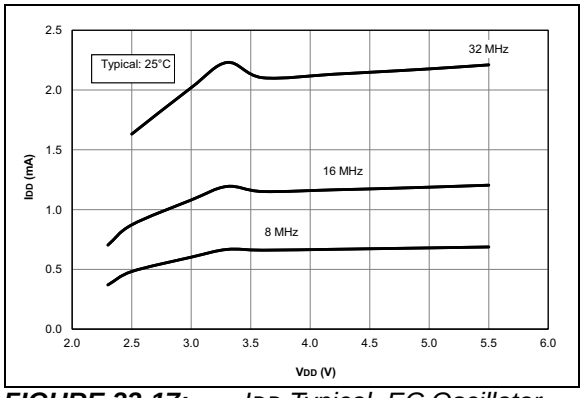


FIGURE 32-17: *IDD Typical, EC Oscillator HP Mode, PIC16F1788/9 Only.*

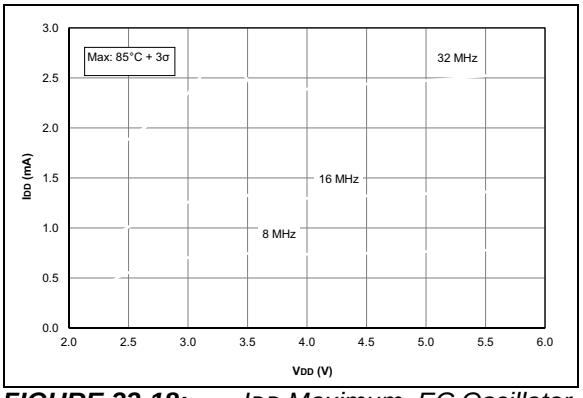


FIGURE 32-18: *IDD Maximum, EC Oscillator HP Mode, PIC16F1788/9 Only.*

33.11 Demonstration/Development Boards, Evaluation Kits, and Starter Kits

A wide variety of demonstration, development and evaluation boards for various PIC MCUs and dsPIC DSCs allows quick application development on fully functional systems. Most boards include prototyping areas for adding custom circuitry and provide application firmware and source code for examination and modification.

The boards support a variety of features, including LEDs, temperature sensors, switches, speakers, RS-232 interfaces, LCD displays, potentiometers and additional EEPROM memory.

The demonstration and development boards can be used in teaching environments, for prototyping custom circuits and for learning about various microcontroller applications.

In addition to the PICDEM™ and dsPICDEM™ demonstration/development board series of circuits, Microchip has a line of evaluation kits and demonstration software for analog filter design, KEELOQ® security ICs, CAN, IrDA®, PowerSmart battery management, SEEVAL® evaluation system, Sigma-Delta ADC, flow rate sensing, plus many more.

Also available are starter kits that contain everything needed to experience the specified device. This usually includes a single application and debug capability, all on one board.

Check the Microchip web page (www.microchip.com) for the complete list of demonstration, development and evaluation kits.

33.12 Third-Party Development Tools

Microchip also offers a great collection of tools from third-party vendors. These tools are carefully selected to offer good value and unique functionality.

- Device Programmers and Gang Programmers from companies, such as SoftLog and CCS
- Software Tools from companies, such as Gimpel and Trace Systems
- Protocol Analyzers from companies, such as Saleae and Total Phase
- Demonstration Boards from companies, such as MikroElektronika, Digilent® and Olimex
- Embedded Ethernet Solutions from companies, such as EZ Web Lynx, WIZnet and IPLogika®