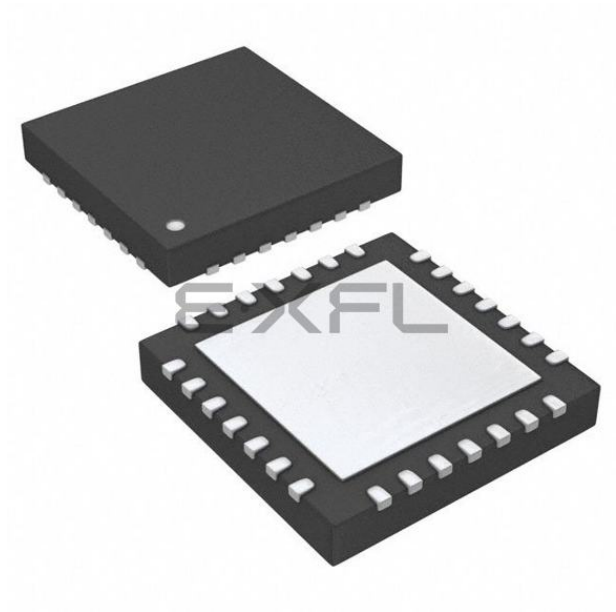

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1788-i-ml

TABLE 1-2: PIC16(L)F1788 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB4/AN11/C3IN1+/$\overline{SS}$(1)	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	C3IN1+	AN	—	Comparator C3 positive input.
	$\overline{SS}$	ST	—	Slave Select input.
RB5/AN13/C4IN2-/T1G/CCP3(1) SDO(1)/C3OUT	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	C4IN2-	AN	—	Comparator C4 negative input.
	T1G	ST	—	Timer1 gate input.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SDO	—	CMOS	SPI data output.
	C3OUT	—	CMOS	Comparator C3 output.
RB6/C4IN1+/TX(1)/CK(1)/SDI(1)/ SDA(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	C4IN1+	AN	—	Comparator C4 positive input.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C data input/output.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/DAC2OUT2/ DAC3OUT2/DAC4OUT2/RX(1)/ DT(1)/SCK(1)/SCL(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Voltage Reference output.
	DAC2OUT2	—	AN	Voltage Reference output.
	DAC3OUT2	—	AN	Voltage Reference output.
	DAC4OUT2	—	AN	Voltage Reference output.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1OSO/T1CKI/PSMC1A	RC0	TTL/ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 Oscillator Connection.
	T1CKI	ST	—	Timer1 clock input.
	PSMC1A	—	CMOS	PSMC1 output A.
RC1/T1OSI/PSMC1B/CCP2	RC1	TTL/ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 Oscillator Connection.
	PSMC1B	—	CMOS	PSMC1 output B.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/PSMC1C/PSMC3B/CCP1	RC2	TTL/ST	CMOS	General purpose I/O.
	PSMC1C	—	CMOS	PSMC1 output C.
	PSMC3B	—	CMOS	PSMC3 output B.
	CCP1	ST	CMOS	Capture/Compare/PWM1.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Pin functions can be assigned to one of two locations via software. See **Register 13-1**.
2: All pins have interrupt-on-change functionality.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29											
E80h — E90h	—	Unimplemented								—	—
E91h	PSMC1CON	PSMC1EN	PSMC1LD	P1DBFE	P1DBRE	P1MODE<3:0>				0000 0000	0000 0000
E92h	PSMC1MDL	P1MDLEN	P1MDLPOL	P1MDLBIT	—	P1MSRC<3:0>				000- 0000	000- 0000
E93h	PSMC1SYNC	P1POFST	P1PRPOL	P1DCPOL	—	—	P1SYNC<2:0>			000- -000	000- -000
E94h	PSMC1CLK	—	—	P1CPRE<1:0>		—	—	P1CSRC<1:0>		--00 --00	--00 --00
E95h	PSMC1OEN	—	—	P1OEF	P1OEE	P1OED	P1OEC	P1OEB	P1OEA	--00 0000	--00 0000
E96h	PSMC1POL	—	P1INPOL	P1POLF	P1POLE	P1POLD	P1POLC	P1POLB	P1POLA	-000 0000	-000 0000
E97h	PSMC1BLNK	—	—	P1FEBM<1:0>		—	—	P1REBM<1:0>		--00 --00	--00 --00
E98h	PSMCIREBS	P1REBSIN	—	—	P1REBSC4	P1REBSC3	P1REBSC2	P1REBSC1	—	0--0 000-	0000 000-
E99h	PSMCIFEBS	P1FEBSIN	—	—	P1FEBSC4	P1FEBSC3	P1FEBSC2	P1FEBSC1	—	0--0 000-	0000 000-
E9Ah	PSMC1PHS	P1PHSIN	—	—	P1PHSC4	P1PHSC3	P1PHSC2	P1PHSC1	P1PHST	0--0 0000	0--0 0000
E9Bh	PSMC1DCS	P1DCSIN	—	—	P1DCSC4	P1DCSC3	P1DCSC2	P1DCSC1	P1DCST	0--0 0000	0--0 0000
E9Ch	PSMC1PRS	P1PRSIN	—	—	P1PRSC4	P1PRSC3	P1PRSC2	P1PRSC1	P1PRST	0--0 0000	0--0 0000
E9Dh	PSMC1ASDC	P1ASE	P1ASDEN	P1ARSEN	—	—	—	—	P1ASDOV	000- ---0	000- ---0
E9Eh	PSMC1ASDL	—	—	P1ASDLF	P1ASDLE	P1ASDLD	P1ASDLC	P1ASDLB	P1ASDLA	--00 0000	--00 0000
E9Fh	PSMC1ASDS	P1ASDSIN	—	—	P1ASDSC4	P1ASDSC3	P1ASDSC2	P1ASDSC1	—	0--0 000-	0--0 000-
EA0h	PSMC1INT	P1TOVIE	P1TPHIE	P1TDCIE	P1TPRIE	P1TOVIF	P1TPHIF	P1TDCIF	P1TPRIF	0000 0000	0000 0000
EA1h	PSMC1PHL	Phase Low Count								0000 0000	0000 0000
EA2h	PSMC1PHH	Phase High Count								0000 0000	0000 0000
EA3h	PSMC1DCL	Duty Cycle Low Count								0000 0000	0000 0000
EA4h	PSMC1DCH	Duty Cycle High Count								0000 0000	0000 0000
EA5h	PSMC1PRL	Period Low Count								0000 0000	0000 0000
EA6h	PSMC1PRH	Period High Count								0000 0000	0000 0000
EA7h	PSMC1TMRL	Time base Low Counter								0000 0001	0000 0001
EA8h	PSMC1TMRH	Time base High Counter								0000 0000	0000 0000
EA9h	PSMC1DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
EAAh	PSMC1DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
EABh	PSMC1BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
EACh	PSMC1BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
EADh	PSMC1FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
EAEh	PSMC1STR0	—	—	P1STRF	P1STRE	P1STRD	P1STRC	P1STRB	P1STRA	--00 0001	--00 0001
EAFh	PSMC1STR1	P1SSYNC	—	—	—	—	—	P1LSMEN	P1HSMEN	0--- --00	0--- --00
EB0h	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved.
Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 30											
F0Ch — F10h	—	Unimplemented								—	—
F11h	PSMC4CON	PSMC4EN	PSMC4LD	P4DBFE	P4DBRE	P4MODE<3:0>				0000 0000	0000 0000
F12h	PSMC4MDL	P4MDLEN	P4MDLPOL	P4MDLBIT	—	P4MSRC<3:0>				000- 0000	000- 0000
F13h	PSMC4SYNC	P4POFST	P4PRPOL	P4DCPOL	—	—	P4SYNC<2:0>			000- -000	000- -000
F14h	PSMC4CLK	—	—	P4CPRE<1:0>		—	—	P4CSRC<1:0>		--00 --00	--00 --00
F15h	PSMC4OEN	—	—	—	—	—	—	P4OEB	P4OEA	---- --00	---- --00
F16h	PSMC4POL	—	P4INPOL	—	—	—	—	P4POLB	P4POLA	-0-- --00	-0-- --00
F17h	PSMC4BLNK	—	—	P4FEBM<1:0>		—	—	P4REBM<1:0>		--00 --00	--00 --00
F18h	PSMC4REBS	P4REBSIN	—	—	P4REBSC4	P4REBSC3	P4REBSC2	P4REBSC1	—	0--0 000-	0--0 000-
F19h	PSMC4FEBS	P4FEBSIN	—	—	P4FEBSC4	P4FEBSC3	P4FEBSC2	P4FEBSC1	—	0--0 000-	0--0 000-
F1Ah	PSMC4PHS	P4PHSIN	—	—	P4PHSC4	P4PHSC3	P4PHSC2	P4PHSC1	P4PHST	0--0 0000	0--0 0000
F1Bh	PSMC4DCS	P4DCSIN	—	—	P4DCSC4	P4DCSC3	P4DCSC2	P4DCSC1	P4DCST	0--0 0000	0--0 0000
F1Ch	PSMC4PRS	P4PRSIN	—	—	P4PRSC4	P4PRSC3	P4PRSC2	P4PRSC1	P4PRST	0--0 0000	0--0 0000
F1Dh	PSMC4ASDC	P4ASE	P4ASDEN	P4ARSEN	—	—	—	—	P4ASDOV	000- ---0	000- ---0
F1Eh	PSMC4ASDL	—	—	—	—	—	—	P4ASDLB	P4ASDLA	---- --00	---- --00
F1Fh	PSMC4ASDS	P4ASDSIN	—	—	P4ASDSC4	P4ASDSC3	P4ASDSC2	P4ASDSC1	—	0--0 000-	0--0 000-
F20h	PSMC4INT	P4TOVIE	P4TPHIE	P4TDCIE	P4TPRIE	P4TOVIF	P4TPHIF	P4TDCIF	P4TPRIF	0000 0000	0000 0000
F21h	PSMC4PHL	Phase Low Count								0000 0000	0000 0000
F22h	PSMC4PHH	Phase High Count								0000 0000	0000 0000
F23h	PSMC4DCL	Duty Cycle Low Count								0000 0000	0000 0000
F24h	PSMC4DCH	Duty Cycle High Count								0000 0000	0000 0000
F25h	PSMC4PRL	Period Low Count								0000 0000	0000 0000
F26h	PSMC4PRH	Period High Count								0000 0000	0000 0000
F27h	PSMC4TMRL	Time base Low Counter								0000 0001	0000 0001
F28h	PSMC4TMRH	Time base High Counter								0000 0000	0000 0000
F29h	PSMC4DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
F2Ah	PSMC4DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
F2Bh	PSMC4BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
F2Ch	PSMC4BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
F2Dh	PSMC4FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
F2Eh	PSMC4STR0	—	—	—	—	—	—	P4STRB	P4STRA	---- --01	---- --01
F2Fh	PSMC4STR1	P4SSYNC	—	—	—	—	—	P4LSMEN	P4HSMEN	0--- --00	0--- --00

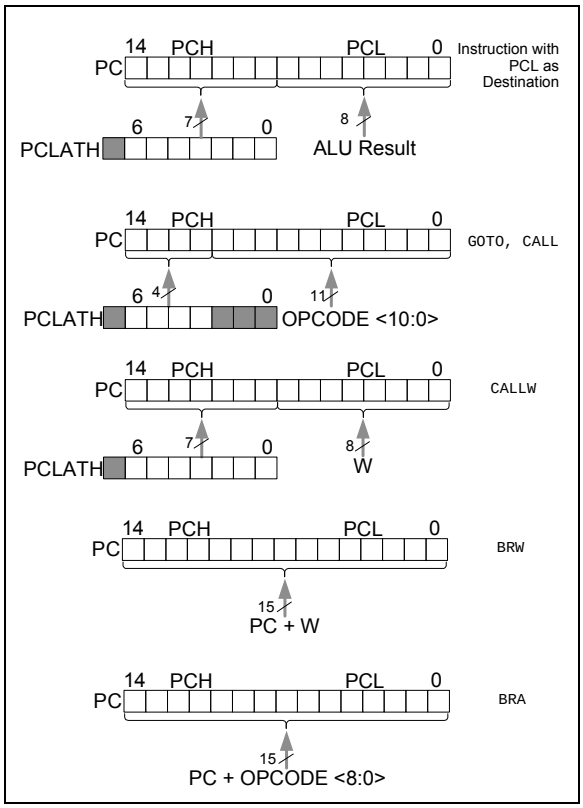
Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

3.4 PCL and PCLATH

The Program Counter (PC) is 15 bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte (PC<14:8>) is not directly readable or writable and comes from PCLATH. On any Reset, the PC is cleared. Figure 3-3 shows the five situations for the loading of the PC.

FIGURE 3-3: LOADING OF PC IN DIFFERENT SITUATIONS



3.4.1 MODIFYING PCL

Executing any instruction with the PCL register as the destination simultaneously causes the Program Counter PC<14:8> bits (PCH) to be replaced by the contents of the PCLATH register. This allows the entire contents of the program counter to be changed by writing the desired upper seven bits to the PCLATH register. When the lower eight bits are written to the PCL register, all 15 bits of the program counter will change to the values contained in the PCLATH register and those being written to the PCL register.

3.4.2 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to Application Note AN556, *"Implementing a Table Read"* (DS00556).

3.4.3 COMPUTED FUNCTION CALLS

A computed function CALL allows programs to maintain tables of functions and provide another way to execute state machines or look-up tables. When performing a table read using a computed function CALL, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block).

If using the CALL instruction, the PCH<2:0> and PCL registers are loaded with the operand of the CALL instruction. PCH<6:3> is loaded with PCLATH<6:3>.

The CALLW instruction enables computed calls by combining PCLATH and W to form the destination address. A computed CALLW is accomplished by loading the W register with the desired address and executing CALLW. The PCL register is loaded with the value of W and PCH is loaded with PCLATH.

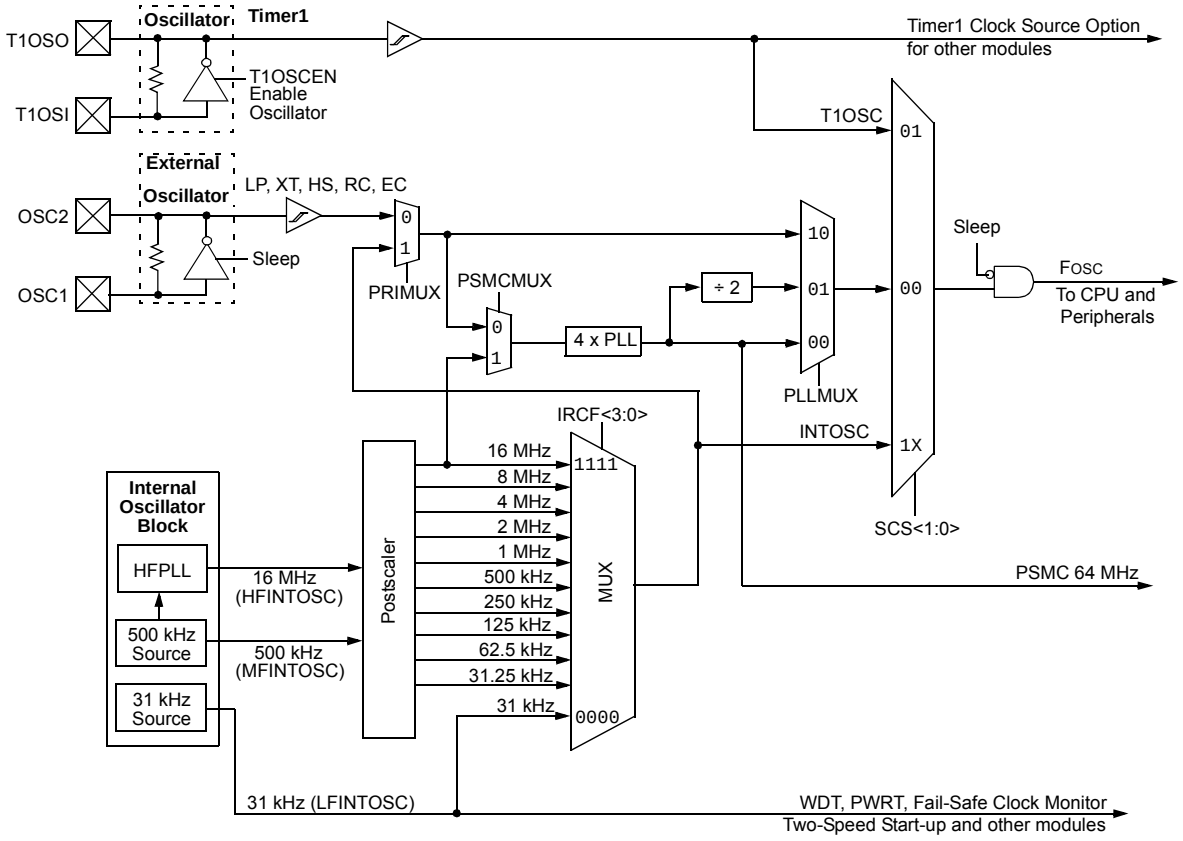
3.4.4 BRANCHING

The branching instructions add an offset to the PC. This allows relocatable code and code that crosses page boundaries. There are two forms of branching, BRW and BRA. The PC will have incremented to fetch the next instruction in both cases. When using either branching instruction, a PCL memory boundary may be crossed.

If using BRW, load the W register with the desired unsigned address and execute BRW. The entire PC will be loaded with the address PC + 1 + W.

If using BRA, the entire PC will be loaded with PC + 1 +, the signed value of the operand of the BRA instruction.

FIGURE 6-1: SIMPLIFIED PIC® MCU CLOCK SOURCE BLOCK DIAGRAM



SCS	FOSC<2:0>	PLLEN or SPLLEN	PRIMUX	PSMCMUX	PLLMUX
=00	=100	0	1	1	10
		1	1	1	01
	≠100	0	0	1	10
		1(1)	0	0	00
≠00	XXX	X	X	1	XX

Note 1: This selection should not be made when the PSMC is using the 64 MHz clock option.

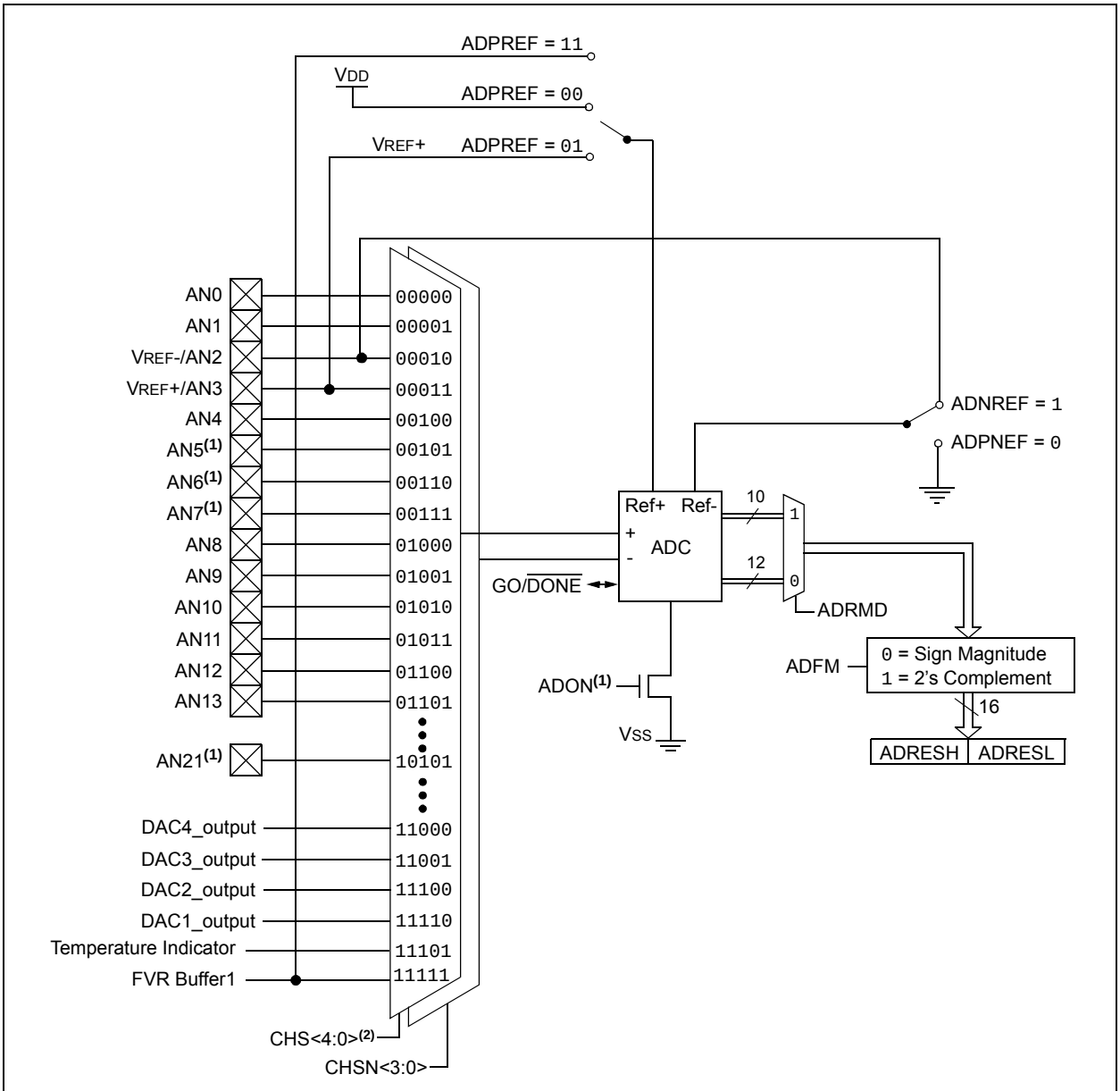
17.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

The Analog-to-Digital Converter (ADC) allows conversion of a single-ended and differential analog input signals to a 12-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 12-bit binary result via successive approximation and stores the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 17-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

FIGURE 17-1: ADC BLOCK DIAGRAM



Note 1: When ADON = 0, all multiplexer inputs are disconnected. PIC16(L)F1789 only.

2: See ADCON0 register (Register 17-1) and ADCON2 register (Register 17-3) for detailed analog channel selection per device.

23.6.2 TIMER1 GATE SOURCE SELECTION

Timer1 gate source selections are shown in Table 23-4. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

TABLE 23-4: TIMER1 GATE SOURCES

T1GSS	Timer1 Gate Source
00	Timer1 Gate Pin
01	Overflow of Timer0 (TMR0 increments from FFh to 00h)
10	Comparator 1 Output sync_C1OUT (optionally Timer1 synchronized output)
11	Comparator 2 Output sync_C2OUT (optionally Timer1 synchronized output)

23.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

23.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

23.6.2.3 Comparator C1 Gate Operation

The output resulting from a Comparator 1 operation can be selected as a source for Timer1 gate control. The Comparator 1 output (sync_C1OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see **Section 21.4.1 "Comparator Output Synchronization"**.

23.6.2.4 Comparator C2 Gate Operation

The output resulting from a Comparator 2 operation can be selected as a source for Timer1 gate control. The Comparator 2 output (sync_C2OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see **Section 21.4.1 "Comparator Output Synchronization"**.

23.6.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 23-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

Note:	Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

23.6.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1 Gate Single-Pulse mode is enabled by first setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/$\overline{\text{DONE}}$ bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/$\overline{\text{DONE}}$ bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/$\overline{\text{DONE}}$ bit is once again set in software. See Figure 23-5 for timing details.

If the Single-Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/$\overline{\text{DONE}}$ bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 23-6 for timing details.

23.6.5 TIMER1 GATE VALUE

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is accessible by reading the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

23.6.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

23.7 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit of the PIR1 register is set. To enable the interrupt on rollover, you must set these bits:

- TMR1ON bit of the T1CON register
- TMR1IE bit of the PIE1 register
- PEIE bit of the INTCON register
- GIE bit of the INTCON register

The interrupt is cleared by clearing the TMR1IF bit in the Interrupt Service Routine.

Note:	The TMR1H:TMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

23.8 Timer1 Operation During Sleep

Timer1 can only operate during Sleep when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To set up the timer to wake the device:

- TMR1ON bit of the T1CON register must be set
- TMR1IE bit of the PIE1 register must be set
- PEIE bit of the INTCON register must be set
- $\overline{\text{T1SYNC}}$ bit of the T1CON register must be set
- TMR1CS bits of the T1CON register must be configured
- T1OSCEN bit of the T1CON register must be configured

The device will wake-up on an overflow and execute the next instructions. If the GIE bit of the INTCON register is set, the device will call the Interrupt Service Routine.

Timer1 oscillator will continue to operate in Sleep regardless of the $\overline{\text{T1SYNC}}$ bit setting.

23.9 CCP Capture/Compare Time Base

The CCP modules use the TMR1H:TMR1L register pair as the time base when operating in Capture or Compare mode.

In Capture mode, the value in the TMR1H:TMR1L register pair is copied into the CCPR1H:CCPR1L register pair on a configured event.

In Compare mode, an event is triggered when the value CCPR1H:CCPR1L register pair matches the value in the TMR1H:TMR1L register pair. This event can be a Auto-conversion Trigger.

For more information, see **Section 25.0 "Capture/Compare/PWM Modules"**.

23.10 CCP Auto-Conversion Trigger

When any of the CCP's are configured to trigger a auto-conversion, the trigger will clear the TMR1H:TMR1L register pair. This auto-conversion does not cause a Timer1 interrupt. The CCP module may still be configured to generate a CCP interrupt.

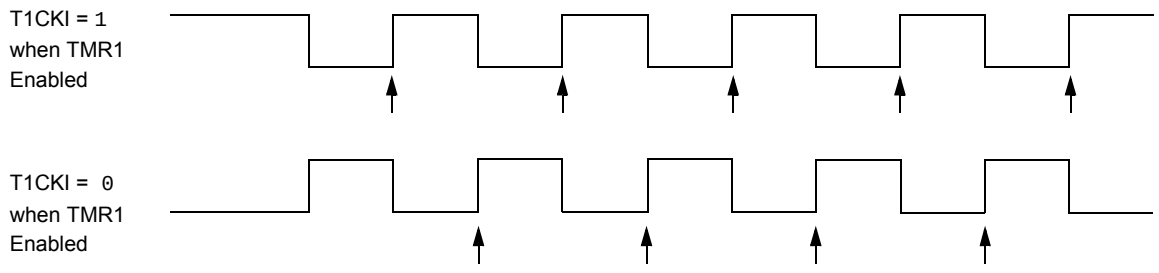
In this mode of operation, the CCPR1H:CCPR1L register pair becomes the period register for Timer1.

Timer1 should be synchronized and FOSC/4 should be selected as the clock source in order to utilize the Auto-conversion Trigger. Asynchronous operation of Timer1 can cause a Auto-conversion Trigger to be missed.

In the event that a write to TMR1H or TMR1L coincides with a Auto-conversion Trigger from the CCP, the write will take precedence.

For more information, see **Section 25.2.4 "Auto-Conversion Trigger"**.

FIGURE 23-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

TABLE 23-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	143
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				231
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				231
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								209*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								209*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	142
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	147
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	217
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		218

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

* Page provides register information.

TABLE 24-1: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER2

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				231
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
PR2	Timer2 Module Period Register								220*
T2CON	—	T2OUTPS<3:0>				TMR2ON	T2CKPS<1:0>		222
TMR2	Holding Register for the 8-bit TMR2 Register								220*

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for Timer2 module.

* Page provides register information.

REGISTER 26-3: PSMC1SYNC: PSMC1 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P1POFST	P1PRPOL	P1DCPOL	—	—	P1SYNC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P1POFST:** PSMC1 Phase Offset Control bit
- 1 = sync_out source is phase event and latch set source is synchronous period event
- 0 = sync_out source is period event and latch set source is phase event

bit 6 **P1PRPOL:** PSMC1 Period Polarity Event Control bit
- 1 = Selected asynchronous period event inputs are inverted
- 0 = Selected asynchronous period event inputs are not inverted

bit 5 **P1DCPOL:** PSMC1 Duty-cycle Event Polarity Control bit
- 1 = Selected asynchronous duty-cycle event inputs are inverted
- 0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **P1SYNC<2:0>:** PSMC1 Period Synchronization Mode bits
- 1xx = Reserved - Do not use
- 100 = PSMC1 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)
- 011 = PSMC1 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
- 010 = PSMC1 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)
- 001 = PSMC1 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)
- 000 = PSMC1 is synchronized with period event

REGISTER 26-4: PSMC2SYNC: PSMC2 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P2POFST	P2PRPOL	P2DCPOL	—	—	P2SYNC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P2POFST:** PSMC2 Phase Offset Control bit
- 1 = sync_out source is phase event and latch set source is synchronous period event
- 0 = sync_out source is period event and latch set source is phase event

bit 6 **P2PRPOL:** PSMC2 Period Polarity Event Control bit
- 1 = Selected asynchronous period event inputs are inverted
- 0 = Selected asynchronous period event inputs are not inverted

bit 5 **P2DCPOL:** PSMC2 Duty-cycle Event Polarity Control bit
- 1 = Selected asynchronous duty-cycle event inputs are inverted
- 0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **P2SYNC<2:0>:** PSMC2 Period Synchronization Mode bits
- 1xx = Reserved - Do not use
- 100 = PSMC2 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)
- 011 = PSMC2 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
- 010 = PSMC2 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)
- 001 = PSMC2 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)
- 000 = PSMC2 is synchronized with period event

28.1.2 EUSART ASYNCHRONOUS RECEIVER

The Asynchronous mode is typically used in RS-232 systems. The receiver block diagram is shown in Figure 28-2. The data is received on the RX/DT pin and drives the data recovery block. The data recovery block is actually a high-speed shifter operating at 16 times the baud rate, whereas the serial Receive Shift Register (RSR) operates at the bit rate. When all eight or nine bits of the character have been shifted in, they are immediately transferred to a two character First-In-First-Out (FIFO) memory. The FIFO buffering allows reception of two complete characters and the start of a third character before software must start servicing the EUSART receiver. The FIFO and RSR registers are not directly accessible by software. Access to the received data is via the RCREG register.

28.1.2.1 Enabling the Receiver

The EUSART receiver is enabled for asynchronous operation by configuring the following three control bits:

- CREN = 1
- SYNC = 0
- SPEN = 1

All other EUSART control bits are assumed to be in their default state.

Setting the CREN bit of the RCSTA register enables the receiver circuitry of the EUSART. Clearing the SYNC bit of the TXSTA register configures the EUSART for asynchronous operation. Setting the SPEN bit of the RCSTA register enables the EUSART. The programmer must set the corresponding TRIS bit to configure the RX/DT I/O pin as an input.

Note:	If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

28.1.2.2 Receiving Data

The receiver data recovery circuit initiates character reception on the falling edge of the first bit. The first bit, also known as the Start bit, is always a zero. The data recovery circuit counts one-half bit time to the center of the Start bit and verifies that the bit is still a zero. If it is not a zero then the data recovery circuit aborts character reception, without generating an error, and resumes looking for the falling edge of the Start bit. If the Start bit zero verification succeeds then the data recovery circuit counts a full bit time to the center of the next bit. The bit is then sampled by a majority detect circuit and the resulting '0' or '1' is shifted into the RSR. This repeats until all data bits have been sampled and shifted into the RSR. One final bit time is measured and the level sampled. This is the Stop bit, which is always a '1'. If the data recovery circuit samples a '0' in the Stop bit position then a framing error is set for this character, otherwise the framing error is cleared for this character. See **Section 28.1.2.4 "Receive Framing Error"** for more information on framing errors.

Immediately after all data bits and the Stop bit have been received, the character in the RSR is transferred to the EUSART receive FIFO and the RCIF interrupt flag bit of the PIR1 register is set. The top character in the FIFO is transferred out of the FIFO by reading the RCREG register.

Note:	If the receive FIFO is overrun, no additional characters will be received until the overrun condition is cleared. See **Section 28.1.2.5 "Receive Overrun Error"** for more information on overrun errors.

28.1.2.3 Receive Interrupts

The RCIF interrupt flag bit of the PIR1 register is set whenever the EUSART receiver is enabled and there is an unread character in the receive FIFO. The RCIF interrupt flag bit is read-only, it cannot be set or cleared by software.

RCIF interrupts are enabled by setting all of the following bits:

- RCIE, Interrupt Enable bit of the PIE1 register
- PEIE, Peripheral Interrupt Enable bit of the INTCON register
- GIE, Global Interrupt Enable bit of the INTCON register

The RCIF interrupt flag bit will be set when there is an unread character in the FIFO, regardless of the state of interrupt enable bits.

RETURN **Return from Subroutine**

Syntax: [*label*] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

RLF **Rotate Left f through Carry**

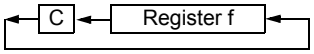
Syntax: [*label*] RLF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example:

```
RLF     REG1,0
```

Before Instruction

```
REG1    =   1110
0110
C       =   0
```

After Instruction

```
REG1    =   1110
0110
W       =   1100
1100
C       =   1
```

RRF **Rotate Right f through Carry**

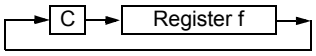
Syntax: [*label*] RRF f,d

Operands: $0 \le f \le 127$
$d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



SLEEP **Enter Sleep mode**

Syntax: [*label*] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{TO}$,
0 → $\overline{PD}$

Status Affected: $\overline{TO}$, $\overline{PD}$

Description: The power-down Status bit, $\overline{PD}$ is cleared. Time-out Status bit, $\overline{TO}$ is set. Watchdog Timer and its prescaler are cleared.
The processor is put into Sleep mode with the oscillator stopped.

SUBLW **Subtract W from literal**

Syntax: [*label*] SUBLW k

Operands: $0 \le k \le 255$

Operation: k - (W) → (W)

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	W > k
C = 1	W ≤ k
DC = 0	W<3:0> > k<3:0>
DC = 1	W<3:0> ≤ k<3:0>

FIGURE 31-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

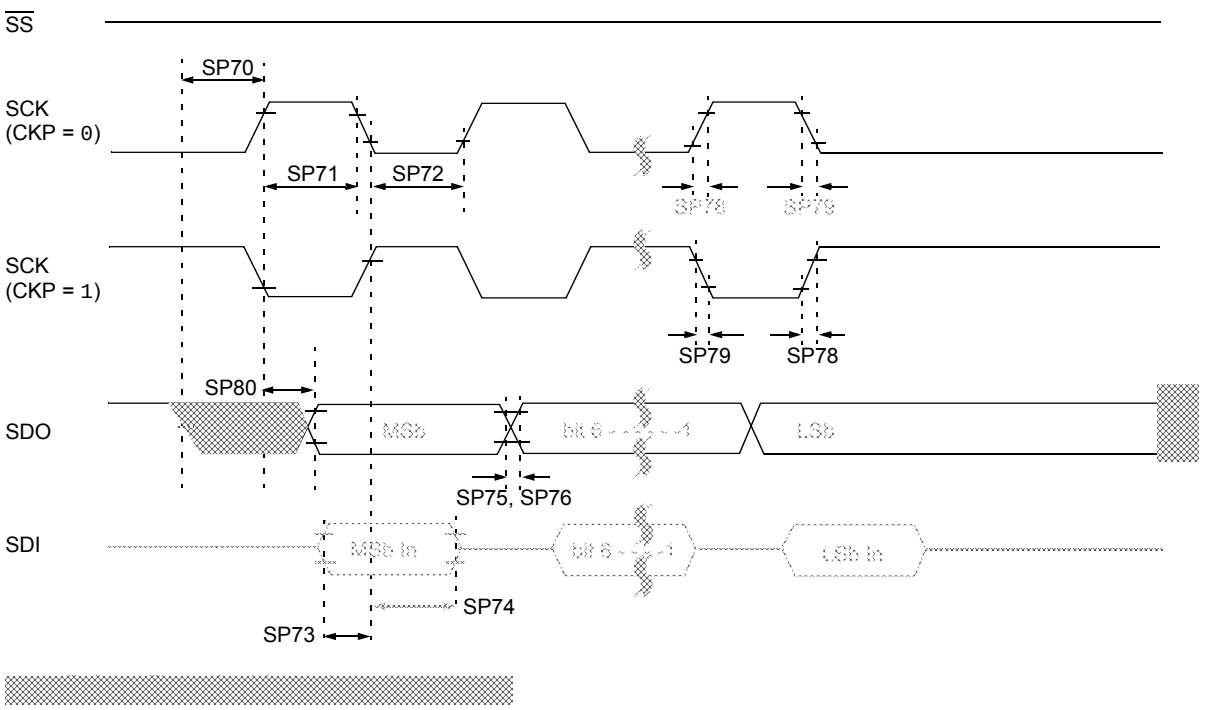
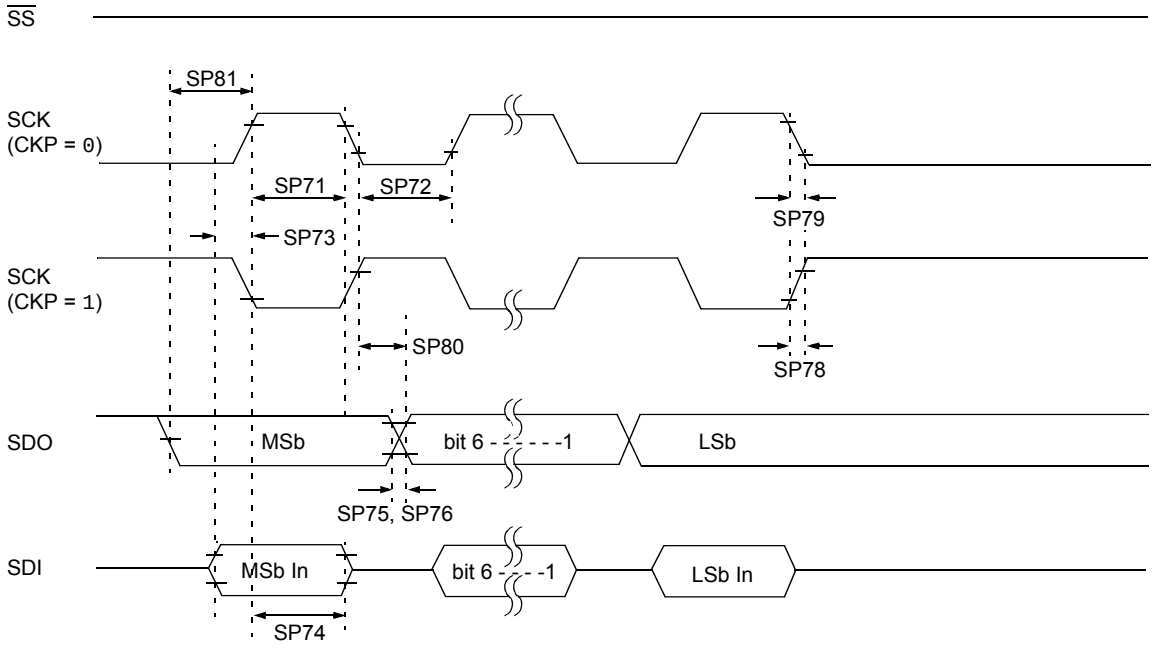


FIGURE 31-17: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



Note: Refer to Figure 31-4 for load conditions.

32.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

Unless otherwise noted, all graphs apply to both the F and LF devices.

Note:	The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

"Typical" represents the mean of the distribution at 25°C. "Maximum", "Max.", "Minimum" or "Min." represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

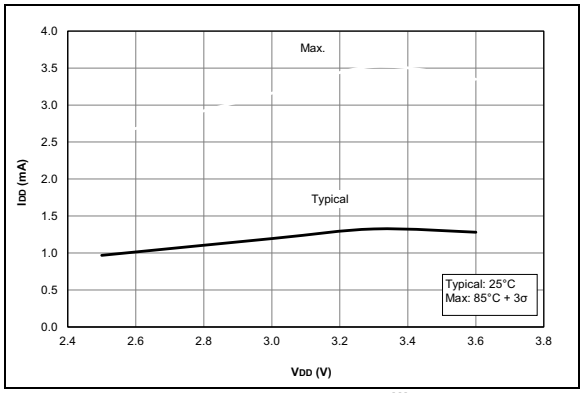


FIGURE 32-31: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16LF1788/9 Only.*

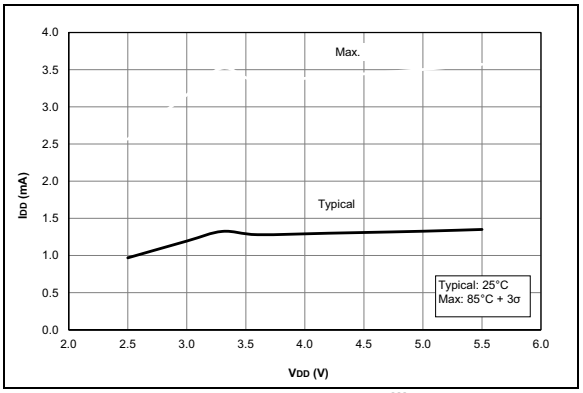


FIGURE 32-32: *IDD, HS Oscillator, 32 MHz (8 MHz + 4x PLL), PIC16F1788/9 Only.*

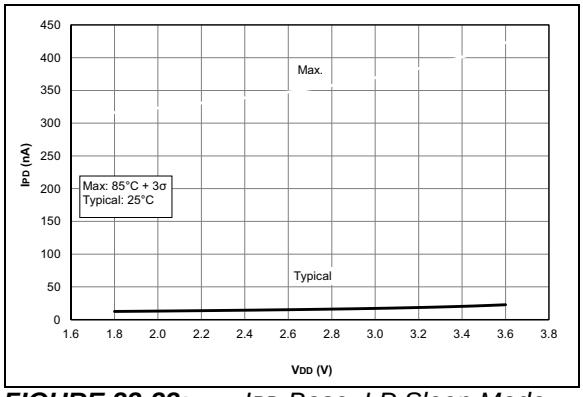


FIGURE 32-33: *IPD Base, LP Sleep Mode, PIC16LF1788/9 Only.*

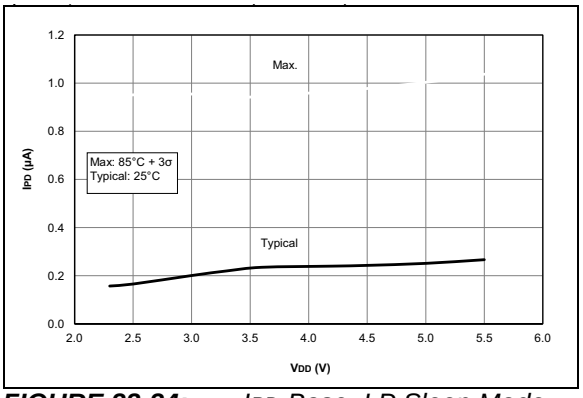


FIGURE 32-34: *IPD Base, LP Sleep Mode (VREGPM = 1), PIC16F1788/9 Only.*

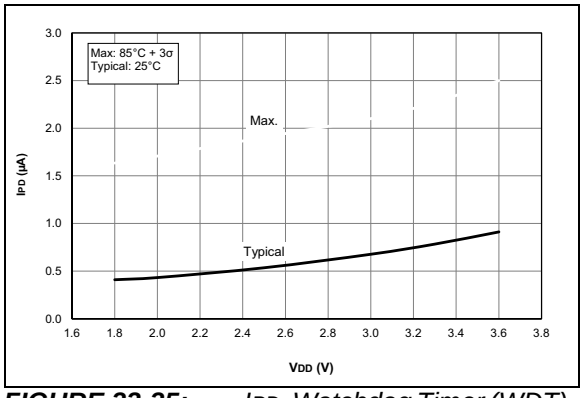


FIGURE 32-35: *IPD, Watchdog Timer (WDT), PIC16LF1788/9 Only.*

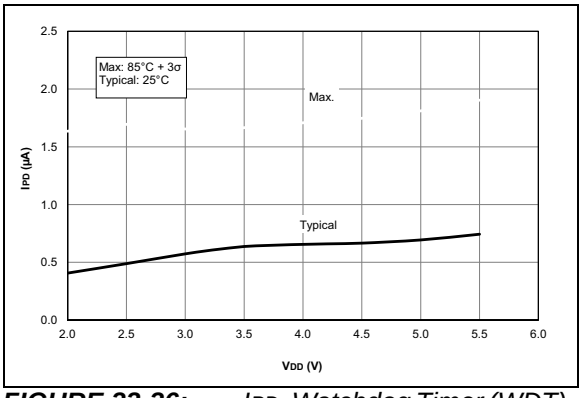


FIGURE 32-36: *IPD, Watchdog Timer (WDT), PIC16F1788/9 Only.*

Note: Unless otherwise noted, VIN = 5V, FOSC = 300 kHz, CIN = 0.1 µF, TA = 25°C.

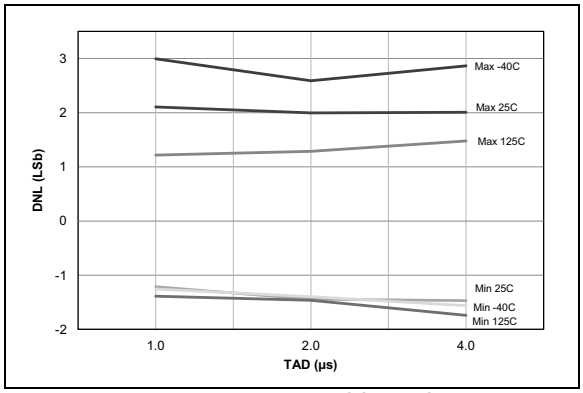


FIGURE 32-97: *ADC 12-bit Mode, Single-Ended DNL, VDD = 5.5V, VREF = 5.5V.*

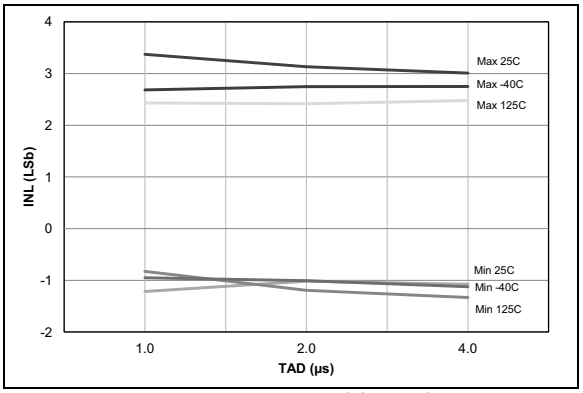


FIGURE 32-98: *ADC 12-bit Mode, Single-Ended INL, VDD = 5.5V, VREF = 5.5V.*

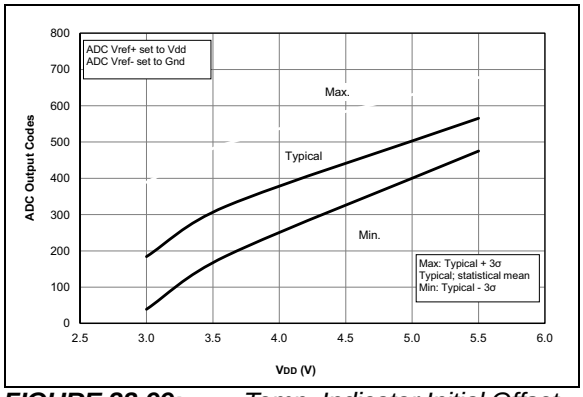


FIGURE 32-99: *Temp. Indicator Initial Offset, High Range, Temp. = 20°C, PIC16F1788/9 Only.*

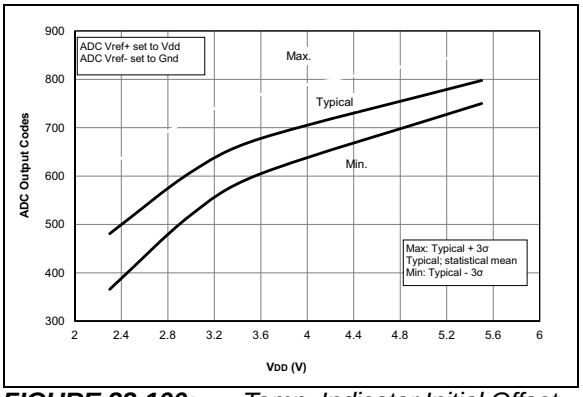


FIGURE 32-100: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16F1788/9 Only.*

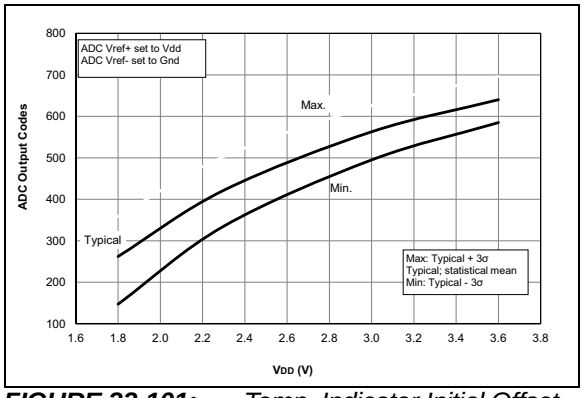


FIGURE 32-101: *Temp. Indicator Initial Offset, Low Range, Temp. = 20°C, PIC16LF1788/9 Only.*

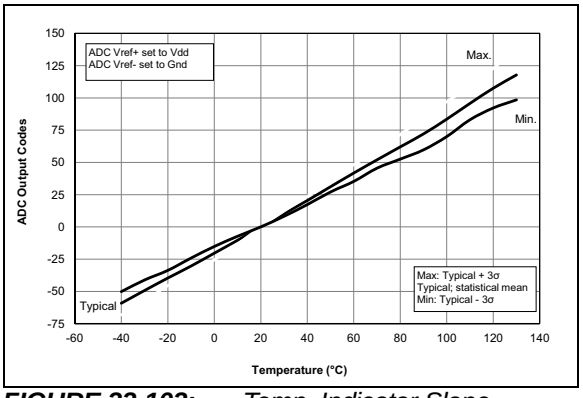
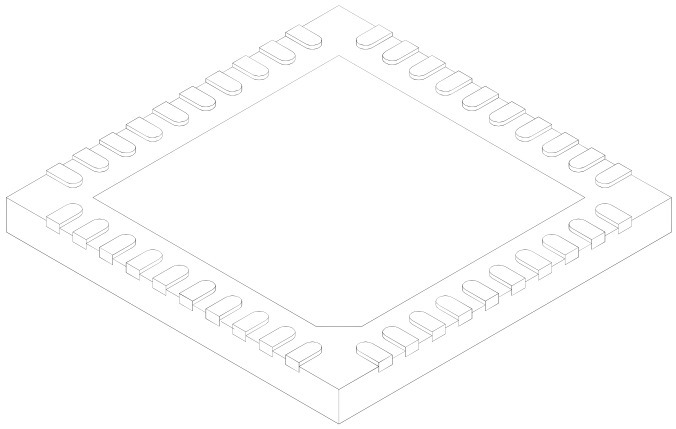


FIGURE 32-102: *Temp. Indicator Slope Normalized to 20°C, High Range, VDD = 5.5V, PIC16F1788/9 Only.*

40-Lead Ultra Thin Plastic Quad Flat, No Lead Package (MV) – 5x5x0.5 mm Body [UQFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		40	
Pitch	e		0.40 BSC	
Overall Height	A	0.45	0.50	0.55
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.127 REF	
Overall Width	E		5.00 BSC	
Exposed Pad Width	E2	3.60	3.70	3.80
Overall Length	D		5.00 BSC	
Exposed Pad Length	D2	3.60	3.70	3.80
Contact Width	b	0.15	0.20	0.25
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated.
3. Dimensioning and tolerancing per ASME Y14.5M.

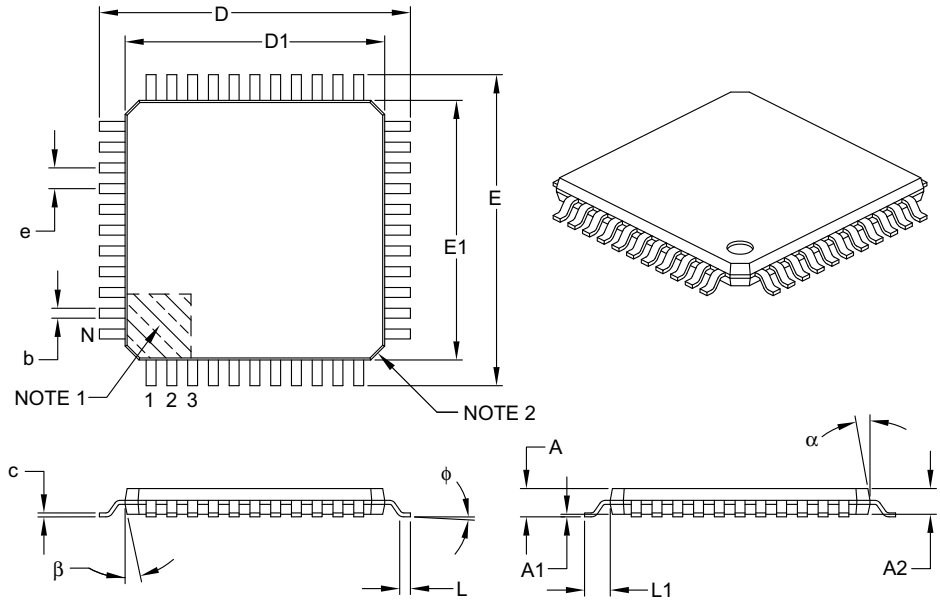
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-156A Sheet 2 of 2

44-Lead Plastic Thin Quad Flatpack (PT) – 10x10x1 mm Body, 2.00 mm [TQFP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Leads	N		44	
Lead Pitch	e		0.80 BSC	
Overall Height	A	–	–	1.20
Molded Package Thickness	A2	0.95	1.00	1.05
Standoff	A1	0.05	–	0.15
Foot Length	L	0.45	0.60	0.75
Footprint	L1		1.00 REF	
Foot Angle	φ	0°	3.5°	7°
Overall Width	E		12.00 BSC	
Overall Length	D		12.00 BSC	
Molded Package Width	E1		10.00 BSC	
Molded Package Length	D1		10.00 BSC	
Lead Thickness	c	0.09	–	0.20
Lead Width	b	0.30	0.37	0.45
Mold Draft Angle Top	α	11°	12°	13°
Mold Draft Angle Bottom	β	11°	12°	13°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Chamfers at corners are optional; size may vary.
3. Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-076B

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	[X](1)	-	X	/XX	XXX
Device	Tape and Reel Option		Temperature Range	Package	Pattern

Device:	PIC16F1788, PIC16LF1788, PIC16F1789, PIC16LF1789	
Tape and Reel Option:	Blank T	= Standard packaging (tube or tray) = Tape and Reel(1)
Temperature Range:	I E	= -40°C to +85°C (Industrial) = -40°C to +125°C (Extended)
Package:(2)	ML MV P PT SP SO SS	= QFN = UQFN = PDIP = TQFP = SPDIP = SOIC = SSOP
Pattern:	QTP, SQTP, Code or Special Requirements (blank otherwise)	

Examples:

a) PIC16LF1788- I/P
Industrial temperature
PDIP package

b) PIC16F1789- E/SS
Extended temperature,
SSOP package

Note 1: Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package. Check with your Microchip Sales Office for package availability with the Tape and Reel option.

2: Small form-factor packaging options may be available. Please check www.microchip.com/packaging for small-form factor package availability, or contact your local Sales Office.