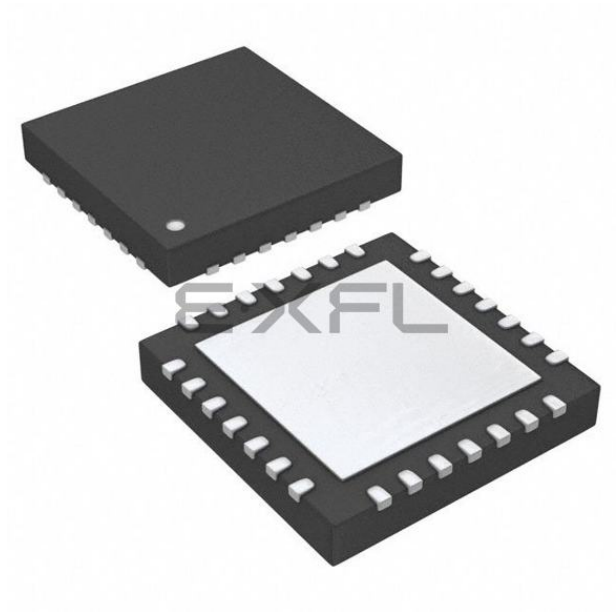

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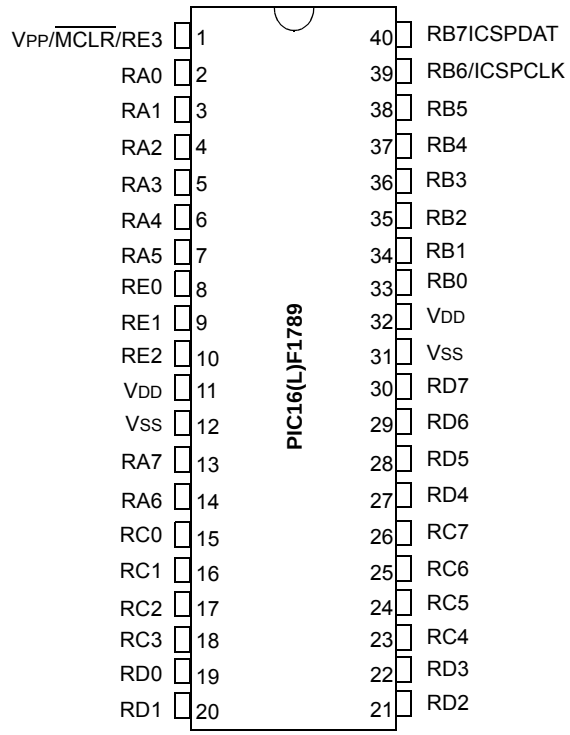
Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 11x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1788t-i-ml

Pin Diagram – 40-Pin PDIP



Note: See Table 2 for the location of all peripheral functions.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29 (Continued)											
ED1h	PSMC3CON	PSMC3EN	PSMC3LD	P3DBFE	P3DBRE	P3MODE<3:0>				0000 0000	0000 0000
ED2h	PSMC3MDL	P3MDLEN	P3MDLPOL	P3MDLBIT	—	P3MSRC<3:0>				000- 0000	000- 0000
ED3h	PSMC3SYNC	P3POFST	P3PRPOL	P3DCPOL	—	—	P3SYNC<2:0>			000- -000	000- -000
ED4h	PSMC3CLK	—	—	P3CPRE<1:0>		—	—	P3CSRC<1:0>		--00 --00	--00 --00
ED5h	PSMC3OEN	—	—	—	—	—	—	P3OEB	P3OEA	---- --00	---- --00
ED6h	PSMC3POL	—	P3INPOL	—	—	—	—	P3POLB	P3POLA	-0-- --00	-0-- --00
ED7h	PSMC3BLNK	—	—	P3FEBM<1:0>		—	—	P3REBM<1:0>		--00 --00	--00 --00
ED8h	PSMC3REBS	P3REBSIN	—	—	P3REBSC4	P3REBSC3	P3REBSC2	P3REBSC1	—	0--0 000-	0--0 000-
ED9h	PSMC3FEBS	P3FEBSIN	—	—	P3FEBSC4	P3FEBSC3	P3FEBSC2	P3FEBSC1	—	0--0 000-	0--0 000-
EDAh	PSMC3PHS	P3PHSIN	—	—	P3PHSC4	P3PHSC3	P3PHSC2	P3PHSC1	P3PHST	0--0 0000	0--0 0000
EDBh	PSMC3DCS	P3DCSIN	—	—	P3DCSC4	P3DCSC3	P3DCSC2	P3DCSC1	P3DCST	0--0 0000	0--0 0000
EDCh	PSMC3PRS	P3PRSIN	—	—	P3PRSC4	P3PRSC3	P3PRSC2	P3PRSC1	P3PRST	0--0 0000	0--0 0000
EDDh	PSMC3ASDC	P3ASE	P3ASDEN	P3ARSEN	—	—	—	—	P3ASDOV	000- ---0	000- ---0
EDEh	PSMC3ASDL	—	—	—	—	—	—	P3ASDLB	P3ASDLA	---- --00	---- --00
EDFh	PSMC3ASDS	P3ASDSIN	—	—	P3ASDSC4	P3ASDSC3	P3ASDSC2	P3ASDSC1	—	0--0 000-	0--0 000-
EE0h	PSMC3INT	P3TOVIE	P3TPHIE	P3TDCIE	P3TPRIE	P3TOVIF	P3TPHIF	P3TDCIF	P3TPRIF	0000 0000	0000 0000
EE1h	PSMC3PHL	Phase Low Count								0000 0000	0000 0000
EE2h	PSMC3PHH	Phase High Count								0000 0000	0000 0000
EE3h	PSMC3DCL	Duty Cycle Low Count								0000 0000	0000 0000
EE4h	PSMC3DCH	Duty Cycle High Count								0000 0000	0000 0000
EE5h	PSMC3PRL	Period Low Count								0000 0000	0000 0000
EE6h	PSMC3PRH	Period High Count								0000 0000	0000 0000
EE7h	PSMC3TMRL	Time base Low Counter								0000 0001	0000 0001
EE8h	PSMC3TMRH	Time base High Counter								0000 0000	0000 0000
EE9h	PSMC3DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
EEAh	PSMC3DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
EEBh	PSMC3BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
EECh	PSMC3BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
EEDh	PSMC3FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
EEEh	PSMC3STR0	—	—	—	—	—	—	P3STRB	P3STRA	---- --01	---- --01
EEFh	PSMC3STR1	P3SSYNC	—	—	—	—	—	P3LSMEN	P3HSMEN	0--- --00	0--- --00

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

4.3 Code Protection

Code protection allows the device to be protected from unauthorized access. Program memory protection and data EEPROM protection are controlled independently. Internal access to the program memory and data EEPROM are unaffected by any code protection setting.

4.3.1 PROGRAM MEMORY PROTECTION

The entire program memory space is protected from external reads and writes by the $\overline{CP}$ bit in Configuration Words. When $\overline{CP}$ = 0, external reads and writes of program memory are inhibited and a read will return all '0's. The CPU can continue to read program memory, regardless of the protection bit settings. Writing the program memory is dependent upon the write protection setting. See **Section 4.4 "Write Protection"** for more information.

4.3.2 DATA EEPROM PROTECTION

The entire data EEPROM is protected from external reads and writes by the $\overline{CPD}$ bit. When $\overline{CPD}$ = 0, external reads and writes of data EEPROM are inhibited. The CPU can continue to read and write data EEPROM regardless of the protection bit settings.

4.4 Write Protection

Write protection allows the device to be protected from unintended self-writes. Applications, such as bootloader software, can be protected while allowing other regions of the program memory to be modified.

The WRT<1:0> bits in Configuration Words define the size of the program memory block that is protected.

4.5 User ID

Four memory locations (8000h-8003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are readable and writable during normal execution. See **Section 12.5 "User ID, Device ID and Configuration Word Access"**for more information on accessing these memory locations. For more information on checksum calculation, see the *"PIC16(L)F178X Memory Programming Specification"* (DS41457).

6.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with both external and internal clock sources to provide a system clock source. The input frequency for the 4x PLL must fall within specifications. See the PLL Clock Timing Specifications in **Section 30.0 "Electrical Specifications"**.

The 4x PLL may be enabled for use by one of two methods:

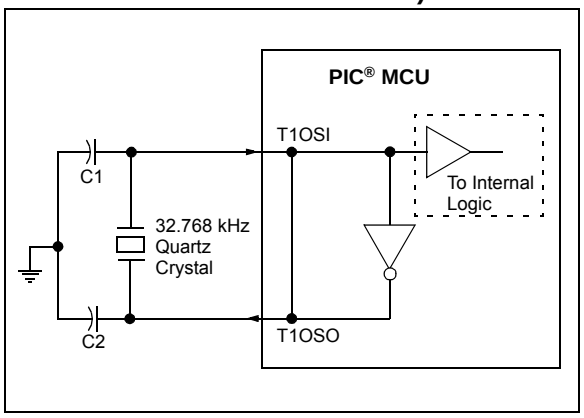
1. Program the PLLEN bit in Configuration Words to a '1'.
2. Write the SPLLEN bit in the OSCCON register to a '1'. If the PLLEN bit in Configuration Words is programmed to a '1', then the value of SPLLEN is ignored.

6.2.1.5 TIMER1 Oscillator

The Timer1 oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

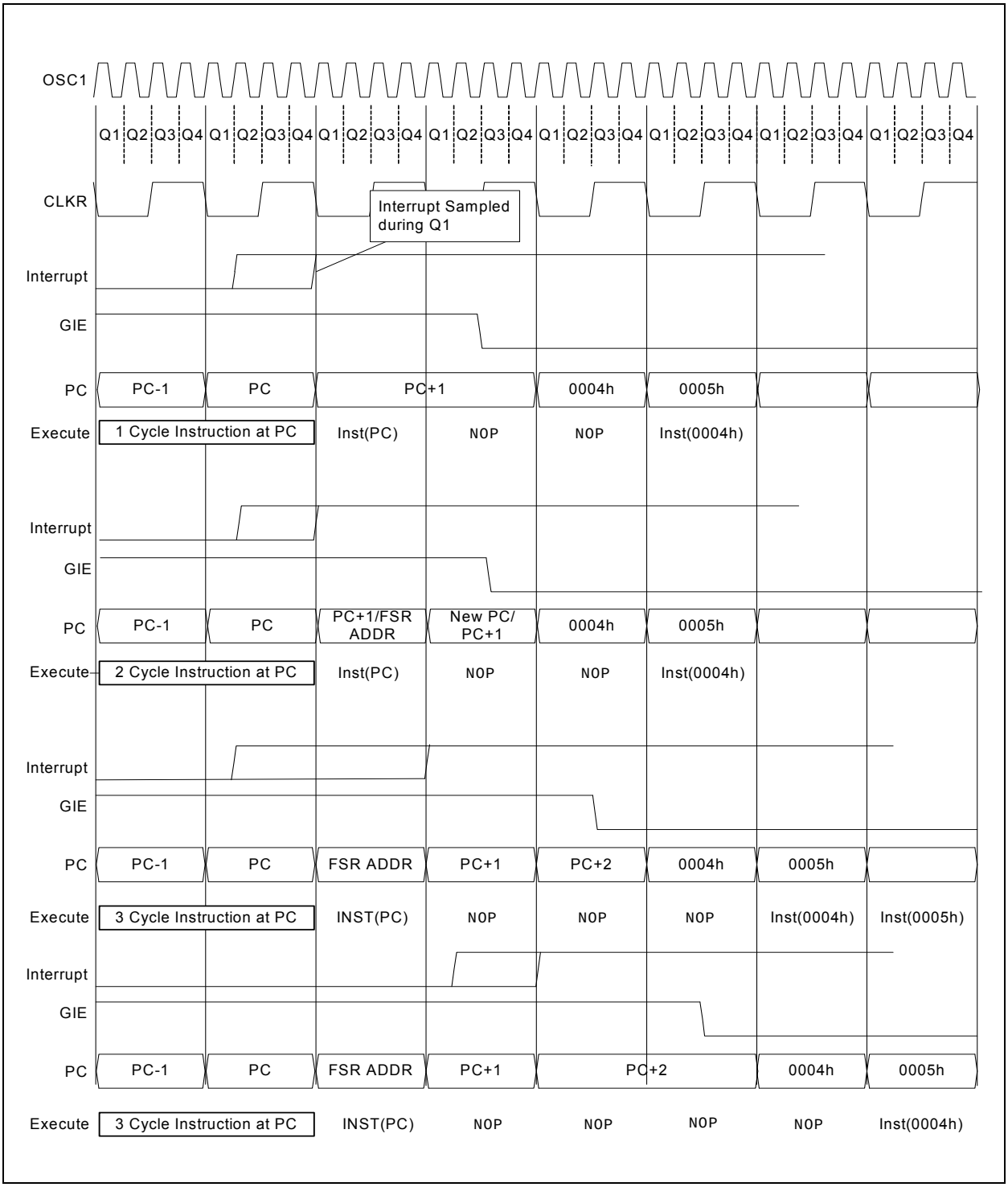
The Timer1 oscillator can be used as an alternate system clock source and can be selected during run-time using clock switching. Refer to **Section 6.3 "Clock Switching"** for more information.

FIGURE 6-5: QUARTZ CRYSTAL OPERATION (TIMER1 OSCILLATOR)



Note 1:	Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2:	Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.
3:	For oscillator design assistance, reference the following Microchip Applications Notes: • AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826) • AN849, "*Basic PIC® Oscillator Design*" (DS00849) • AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943) • AN949, "*Making Your Oscillator Work*" (DS00949) • TB097, "*Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS*" (DS91097) • AN1288, "*Design Practices for Low-Power External Oscillators*" (DS01288)

FIGURE 8-2: INTERRUPT LATENCY



9.2 Low-Power Sleep Mode

"F" devices contain an internal Low Dropout (LDO) voltage regulator, which allows the device I/O pins to operate at voltages up to 5.5V while the internal device logic operates at a lower voltage. The LDO and its associated reference circuitry must remain active when the device is in Sleep mode. "F" devices allow the user to optimize the operating current in Sleep, depending on the application requirements.

A Low-Power Sleep mode can be selected by setting the VREGPM bit of the VREGCON register. With this bit set, the LDO and reference circuitry are placed in a low-power state when the device is in Sleep.

9.2.1 SLEEP CURRENT VS. WAKE-UP TIME

In the default operating mode, the LDO and reference circuitry remain in the normal configuration while in Sleep. The device is able to exit Sleep mode quickly since all circuits remain active. In Low-Power Sleep mode, when waking up from Sleep, an extra delay time is required for these circuits to return to the normal configuration and stabilize.

The Low-Power Sleep mode is beneficial for applications that stay in Sleep mode for long periods of time. The normal mode is beneficial for applications that need to wake from Sleep quickly and frequently.

9.2.2 PERIPHERAL USAGE IN SLEEP

Some peripherals that can operate in Sleep mode will not operate properly with the Low-Power Sleep mode selected. The LDO will remain in the normal power mode when those peripherals are enabled. The Low-Power Sleep mode is intended for use with these peripherals:

- Brown-Out Reset (BOR)
- Watchdog Timer (WDT)
- External interrupt pin/Interrupt-on-change pins
- Timer1 (with external clock source)

Note:	"LF" devices do not have a configurable Low-Power Sleep mode. "LF" devices are an unregulated device and are always in the lowest power state when in Sleep, with no wake-up time penalty. These devices have a lower maximum V_{DD} and I/O voltage than "F" devices. See **Section 31.0 "Electrical Specifications"** for more information.

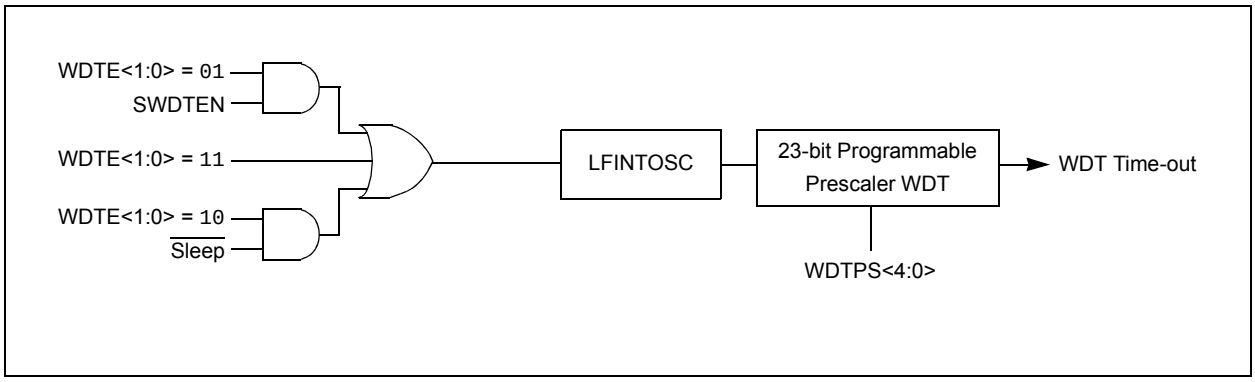
11.0 WATCHDOG TIMER (WDT)

The Watchdog Timer is a system timer that generates a Reset if the firmware does not issue a CLRWDT instruction within the time-out period. The Watchdog Timer is typically used to recover the system from unexpected events.

The WDT has the following features:

- Independent clock source
- Multiple operating modes
  - WDT is always on
  - WDT is off when in Sleep
  - WDT is controlled by software
  - WDT is always off
- Configurable time-out period is from 1 ms to 256 seconds (nominal)
- Multiple Reset conditions
- Operation during Sleep

FIGURE 11-1: WATCHDOG TIMER BLOCK DIAGRAM



EXAMPLE 12-6: WRITING TO FLASH PROGRAM MEMORY

```
; This write routine assumes the following:
; 1. The 16 bytes of data are loaded, starting at the address in DATA_ADDR
; 2. Each word of data to be written is made up of two adjacent bytes in DATA_ADDR,
;    stored in little endian format
; 3. A valid starting address (the least significant bits = 0000) is loaded in ADDRH:ADDRL
; 4. ADDRH and ADDRL are located in shared data memory 0x70 - 0x7F (common RAM)
;
        BCF         INTCON,GIE     ; Disable ints so required sequences will execute properly
        BANKSEL     EEADRH         ; Bank 3
        MOVF        ADDRH,W        ; Load initial address
        MOVWF       EEADRH         ;
        MOVF        ADDRL,W        ;
        MOVWF       EEADRL         ;
        MOVLW       LOW DATA_ADDR  ; Load initial data address
        MOVWF       FSR0L          ;
        MOVLW       HIGH DATA_ADDR ; Load initial data address
        MOVWF       FSR0H          ;
        BSF         EECON1,EEPGD   ; Point to program memory
        BCF         EECON1,CFGS    ; Not configuration space
        BSF         EECON1,WREN    ; Enable writes
        BSF         EECON1,LWLO    ; Only Load Write Latches
LOOP
        MOVIW       FSR0++         ; Load first data byte into lower
        MOVWF       EEDATL         ;
        MOVIW       FSR0++         ; Load second data byte into upper
        MOVWF       EEDATH         ;

        MOVF        EEADRL,W       ; Check if lower bits of address are '000'
        XORLW       0x0F           ; Check if we're on the last of 16 addresses
        ANDLW       0x0F           ;
        BTFSC       STATUS,Z       ; Exit if last of 16 words,
        GOTO        START_WRITE    ;

  Required Sequence
        MOVLW       55h            ; Start of required write sequence:
        MOVWF       EECON2         ; Write 55h
        MOVLW       0AAh           ;
        MOVWF       EECON2         ; Write AAh
        BSF         EECON1,WR      ; Set WR bit to begin write
        NOP                        ; Any instructions here are ignored as processor
                                   ; halts to begin write sequence
        NOP                        ; Processor will stop here and wait for write to complete.

                                   ; After write processor continues with 3rd instruction.

        INCF        EEADRL,F       ; Still loading latches Increment address
        GOTO        LOOP           ; Write next latches

START_WRITE
        BCF         EECON1,LWLO    ; No more loading latches - Actually start Flash program
                                   ; memory write

  Required Sequence
        MOVLW       55h            ; Start of required write sequence:
        MOVWF       EECON2         ; Write 55h
        MOVLW       0AAh           ;
        MOVWF       EECON2         ; Write AAh
        BSF         EECON1,WR      ; Set WR bit to begin write
        NOP                        ; Any instructions here are ignored as processor
                                   ; halts to begin write sequence
        NOP                        ; Processor will stop here and wait for write complete.

                                   ; after write processor continues with 3rd instruction
        BCF         EECON1,WREN    ; Disable writes
        BSF         INTCON,GIE     ; Enable interrupts
```

21.7 Comparator Negative Input Selection

The CxNCH<2:0> bits of the CMxCON0 register direct an analog input pin or analog ground to the inverting input of the comparator:

- CxIN- pin
- Analog Ground

Some inverting input selections share a pin with the operational amplifier output function. Enabling both functions at the same time will direct the operational amplifier output to the comparator inverting input.

Note:	To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

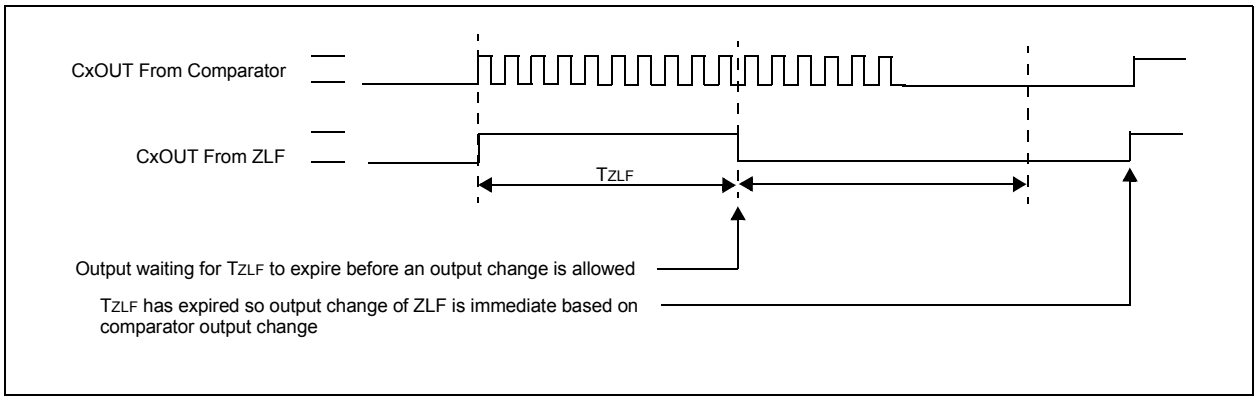
21.8 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 31.0 "Electrical Specifications"** for more details.

21.9 Zero Latency Filter

In high-speed operation, and under proper circuit conditions, it is possible for the comparator output to oscillate. This oscillation can have adverse effects on the hardware and software relying on this signal. Therefore, a digital filter has been added to the comparator output to suppress the comparator output oscillation. Once the comparator output changes, the output is prevented from reversing the change for a nominal time of 20 ns. This allows the comparator output to stabilize without affecting other dependent devices. Refer to Figure 21-3.

FIGURE 21-3: COMPARATOR ZERO LATENCY FILTER OPERATION



21.11 Register Definitions: Comparator Control

REGISTER 21-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0
CxON	CxOUT	CxOE	CxPOL	CxZLF	CxSP	CxHYS	CxSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CxON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **CxOUT:** Comparator Output bit
If CxPOL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If CxPOL = 0 (non-inverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **CxOE:** Comparator Output Enable bit
1 = CxOUT is present on the CxOUT pin. Requires that the associated TRIS bit be cleared to actually drive the pin. Not affected by CxON.
0 = CxOUT is internal only

bit 4 **CxPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3 **CxZLF:** Comparator Zero Latency Filter Enable bit
1 = Comparator output is filtered
0 = Comparator output is unfiltered

bit 2 **CxSP:** Comparator Speed/Power Select bit
1 = Comparator operates in normal power, higher speed mode
0 = Comparator operates in low-power, low-speed mode

bit 1 **CxHYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **CxSYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous.

26.3.2 COMPLEMENTARY PWM

The complementary PWM uses the same events as the single PWM, but two waveforms are generated instead of only one.

The two waveforms are opposite in polarity to each other. The two waveforms may also have dead-band control as well.

26.3.2.1 Mode Features and Controls

- Dead-band control available
- PWM primary output can be steered to the following pins:
  - PSMCxA
  - PSMCxC
  - PSMCxE
- PWM complementary output can be steered to the following pins:
  - PSMCxB
  - PSMCxD
  - PSMCxE

26.3.2.2 Waveform Generation

Rising Edge Event

- Complementary output is set inactive
- Optional rising edge dead band is activated
- Primary output is set active

Falling Edge Event

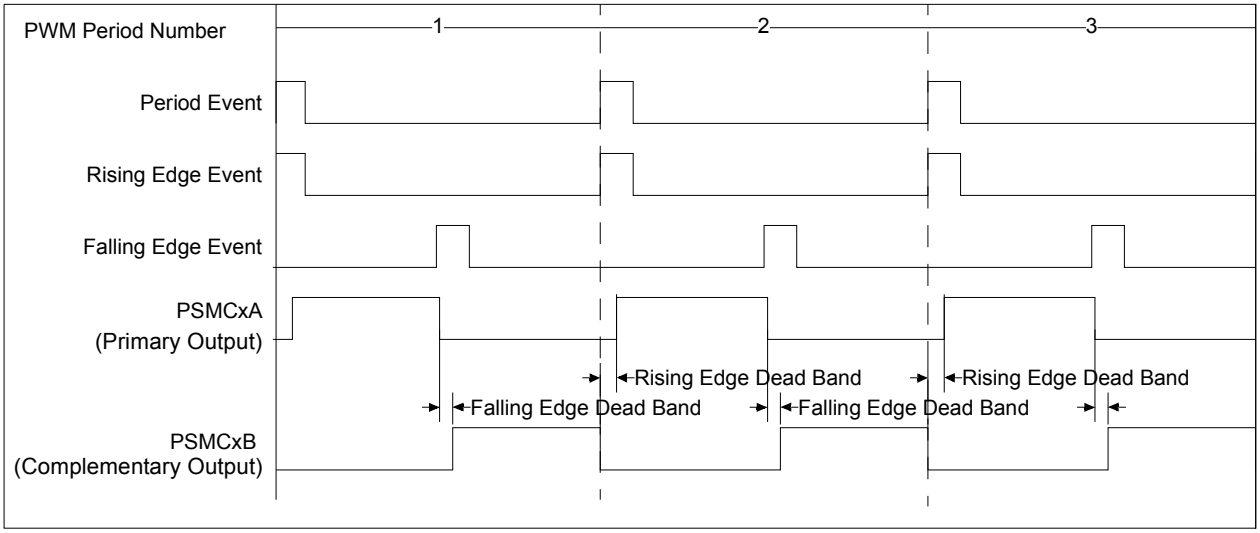
- Primary output is set inactive
- Optional falling edge dead band is activated
- Complementary output is set active

Code for setting up the PSMC generate the complementary single-phase waveform shown in Figure 26-5, and given in Example 26-2.

EXAMPLE 26-2: COMPLEMENTARY SINGLE-PHASE SETUP

```
; Complementary Single-phase PWM PSMC setup
; Fully synchronous operation
; Period = 10 us
; Duty cycle = 50%
; Deadband = 93.75 +15.6/-0 ns
   BANKSEL PSMC1CON
   MOVLW   0x02        ; set period
   MOVWF   PSMC1PRH
   MOVLW   0x7F
   MOVWF   PSMC1PRL
   MOVLW   0x01        ; set duty cycle
   MOVWF   PSMC1DCH
   MOVLW   0x3F
   MOVWF   PSMC1DCL
   CLRF    PSMC1PHH    ; no phase offset
   CLRF    PSMC1PHL
   MOVLW   0x01        ; PSMC clock=64 MHz
   MOVWF   PSMC1CLK
; output on A, normal polarity
   MOVLW   B'00000011'; A and B enables
   MOVWF   PSMC1OEN
   MOVWF   PSMC1STR0
   CLRF    PSMC1POL
; set time base as source for all events
   BSF     PSMC1PRS, P1PRST
   BSF     PSMC1PHS, P1PHST
   BSF     PSMC1DCS, P1DCST
; set rising and falling dead-band times
   MOVLW   D'6'
   MOVWF   PSMC1DBR
   MOVWF   PSMC1DBF
; enable PSMC in Complementary Single Mode
; this also loads steering and time buffers
; and enables rising and falling deadbands
   MOVLW   B'11110001'
   MOVWF   PSMC1CON
   BANKSEL TRISC
   BCF     TRISC, 0    ; enable pin drivers
   BCF     TRISC, 1
```

FIGURE 26-5: COMPLEMENTARY PWM WAVEFORM – PSMCXSTR0 = 03H



26.3.8 PULSE-SKIPPING PWM WITH COMPLEMENTARY OUTPUTS

The pulse-skipping PWM is used to generate a series of fixed-length pulses that may or not be triggered at each period event. If any of the sources enabled to generate a rising edge event are high when a period event occurs, a pulse will be generated. If the rising edge sources are low at the period event, no pulse will be generated.

The rising edge occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

26.3.8.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM is output on only PSMCxA.
- Complementary PWM is output on only PSMCxB.

26.3.8.2 Waveform Generation

Rising Edge Event

If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:

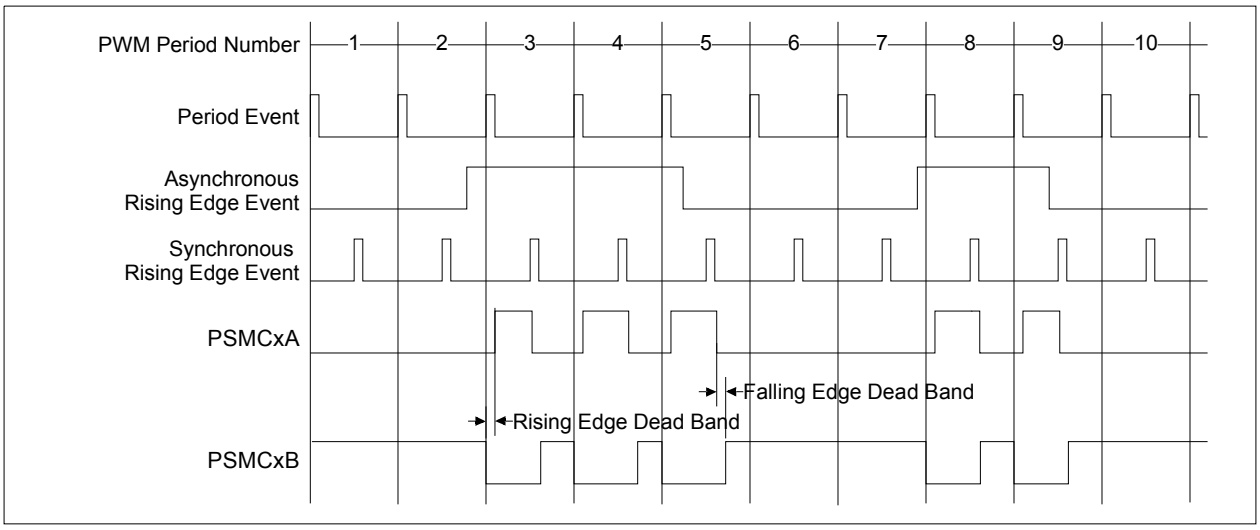
- Complementary output is set inactive
- Dead-band rising is activated (if enabled)
- Primary output is set active

Falling Edge Event

- Primary output is set inactive
- Dead-band falling is activated (if enabled)
- Complementary output is set active

Note:	To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 26-11: PULSE-SKIPPING WITH COMPLEMENTARY OUTPUT PWM WAVEFORM



26.12 Register Definitions: PSMC Control

REGISTER 26-1: PSMCxCON: PSMC CONTROL REGISTER

R/W-0/0	R/W/HC-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxEN	PSMCxLD	PxDBFE	PxDBRE	PxMODE<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **PSMCxEN:** PSMC Module Enable bit
- 1 = PSMCx module is enabled
- 0 = PSMCx module is disabled

bit 6 **PSMCxLD:** PSMC Load Buffer Enable bit
- 1 = PSMCx registers are ready to be updated with the appropriate register contents
- 0 = PSMCx buffer update complete

bit 5 **PxDBFE:** PSMC Falling Edge Dead-Band Enable bit
- 1 = PSMCx falling edge dead band enabled
- 0 = PSMCx falling edge dead band disabled

bit 4 **PxDBRE:** PSMC Rising Edge Dead-Band Enable bit
- 1 = PSMCx rising edge dead band enabled
- 0 = PSMCx rising edge dead band disabled

bit 3-0 **PxMODE<3:0>** PSMC Operating Mode bits
- 1111 = Reserved
- 1110 = Reserved
- 1101 = Reserved
- 1100 = 3-phase steering PWM
- 1011 = Fixed duty cycle, variable frequency, complementary PWM
- 1010 = Fixed duty cycle, variable frequency, single PWM
- 1001 = ECCP compatible Full-Bridge forward output
- 1000 = ECCP compatible Full-Bridge reverse output
- 0111 = Pulse-skipping with complementary output
- 0110 = Pulse-skipping PWM output
- 0101 = Push-pull with four full-bridge outputs and complementary outputs
- 0100 = Push-pull with four full-bridge outputs
- 0011 = Push-pull with complementary outputs
- 0010 = Push-pull output
- 0001 = Single PWM with complementary output (with PWM steering capability)
- 0000 = Single PWM waveform generation (with PWM steering capability)

REGISTER 26-11: PSMCxREBS: PSMC RISING EDGE BLANKED SOURCE REGISTER

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxREBSIN	—	—	PxREBSC4	PxREBSC3	PxREBSC2	PxREBSC1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxREBSIN:** PSMCx Rising Edge Event Blanked from PSMCxIN pin
1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = PSMCxIN pin is not blanked

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxREBSC4:** PSMCx Rising Edge Event Blanked from sync_C4OUT
1 = sync_C4OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C4OUT is not blanked

bit 3 **PxREBSC3:** PSMCx Rising Edge Event Blanked from sync_C3OUT
1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C3OUT is not blanked

bit 2 **PxREBSC2:** PSMCx Rising Edge Event Blanked from sync_C2OUT
1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C2OUT is not blanked

bit 1 **PxREBSC1:** PSMCx Rising Edge Event Blanked from sync_C1OUT
1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C1OUT is not blanked

bit 0 **Unimplemented:** Read as '0'

REGISTER 26-12: PSMCxFEBS: PSMC FALLING EDGE BLANKED SOURCE REGISTER

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxFEBSIN	—	—	PxFEBSC4	PxFEBSC3	PxFEBSC2	PxFEBSC1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxFEBSIN:** PSMCx Falling Edge Event Blanked from PSMCxIN pin
1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = PSMCxIN pin is not blanked

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxFEBSC4:** PSMCx Falling Edge Event Blanked from sync_C4OUT
1 = sync_C4OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C4OUT is not blanked

bit 3 **PxFEBSC3:** PSMCx Falling Edge Event Blanked from sync_C3OUT
1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C3OUT is not blanked

bit 2 **PxFEBSC2:** PSMCx Falling Edge Event Blanked from sync_C2OUT
1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C2OUT is not blanked

bit 1 **PxFEBSC1:** PSMCx Falling Edge Event Blanked from sync_C1OUT
1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C1OUT is not blanked

bit 0 **Unimplemented:** Read as '0'

TABLE 26-5: SUMMARY OF REGISTERS ASSOCIATED WITH PSMC

Name	Bit7	Bit6	Bit5	Bit4	BIt3	Bit2	Bit1	Bit0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
ODCONC	ODC7	ODC6	ODC5	ODC4	ODC3	ODC2	ODC1	ODC0	148
PIE4	PSMC4TIE	PSMC3TIE	PSMC2TIE	PSMC1TIE	PSMC4SIE	PSMC3SIE	PSMC2SIE	PSMC1SIE	101
PIR4	PSMC4TIF	PSMC3TIF	PSMC2TIF	PSMC1TIF	PSMC4SIF	PSMC3SIF	PSMC2SIF	PSMC1SIF	105
PSMCxASDC	PxASE	PxASDEN	PxARSEN	—	—	—	—	PxASDOV	276
PSMCxASDL	—	—	PxASDLF(1)	PxASDLE(1)	PxASDLD(1)	PxASDLC(1)	PxASDLB	PxASDLA	277
PSMCxASDS	PxASDSIN	—	—	PxASDSC4	PxASDSC3	PxASDSC2	PxASDSC1	—	278
PSMCxBLKF	PSMCxBLKF<7:0>								284
PSMCxBLKR	PSMCxBLKR<7:0>								284
PSMCxBLNK	—	—	PxFEBM1	PxFEBM0	—	—	PxREBM1	PxREBM0	271
PSMCxCLK	—	—	PxCPRE<1:0>		—	—	PxCSRC<1:0>		270
PSMCxCON	PSMCxEN	PSMCxLD	PxDBFE	PxDBRE	PxMODE<3:0>				265
PSMCxDBF	PSMCxDBF<7:0>								283
PSMCxDBR	PSMCxDBR<7:0>								283
PSMCxDCH	PSMCxDC<15:8>								281
PSMCxDCL	PSMCxDC<7:0>								281
PSMCxDCS	PxDCSIN	—	—	PxDCSC4	PxDCSC3	PxDCSC2	PxDCSC1	PxDCST	274
PSMCxFEBS	PxFEBSIN	—	—	PxFEBSC4	PxFEBSC3	PxFEBSC2	PxFEBSC1	—	272
PSMCxFFA	—	—	—	—	PSMCxFFA<3:0>				283
PSMCxINT	PxTOVIE	PxTPHIE	PxTDCIE	PxTPRIE	PxTOVIF	PxTPHIF	PxTDCIF	PxTPRIF	288
PSMCxMDL	PxMDLEN	PxMDLPOL	PxMDLBIT	—	PxMSRC<3:0>				266
PSMCxOEN	—	—	PxOEF(1)	PxOEE(1)	PxOED(1)	PxOEC(1)	PxOEB	PxOEA	270
PSMCxPHH	PSMCxPH<15:8>								280
PSMCxPHL	PSMCxPH<7:0>								280
PSMCxPHS	PxPHSIN	—	—	PxPHSC4	PxPHSC3	PxPHSC2	PxPHSC1	PxPHST	273
PSMCxPOL	—	PxPOLIN	PxPOLF(1)	PxPOLE(1)	PxPOLD(1)	PxPOLC(1)	PxPOLB	PxPOLA	271
PSMCxPRH	PSMCxPR<15:8>								282
PSMCxPRL	PSMCxPR<7:0>								282
PSMCxPRS	PxPRSIN	—	—	PxPRSC4	PxPRSC3	PxPRSC2	PxPRSC1	PxPRST	275
PSMCxREBS	PxREBSIN	—	—	PxREBSC4	PxREBSC3	PxREBSC2	PxREBSC1	—	272
PSMCxSTR0	—	—	PxSTRF(1)	PxSTRE(1)	PxSTRD(1)	PxSTRC(1)	PxSTRB	PxSTRA	285
PSMCxSTR1	PxSSYNC	—	—	—	—	—	PxLSMEN	PxHSMEN	287
PSMCxSYNC	PxPOFST	PxPRPOL	PxDCPOL	—	—	PxSYNC<2:0>			267
PSMCxTMRH	PSMCxTMR<15:8>								279
PSMCxTMRL	PSMCxTMR<7:0>								279
SLRCONC	SLRC7	SLRC6	SLRC5	SLRC4	SLRC3	SLCR2	SRC1	SLRC0	148
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	147

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by PSMC module.

Note 1: Unimplemented in PSMC2.

27.5.2 SLAVE RECEPTION

When the R/$\overline{W}$ bit of a matching received address byte is clear, the R/$\overline{W}$ bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and acknowledged.

When the overflow condition exists for a received address, then not Acknowledge is given. An overflow condition is defined as either bit BF of the SSPSTAT register is set, or bit SSPOV of the SSPCON1 register is set. The BOEN bit of the SSPCON3 register modifies this operation. For more information see Register 27-4.

An MSSP interrupt is generated for each transferred data byte. Flag bit, SSP1IF, must be cleared by software.

When the SEN bit of the SSPCON2 register is set, SCL will be held low (clock stretch) following each received byte. The clock must be released by setting the CKP bit of the SSPCON1 register, except sometimes in 10-bit mode. See **Section 27.2.3 "SPI Master Mode"** for more detail.

27.5.2.1 7-bit Addressing Reception

This section describes a standard sequence of events for the MSSP module configured as an I^2C Slave in 7-bit Addressing mode. All decisions made by hardware or software and their effect on reception. Figure 27-13 and Figure 27-14 is used as a visual reference for this description.

This is a step by step process of what typically must be done to accomplish I^2C communication.

1. Start bit detected.
2. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Matching address with R/$\overline{W}$ bit clear is received.
4. The slave pulls SDA low sending an $\overline{ACK}$ to the master, and sets SSP1IF bit.
5. Software clears the SSP1IF bit.
6. Software reads received address from SSPBUF clearing the BF flag.
7. If SEN = 1; Slave software sets CKP bit to release the SCL line.
8. The master clocks out a data byte.
9. Slave drives SDA low sending an $\overline{ACK}$ to the master, and sets SSP1IF bit.
10. Software clears SSP1IF.
11. Software reads the received byte from SSPBUF clearing BF.
12. Steps 8-12 are repeated for all received bytes from the master.
13. Master sends Stop condition, setting P bit of SSPSTAT, and the bus goes idle.

27.5.2.2 7-bit Reception with AHEN and DHEN

Slave device reception with AHEN and DHEN set operate the same as without these options with extra interrupts and clock stretching added after the 8th falling edge of SCL. These additional interrupts allow the slave software to decide whether it wants to $\overline{ACK}$ the receive address or data byte, rather than the hardware. This functionality adds support for PMBus™ that was not present on previous versions of this module.

This list describes the steps that need to be taken by slave software to use these options for I^2C communication. Figure 27-15 displays a module using both address and data holding. Figure 27-16 includes the operation with the SEN bit of the SSPCON2 register set.

1. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
2. Matching address with R/$\overline{W}$ bit clear is clocked in. SSP1IF is set and CKP cleared after the 8th falling edge of SCL.
3. Slave clears the SSP1IF.
4. Slave can look at the ACKTIM bit of the SSPCON3 register to determine if the SSP1IF was after or before the $\overline{ACK}$.
5. Slave reads the address value from SSPBUF, clearing the BF flag.
6. Slave sets $\overline{ACK}$ value clocked out to the master by setting ACKDT.
7. Slave releases the clock by setting CKP.
8. SSP1IF is set after an $\overline{ACK}$, not after a NACK.
9. If SEN = 1 the slave hardware will stretch the clock after the $\overline{ACK}$.
10. Slave clears SSP1IF.

Note: SSP1IF is still set after the 9th falling edge of SCL even if there is no clock stretching and BF has been cleared. Only if NACK is sent to master is SSP1IF not set

11. SSP1IF set and CKP cleared after 8th falling edge of SCL for a received data byte.
12. Slave looks at ACKTIM bit of SSPCON3 to determine the source of the interrupt.
13. Slave reads the received data from SSPBUF clearing BF.
14. Steps 7-14 are the same for each received data byte.
15. Communication is ended by either the slave sending an $\overline{ACK}$ = 1, or the master sending a Stop condition. If a Stop is sent and Interrupt on Stop Detect is disabled, the slave will only know by polling the P bit of the SSTSTAT register.

27.5.3 SLAVE TRANSMISSION

When the R/$\overline{W}$ bit of the incoming address byte is set and an address match occurs, the R/$\overline{W}$ bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register, and an $\overline{ACK}$ pulse is sent by the slave on the ninth bit.

Following the $\overline{ACK}$, slave hardware clears the CKP bit and the SCL pin is held low (see **Section 27.5.6 "Clock Stretching"** for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data.

The transmit data must be loaded into the SSPBUF register which also loads the SSPSR register. Then the SCL pin should be released by setting the CKP bit of the SSPCON1 register. The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time.

The $\overline{ACK}$ pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. This $\overline{ACK}$ value is copied to the ACKSTAT bit of the SSPCON2 register. If ACKSTAT is set (not $\overline{ACK}$), then the data transfer is complete. In this case, when the not $\overline{ACK}$ is latched by the slave, the slave goes idle and waits for another occurrence of the Start bit. If the SDA line was low ($\overline{ACK}$), the next transmit data must be loaded into the SSPBUF register. Again, the SCL pin must be released by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSP1IF bit must be cleared by software and the SSPSTAT register is used to determine the status of the byte. The SSP1IF bit is set on the falling edge of the ninth clock pulse.

27.5.3.1 Slave Mode Bus Collision

A slave receives a Read request and begins shifting data out on the SDA line. If a bus collision is detected and the SBCDE bit of the SSPCON3 register is set, the BCL1IF bit of the PIR register is set. Once a bus collision is detected, the slave goes idle and waits to be addressed again. User software can use the BCL1IF bit to handle a slave bus collision.

27.5.3.2 7-bit Transmission

A master device can transmit a read request to a slave, and then clock data out of the slave. The list below outlines what software for a slave will need to do to accomplish a standard transmission. Figure 27-17 can be used as a reference to this list.

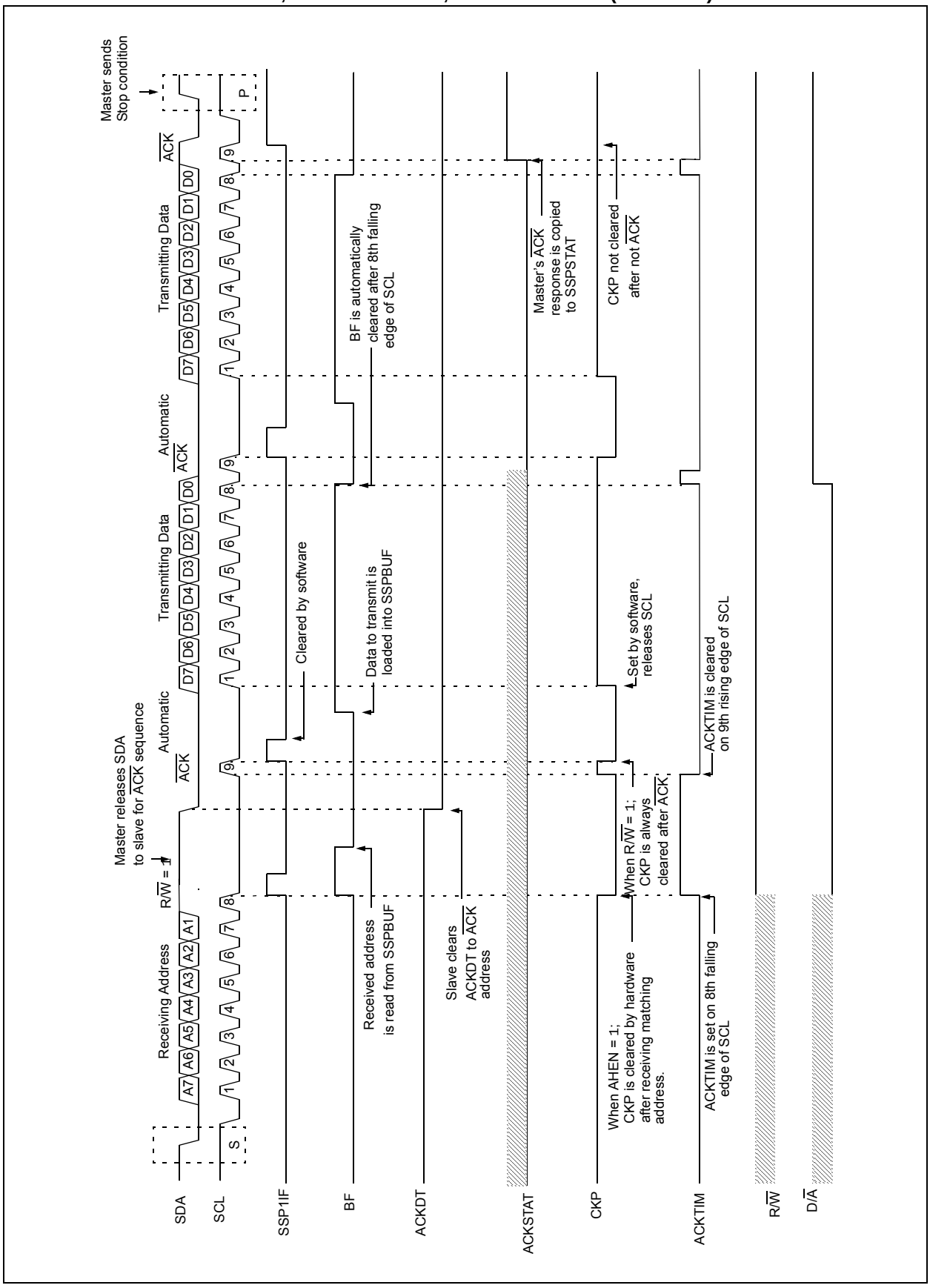
1. Master sends a Start condition on SDA and SCL.
2. S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Matching address with R/$\overline{W}$ bit set is received by the Slave setting SSP1IF bit.
4. Slave hardware generates an $\overline{ACK}$ and sets SSP1IF.
5. SSP1IF bit is cleared by user.
6. Software reads the received address from SSPBUF, clearing BF.
7. R/$\overline{W}$ is set so CKP was automatically cleared after the $\overline{ACK}$.
8. The slave software loads the transmit data into SSPBUF.
9. CKP bit is set releasing SCL, allowing the master to clock the data out of the slave.
10. SSP1IF is set after the $\overline{ACK}$ response from the master is loaded into the ACKSTAT register.
11. SSP1IF bit is cleared.
12. The slave software checks the ACKSTAT bit to see if the master wants to clock out more data.

Note 1: If the master $\overline{ACK}$s the clock will be stretched.

2: ACKSTAT is the only bit updated on the rising edge of SCL (9th) rather than the falling.

13. Steps 9-13 are repeated for each transmitted byte.
14. If the master sends a not $\overline{ACK}$; the clock is not held, but SSP1IF is still set.
15. The master sends a Restart condition or a Stop.
16. The slave is no longer addressed.

FIGURE 27-19: I²C SLAVE, 7-BIT ADDRESS, TRANSMISSION (AHEN = 1)



REGISTER 27-2: SSPCON1: SSP CONTROL REGISTER 1

R/C/HS-0/0	R/C/HS-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>			
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets	
'1' = Bit is set	'0' = Bit is cleared	HS = Bit is set by hardware	C = User cleared

bit 7 **WCOL:** Write Collision Detect bit
Master mode:
1 = A write to the SSPBUF register was attempted while the I²C conditions were not valid for a transmission to be started
0 = No collision
Slave mode:
1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)
0 = No collision

bit 6 **SSPOV:** Receive Overflow Indicator bit(1)
In SPI mode:
1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. In Slave mode, the user must read the SSPBUF, even if only transmitting data, to avoid setting overflow. In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register (must be cleared in software).
0 = No overflow
In I²C mode:
1 = A byte is received while the SSPBUF register is still holding the previous byte. SSPOV is a "don't care" in Transmit mode (must be cleared in software).
0 = No overflow

bit 5 **SSPEN:** Synchronous Serial Port Enable bit
In both modes, when enabled, these pins must be properly configured as input or output
In SPI mode:
1 = Enables serial port and configures SCK, SDO, SDI and $\overline{SS}$ as the source of the serial port pins(2)
0 = Disables serial port and configures these pins as I/O port pins
In I²C mode:
1 = Enables the serial port and configures the SDA and SCL pins as the source of the serial port pins(3)
0 = Disables serial port and configures these pins as I/O port pins

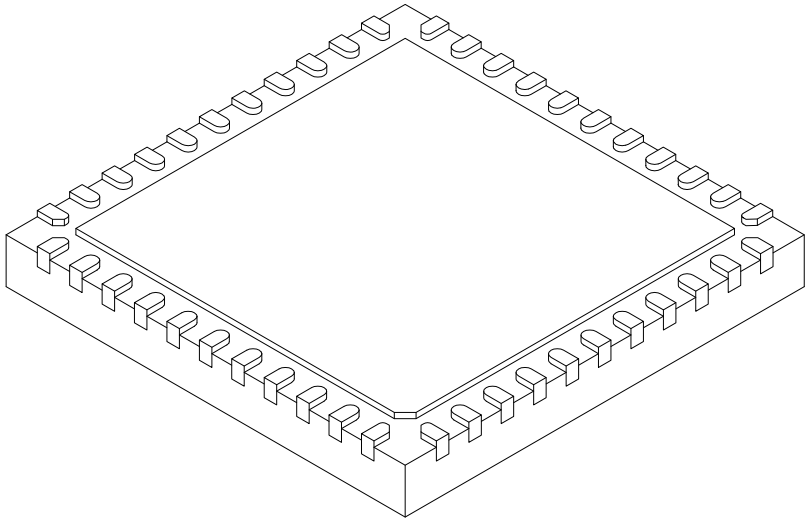
bit 4 **CKP:** Clock Polarity Select bit
In SPI mode:
1 = Idle state for clock is a high level
0 = Idle state for clock is a low level
In I²C Slave mode:
SCL release control
1 = Enable clock
0 = Holds clock low (clock stretch). (Used to ensure data setup time.)
In I²C Master mode:
Unused in this mode

bit 3-0 **SSPM<3:0>:** Synchronous Serial Port Mode Select bits
0000 = SPI Master mode, clock = FOSC/4
0001 = SPI Master mode, clock = FOSC/16
0010 = SPI Master mode, clock = FOSC/64
0011 = SPI Master mode, clock = TMR2 output/2
0100 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control enabled
0101 = SPI Slave mode, clock = SCK pin, $\overline{SS}$ pin control disabled, $\overline{SS}$ can be used as I/O pin
0110 = I²C Slave mode, 7-bit address
0111 = I²C Slave mode, 10-bit address
1000 = I²C Master mode, clock = FOSC / (4 * (SSPADD+1))(4)
1001 = Reserved
1010 = SPI Master mode, clock = FOSC/(4 * (SSPADD+1))(5)
1011 = I²C firmware controlled Master mode (Slave idle)
1100 = Reserved
1101 = Reserved
1110 = I²C Slave mode, 7-bit address with Start and Stop bit interrupts enabled
1111 = I²C Slave mode, 10-bit address with Start and Stop bit interrupts enabled

Note 1: In Master mode, the overflow bit is not set since each new reception (and transmission) is initiated by writing to the SSPBUF register.
2: When enabled, these pins must be properly configured as input or output.
3: When enabled, the SDA and SCL pins must be configured as inputs.
4: SSPADD values of 0, 1 or 2 are not supported for I²C mode.
5: SSPADD value of '0' is not supported. Use SSPM = 0000 instead.

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2