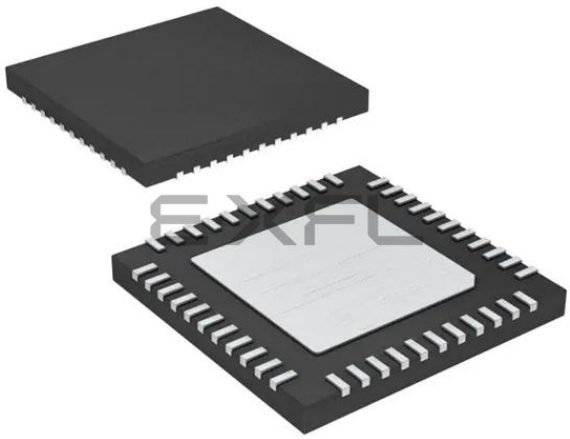


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 14x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1789-e-ml

PIN ALLOCATION TABLE

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1788)

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN,	ADC	Reference	Comparator	Operation Amplifiers	8-bit/ 5-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN0	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—
RA1	3	28	AN1	—	C1IN1- C2IN1- C3IN1- C4IN1-	OPA1OUT	—	—	—	—	—	—	IOC	Y	—
RA2	4	1	AN2	VREF- DAC1VREF-	C1IN0+ C2IN0+ C3IN0+ C4IN0+		DAC1OUT1	—	—	—	—	—	IOC	Y	—
RA3	5	2	AN3	VREF+ DAC1VREF+ DAC2VREF+ DAC3VREF+ DAC4VREF+	C1IN1+	—	—	—	—	—	—	—	IOC	Y	—
RA4	6	3	—	—	C1OUT	OPA1IN+	DAC4OUT1	T0CKI	—	—	—	—	IOC	Y	—
RA5	7	4	AN4	—	C2OUT	OPA1IN-	DAC2OUT1	—	—	—	—	$\overline{SS}$	IOC	Y	—
RA6	10	7	—	—	C2OUT(1)	—	—	—	—	—	—	—	IOC	Y	VCAP OSC2 CLKOUT
RA7	9	6	—	—	—	—	—	—	PSMC1CLK PSMC2CLK PSMC3CLK PSMC4CLK	—	—	—	IOC	Y	CLKIN OSC1
RB0	21	18	AN12	—	C2IN1+	—	—	—	PSMC1IN PSMC2IN PSMC3IN PSMC4IN	CCP1(1)	—	—	INT IOC	Y	—
RB1	22	19	AN10	—	C1IN3- C2IN3- C3IN3- C4IN3-	OPA2OUT	—	—	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	—	—	OPA2IN-	DAC3OUT1	—	—	—	—	—	IOC	Y	CLKR
RB3	24	21	AN9	—	C1IN2- C2IN2- C3IN2-	OPA2IN+	—	—	—	CCP2(1)	—	—	IOC	Y	—
RB4	25	22	AN11	—	C3IN1+	—	—	—	—	—	—	$\overline{SS}$(1)	IOC	Y	—
RB5	26	23	AN13	—	C4IN2- C3OUT	—	—	T1G	—	CCP3(1)	—	SDO(1)	IOC	Y	—
RB6	27	24	—	—	C4IN1+	—	—	—	—	—	TX(1) CK(1)	SDI(1) SDA(1)	IOC	Y	ICSPCLK
RB7	28	25	—	—	—	—	DAC1OUT2 DAC2OUT2 DAC3OUT2 DAC4OUT2	—	—	—	RX(1) DT(1)	SCK(1) SCL(1)	IOC	Y	ICSPDAT
RC0	11	8	—	—	—	—	—	T1CKI T1OSO	PSMC1A	—	—	—	IOC	Y	—
RC1	12	9	—	—	—	—	—	T1OSI	PSMC1B	CCP2	—	—	IOC	Y	—
RC2	13	10	—	—	—	—	—	—	PSMC1C PSMC3B	CCP1	—	—	IOC	Y	—
RC3	14	11	—	—	—	—	—	—	PSMC1D PSMC4A	—	—	SCK SCL	IOC	Y	—
RC4	15	12	—	—	—	—	—	—	PSMC1E PSMC4B	—	—	SDI SDA	IOC	Y	—
RC5	16	13	—	—	—	—	—	—	PSMC1F PSMC3A	—	—	SDO	IOC	Y	—

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

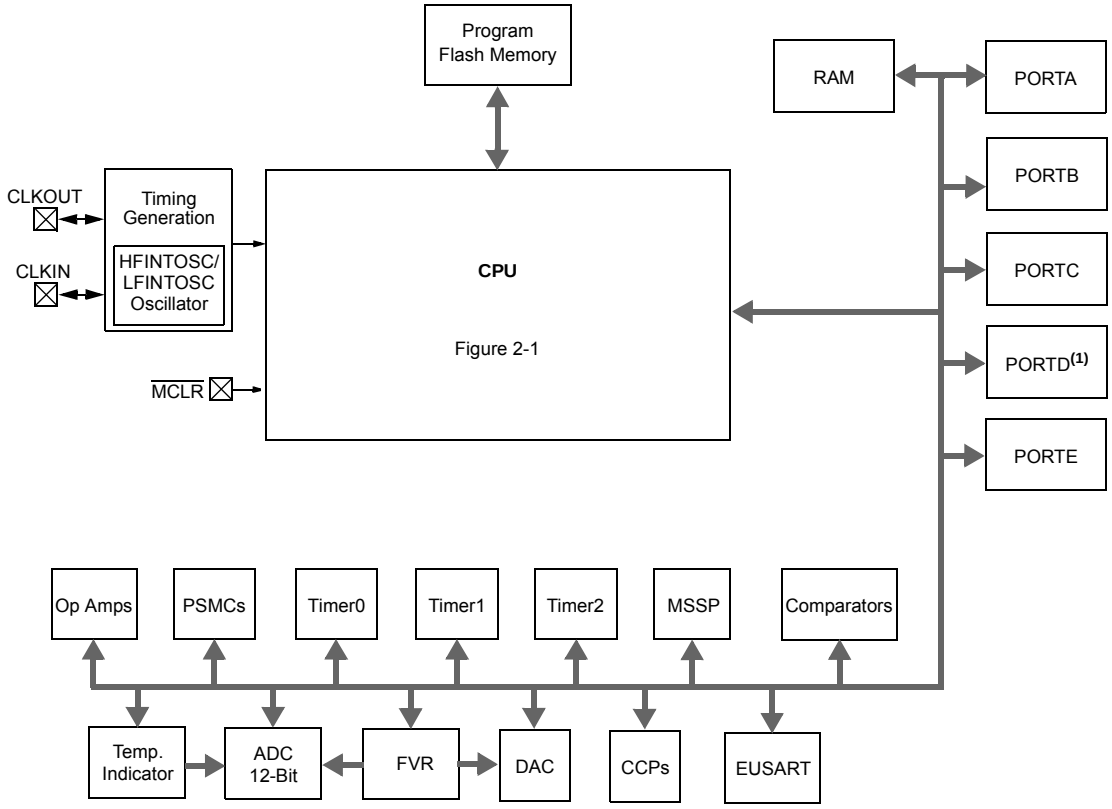
1.0 DEVICE OVERVIEW

The PIC16(L)F1788/9 are described within this data sheet. The block diagram of these devices are shown in Figure 1-1. The available peripherals are shown in Table 1-1, and the pin out descriptions are shown in Tables 1-2 and 1-3.

TABLE 1-1: DEVICE PERIPHERAL SUMMARY

Peripheral		PIC16(L)F1782	PIC16(L)F1783	PIC16(L)F1784	PIC16(L)F1786	PIC16(L)F1787	PIC16(L)F1788	PIC16(L)F1789
Analog-to-Digital Converter (ADC)		●	●	●	●	●	●	●
Fixed Voltage Reference (FVR)		●	●	●	●	●	●	●
Reference Clock Module		●	●	●	●	●	●	●
Temperature Indicator		●	●	●	●	●	●	●
Capture/Compare/PWM (CCP/ECCP) Modules								
	CCP1	●	●	●	●	●	●	●
	CCP2	●	●	●	●	●	●	●
	CCP3			●	●	●	●	●
Comparators								
	C1	●	●	●	●	●	●	●
	C2	●	●	●	●	●	●	●
	C3	●	●	●	●	●	●	●
	C4			●	●	●	●	●
Digital-to-Analog Converter (DAC)								
	(8-bit DAC) D1	●	●	●	●	●	●	●
	(5-bit DAC) D2						●	●
	(5-bit DAC) D3						●	●
	(5-bit DAC) D4						●	●
Enhanced Universal Synchronous/Asynchronous Receiver/Transmitter (EUSART)								
	EUSART	●	●	●	●	●	●	●
Master Synchronous Serial Ports								
	MSSP	●	●	●	●	●	●	●
Op Amp								
	Op Amp 1	●	●	●	●	●	●	●
	Op Amp 2	●	●	●	●	●	●	●
	Op Amp 3			●		●		●
Programmable Switch Mode Controller (PSMC)								
	PSMC1	●	●	●	●	●	●	●
	PSMC2	●	●	●	●	●	●	●
	PSMC3			●	●	●	●	●
	PSMC4						●	●
Timers								
	Timer0	●	●	●	●	●	●	●
	Timer1	●	●	●	●	●	●	●
	Timer2	●	●	●	●	●	●	●

FIGURE 1-1: PIC16(L)F1788/9 BLOCK DIAGRAM



Note 1: PIC16(L)F1789 only.
2: See applicable chapters for more information on peripherals.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 29 (Continued)											
EB1h	PSMC2CON	PSMC2EN	PSMC2LD	P2DBFE	P2DBRE	P2MODE<3:0>				0000 0000	0000 0000
EB2h	PSMC2MDL	P2MDLEN	P2MDLPOL	P2MDLBIT	—	P2MSRC<3:0>				000- 0000	000- 0000
EB3h	PSMC2SYNC	P2POFST	P2PRPOL	P2DCPOL	—	—	P2SYNC<2:0>			000- -000	000- -000
EB4h	PSMC2CLK	—	—	P2CPRE<1:0>		—	—	P2CSRC<1:0>		--00 --00	--00 --00
EB5h	PSMC2OEN	—	—	—	—	—	—	P2OEB	P2OEA	---- --00	---- --00
EB6h	PSMC2POL	—	P2INPOL	—	—	—	—	P2POLB	P2POLA	-0-- --00	-0-- --00
EB7h	PSMC2BLNK	—	—	P2FEBM<1:0>		—	—	P2REBM<1:0>		--00 --00	--00 --00
EB8h	PSMC2REBS	P2REBSIN	—	—	P2REBSC4	P2REBSC3	P2REBSC2	P2REBSC1	—	0--0 000-	0--0 000-
EB9h	PSMC2FEBS	P2FEBSIN	—	—	P2FEBSC4	P2FEBSC3	P2FEBSC2	P2FEBSC1	—	0--0 000-	0--0 000-
EBAh	PSMC2PHS	P2PHSIN	—	—	P2PHSC4	P2PHSC3	P2PHSC2	P2PHSC1	P2PHST	0--0 0000	0--0 0000
EBBh	PSMC2DCS	P2DCSIN	—	—	P2DCSC4	P2DCSC3	P2DCSC2	P2DCSC1	P2DCST	0--0 0000	0--0 0000
EBCh	PSMC2PRS	P2PRSIN	—	—	P2PRSC4	P2PRSC3	P2PRSC2	P2PRSC1	P2PRST	0--0 0000	0--0 0000
EBDh	PSMC2ASDC	P2ASE	P2ASDEN	P2ARSEN	—	—	—	—	P2ASDOV	000- ---0	000- ---0
EBEh	PSMC2ASDL	—	—	—	—	—	—	P2ASDLB	P2ASDLA	---- --00	---- --00
EBFh	PSMC2ASDS	P2ASDSIN	—	—	P2ASDSC4	P2ASDSC3	P2ASDSC2	P2ASDSC1	—	0--0 000-	0--0 000-
EC0h	PSMC2INT	P2TOVIE	P2TPHIE	P2TDCIE	P2TPRIE	P2TOVIF	P2TPHIF	P2TDCIF	P2TPRIF	0000 0000	0000 0000
EC1h	PSMC2PHL	Phase Low Count								0000 0000	0000 0000
EC2h	PSMC2PHH	Phase High Count								0000 0000	0000 0000
EC3h	PSMC2DCL	Duty Cycle Low Count								0000 0000	0000 0000
EC4h	PSMC2DCH	Duty Cycle High Count								0000 0000	0000 0000
EC5h	PSMC2PRL	Period Low Count								0000 0000	0000 0000
EC6h	PSMC2PRH	Period High Count								0000 0000	0000 0000
EC7h	PSMC2TMRL	Time base Low Counter								0000 0001	0000 0001
EC8h	PSMC2TMRH	Time base High Counter								0000 0000	0000 0000
EC9h	PSMC2DBR	Rising Edge Dead-band Counter								0000 0000	0000 0000
ECAh	PSMC2DBF	Falling Edge Dead-band Counter								0000 0000	0000 0000
ECBh	PSMC2BLKR	Rising Edge Blanking Counter								0000 0000	0000 0000
ECCh	PSMC2BLKF	Falling Edge Blanking Counter								0000 0000	0000 0000
ECDh	PSMC2FFA	—	—	—	—	Fractional Frequency Adjust Register				---- 0000	---- 0000
ECEh	PSMC2STR0	—	—	—	—	—	—	P2STRB	P2STRA	---- --01	---- --01
ECFh	PSMC2STR1	P2SSYNC	—	—	—	—	—	P2LSMEN	P2HSMEN	0--- --00	0--- --00
ED0h	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

6.2 Clock Source Types

Clock sources can be classified as external or internal.

External clock sources rely on external circuitry for the clock source to function. Examples are: oscillator modules (EC mode), quartz crystal resonators or ceramic resonators (LP, XT and HS modes) and Resistor-Capacitor (RC) mode circuits.

Internal clock sources are contained within the oscillator module. The internal oscillator block has two internal oscillators and a dedicated Phase-Lock Loop (HFPLL) that are used to generate three internal system clock sources: the 16 MHz High-Frequency Internal Oscillator (HFINTOSC), 500 kHz (MFINTOSC) and the 31 kHz Low-Frequency Internal Oscillator (LFINTOSC).

The system clock can be selected between external or internal clock sources via the System Clock Select (SCS) bits in the OSCCON register. See **Section 6.3 "Clock Switching"** for additional information.

6.2.1 EXTERNAL CLOCK SOURCES

An external clock source can be used as the device system clock by performing one of the following actions:

- Program the FOSC<2:0> bits in the Configuration Words to select an external clock source that will be used as the default system clock upon a device Reset.
- Write the SCS<1:0> bits in the OSCCON register to switch the system clock source to:
  - Timer1 oscillator during run-time, or
  - An external clock source determined by the value of the FOSC bits.

See **Section 6.3 "Clock Switching"**for more information.

6.2.1.1 EC Mode

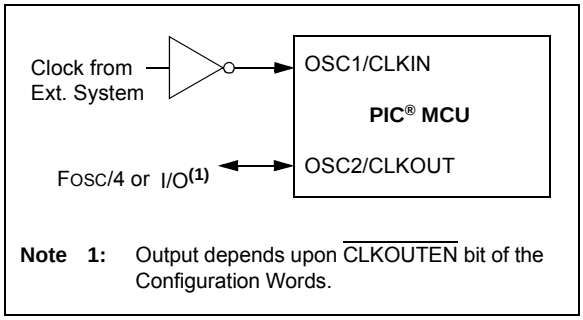
The External Clock (EC) mode allows an externally generated logic level signal to be the system clock source. When operating in this mode, an external clock source is connected to the OSC1 input. OSC2/CLKOUT is available for general purpose I/O or CLKOUT. Figure 6-2 shows the pin connections for EC mode.

EC mode has three power modes to select from through Configuration Words:

- High power, 4-32 MHz (FOSC = 111)
- Medium power, 0.5-4 MHz (FOSC = 110)
- Low power, 0-0.5 MHz (FOSC = 101)

The Oscillator Start-up Timer (OST) is disabled when EC mode is selected. Therefore, there is no delay in operation after a Power-on Reset (POR) or wake-up from Sleep. Because the PIC® MCU design is fully static, stopping the external clock input will have the effect of halting the device while leaving all data intact. Upon restarting the external clock, the device will resume operation as if no time had elapsed.

FIGURE 6-2: EXTERNAL CLOCK (EC) MODE OPERATION



Note 1: Output depends upon $\overline{\text{CLKOUTEN}}$ bit of the Configuration Words.

6.2.1.2 LP, XT, HS Modes

The LP, XT and HS modes support the use of quartz crystal resonators or ceramic resonators connected to OSC1 and OSC2 (Figure 6-3). The three modes select a low, medium or high gain setting of the internal inverter-amplifier to support various resonator types and speed.

LP Oscillator mode selects the lowest gain setting of the internal inverter-amplifier. LP mode current consumption is the least of the three modes. This mode is designed to drive only 32.768 kHz tuning-fork type crystals (watch crystals).

XT Oscillator mode selects the intermediate gain setting of the internal inverter-amplifier. XT mode current consumption is the medium of the three modes. This mode is best suited to drive resonators with a medium drive level specification.

HS Oscillator mode selects the highest gain setting of the internal inverter-amplifier. HS mode current consumption is the highest of the three modes. This mode is best suited for resonators that require a high drive setting.

Figure 6-3 and Figure 6-4 show typical circuits for quartz crystal and ceramic resonators, respectively.

17.3 Register Definitions: ADC Control

REGISTER 17-1: ADCON0: ADC CONTROL REGISTER 0

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **ADRMD:** ADC Result Mode bit
1 = ADRESL and ADRESH provide data formatted for a 10-bit result
0 = ADRESL and ADRESH provide data formatted for a 12-bit result
See Figure 17-3 for details

bit 6-2 **CHS<4:0>:** Positive Differential Input Channel Select bits
11111 = FVR (Fixed Voltage Reference) Buffer 1 Output(3)
11110 = DAC_output(2)
11101 = Temperature Indicator(4)
11100 = DAC2_output(5)
11011 = Reserved
11010 = Reserved
11001 = DAC3_output(5)
11000 = DAC4_output(5)
•
•
•
10110 = Reserved. No channel connected
10101 = AN21(1)
10100 = Reserved. No channel connected
•
•
•
01110 = Reserved. No channel connected.
01101 = AN13
01100 = AN12
01011 = AN11
01010 = AN10
01001 = AN9
01000 = AN8
00111 = AN7(1)
00110 = AN6(1)
00101 = AN5(1)
00100 = AN4
00011 = AN3
00010 = AN2
00001 = AN1
00000 = AN0

bit 1 **GO/$\overline{\text{DONE}}$:** ADC Conversion Status bit
1 = ADC conversion cycle in progress. Setting this bit starts an ADC conversion cycle.
This bit is automatically cleared by hardware when the ADC conversion has completed.
0 = ADC conversion completed/not in progress

bit 0 **ADON:** ADC Enable bit
1 = ADC is enabled
0 = ADC is disabled and consumes no operating current

Note 1: PIC16(L)F1789 only.
2: See **Section 19.0 "8-Bit Digital-to-Analog Converter (DAC) Module"** for more information.
3: See **Section 15.0 "Fixed Voltage Reference (FVR)"** for more information.
4: See **Section 16.0 "Temperature Indicator Module"** for more information.
5: See **Section 20.0 "5-bit Digital-to-Analog Converter (DAC2/3/4) Modules"**for more information.

21.11 Register Definitions: Comparator Control

REGISTER 21-1: CMxCON0: COMPARATOR Cx CONTROL REGISTER 0

R/W-0/0	R-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-0/0
CxON	CxOUT	CxOE	CxPOL	CxZLF	CxSP	CxHYS	CxSYNC
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **CxON:** Comparator Enable bit
1 = Comparator is enabled
0 = Comparator is disabled and consumes no active power

bit 6 **CxOUT:** Comparator Output bit
If CxPOL = 1 (inverted polarity):
1 = CxVP < CxVN
0 = CxVP > CxVN
If CxPOL = 0 (non-inverted polarity):
1 = CxVP > CxVN
0 = CxVP < CxVN

bit 5 **CxOE:** Comparator Output Enable bit
1 = CxOUT is present on the CxOUT pin. Requires that the associated TRIS bit be cleared to actually drive the pin. Not affected by CxON.
0 = CxOUT is internal only

bit 4 **CxPOL:** Comparator Output Polarity Select bit
1 = Comparator output is inverted
0 = Comparator output is not inverted

bit 3 **CxZLF:** Comparator Zero Latency Filter Enable bit
1 = Comparator output is filtered
0 = Comparator output is unfiltered

bit 2 **CxSP:** Comparator Speed/Power Select bit
1 = Comparator operates in normal power, higher speed mode
0 = Comparator operates in low-power, low-speed mode

bit 1 **CxHYS:** Comparator Hysteresis Enable bit
1 = Comparator hysteresis enabled
0 = Comparator hysteresis disabled

bit 0 **CxSYNC:** Comparator Output Synchronous Mode bit
1 = Comparator output to Timer1 and I/O pin is synchronous to changes on Timer1 clock source. Output updated on the falling edge of Timer1 clock source.
0 = Comparator output to Timer1 and I/O pin is asynchronous.

REGISTER 23-2: T1GCON: TIMER1 GATE CONTROL REGISTER

R/W-0/u	R/W-0/u	R/W-0/u	R/W-0/u	R/W/HC-0/u	R-x/x	R/W-0/u	R/W-0/u
TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	HC = Bit is cleared by hardware

bit 7 **TMR1GE:** Timer1 Gate Enable bit

If TMR1ON = 0:
This bit is ignored
If TMR1ON = 1:
1 = Timer1 counting is controlled by the Timer1 gate function
0 = Timer1 counts regardless of Timer1 gate function

bit 6 **T1GPOL:** Timer1 Gate Polarity bit

1 = Timer1 gate is active-high (Timer1 counts when gate is high)
0 = Timer1 gate is active-low (Timer1 counts when gate is low)

bit 5 **T1GTM:** Timer1 Gate Toggle Mode bit

1 = Timer1 Gate Toggle mode is enabled
0 = Timer1 Gate Toggle mode is disabled and toggle flip-flop is cleared
Timer1 gate flip-flop toggles on every rising edge.

bit 4 **T1GSPM:** Timer1 Gate Single-Pulse Mode bit

1 = Timer1 Gate Single-Pulse mode is enabled and is controlling Timer1 gate
0 = Timer1 Gate Single-Pulse mode is disabled

bit 3 **T1GGO/$\overline{\text{DONE}}$:** Timer1 Gate Single-Pulse Acquisition Status bit

1 = Timer1 gate single-pulse acquisition is ready, waiting for an edge
0 = Timer1 gate single-pulse acquisition has completed or has not been started

bit 2 **T1GVAL:** Timer1 Gate Current State bit

Indicates the current state of the Timer1 gate that could be provided to TMR1H:TMR1L.
Unaffected by Timer1 Gate Enable (TMR1GE).

bit 1-0 **T1GSS<1:0>:** Timer1 Gate Source Select bits

11 = Comparator 2 optionally synchronized output (sync_C2OUT)
10 = Comparator 1 optionally synchronized output (sync_C1OUT)
01 = Timer0 overflow output
00 = Timer1 gate pin

26.3.8 PULSE-SKIPPING PWM WITH COMPLEMENTARY OUTPUTS

The pulse-skipping PWM is used to generate a series of fixed-length pulses that may or not be triggered at each period event. If any of the sources enabled to generate a rising edge event are high when a period event occurs, a pulse will be generated. If the rising edge sources are low at the period event, no pulse will be generated.

The rising edge occurs based upon the value in the PSMCxPH register pair.

The falling edge event always occurs according to the enabled event inputs without qualification between any two inputs.

26.3.8.1 Mode Features

- Dead-band control is available
- No steering control available
- Primary PWM is output on only PSMCxA.
- Complementary PWM is output on only PSMCxB.

26.3.8.2 Waveform Generation

Rising Edge Event

If any enabled asynchronous rising edge event = 1 when there is a period event, then upon the next synchronous rising edge event:

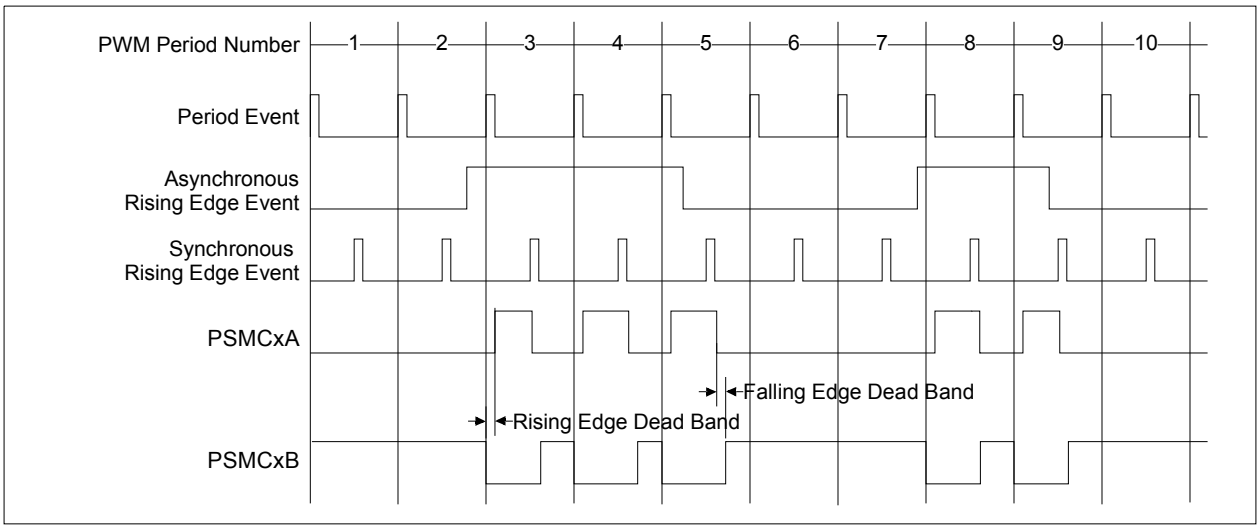
- Complementary output is set inactive
- Dead-band rising is activated (if enabled)
- Primary output is set active

Falling Edge Event

- Primary output is set inactive
- Dead-band falling is activated (if enabled)
- Complementary output is set active

Note:	To use this mode, an external source must be used for the determination of whether or not to generate the set pulse. If the phase time base is used, it will either always generate a pulse or never generate a pulse based on the PSMCxPH value.

FIGURE 26-11: PULSE-SKIPPING WITH COMPLEMENTARY OUTPUT PWM WAVEFORM



26.7 Auto-Shutdown

Auto-shutdown is a method to immediately override the PSMC output levels with specific overrides that allow for safe shutdown of the application.

Auto-shutdown includes a mechanism to allow the application to restart under different conditions.

Auto-shutdown is enabled with the PxASDEN bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 26-16). All auto-shutdown features are enabled when PxASDEN is set and disabled when cleared.

26.7.1 SHUTDOWN

There are two ways to generate a shutdown event:

- Manual
- External Input

26.7.1.1 Manual Override

The auto-shutdown control register can be used to manually override the pin functions. Setting the PxASE bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 26-16) generates a software shut-down event.

The auto-shutdown override will persist as long as PxASE remains set.

26.7.1.2 External Input Source

Any of the given sources that are available for event generation are also available for system shut-down. This is so that external circuitry can monitor and force a shutdown without any software overhead. Auto-shutdown sources are selected with the PSMC Auto-shutdown Source (PSMCxASDS) register (Register 26-18).

When any of the selected external auto-shutdown sources go high, the PxASE bit is set and an auto-shutdown interrupt is generated.

Note:	The external shutdown sources are level sensitive, not edge sensitive. The shutdown condition will persist as long as the circuit is driving the appropriate logic level.

26.7.2 PIN OVERRIDE LEVELS

The logic levels driven to the output pins during an auto-shutdown event are determined by the PSMC Auto-shutdown Output Level (PSMCxASDL) register (Register 26-17).

26.7.2.1 PIN Override Enable

Setting the PxASDOV bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 26-16) will also force the override levels onto the pins, exactly like what happens when the auto-shutdown is used. However, whereas setting PxASE causes an auto-shutdown interrupt, setting PxASDOV does not generate an interrupt.

26.7.3 RESTART FROM AUTO-SHUTDOWN

After an auto-shutdown event has occurred, there are two ways for the module to resume operation:

- Manual restart
- Automatic restart

The restart method is selected with the PxARSEN bit of the PSMC Auto-shutdown Control (PSMCxASDC) register (Register 26-16).

26.7.3.1 Manual Restart

When PxARSEN is cleared, and once the PxASDE bit is set, it will remain set until cleared by software.

The PSMC will restart on the period event after PxASDE bit is cleared in software.

26.7.3.2 Auto-Restart

When PxARSEN is set, the PxASDE bit will clear automatically when the source causing the Reset and no longer asserts the shut-down condition.

The PSMC will restart on the next period event after the auto-shutdown condition is removed.

Examples of manual and automatic restart are shown in Figure 26-20.

Note:	Whether manual or auto-restart is selected, the PxASDE bit cannot be cleared in software when the auto-shutdown condition is still present.

REGISTER 26-3: PSMC1SYNC: PSMC1 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P1POFST	P1PRPOL	P1DCPOL	—	—	P1SYNC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P1POFST:** PSMC1 Phase Offset Control bit
- 1 = sync_out source is phase event and latch set source is synchronous period event
- 0 = sync_out source is period event and latch set source is phase event

bit 6 **P1PRPOL:** PSMC1 Period Polarity Event Control bit
- 1 = Selected asynchronous period event inputs are inverted
- 0 = Selected asynchronous period event inputs are not inverted

bit 5 **P1DCPOL:** PSMC1 Duty-cycle Event Polarity Control bit
- 1 = Selected asynchronous duty-cycle event inputs are inverted
- 0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **P1SYNC<2:0>:** PSMC1 Period Synchronization Mode bits
- 1xx = Reserved - Do not use
- 100 = PSMC1 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)
- 011 = PSMC1 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
- 010 = PSMC1 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)
- 001 = PSMC1 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)
- 000 = PSMC1 is synchronized with period event

REGISTER 26-4: PSMC2SYNC: PSMC2 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P2POFST	P2PRPOL	P2DCPOL	—	—	P2SYNC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P2POFST:** PSMC2 Phase Offset Control bit
- 1 = sync_out source is phase event and latch set source is synchronous period event
- 0 = sync_out source is period event and latch set source is phase event

bit 6 **P2PRPOL:** PSMC2 Period Polarity Event Control bit
- 1 = Selected asynchronous period event inputs are inverted
- 0 = Selected asynchronous period event inputs are not inverted

bit 5 **P2DCPOL:** PSMC2 Duty-cycle Event Polarity Control bit
- 1 = Selected asynchronous duty-cycle event inputs are inverted
- 0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **P2SYNC<2:0>:** PSMC2 Period Synchronization Mode bits
- 1xx = Reserved - Do not use
- 100 = PSMC2 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)
- 011 = PSMC2 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
- 010 = PSMC2 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)
- 001 = PSMC2 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)
- 000 = PSMC2 is synchronized with period event

27.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

27.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)

The SPI interface supports the following modes and features:

- Master mode
- Slave mode
- Clock Parity
- Slave Select Synchronization (Slave mode only)
- Daisy-chain connection of slave devices

Figure 27-1 is a block diagram of the SPI interface module.

FIGURE 27-1: MSSP BLOCK DIAGRAM (SPI MODE)

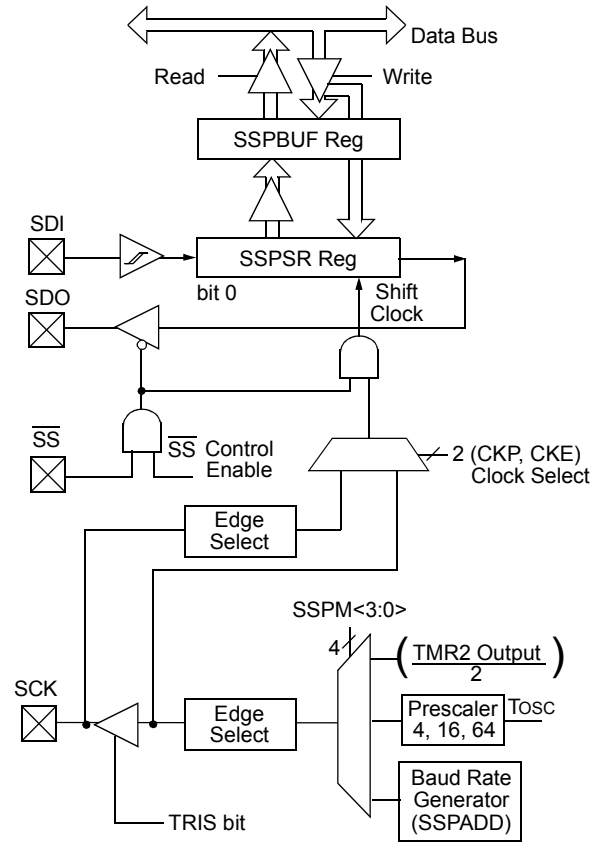
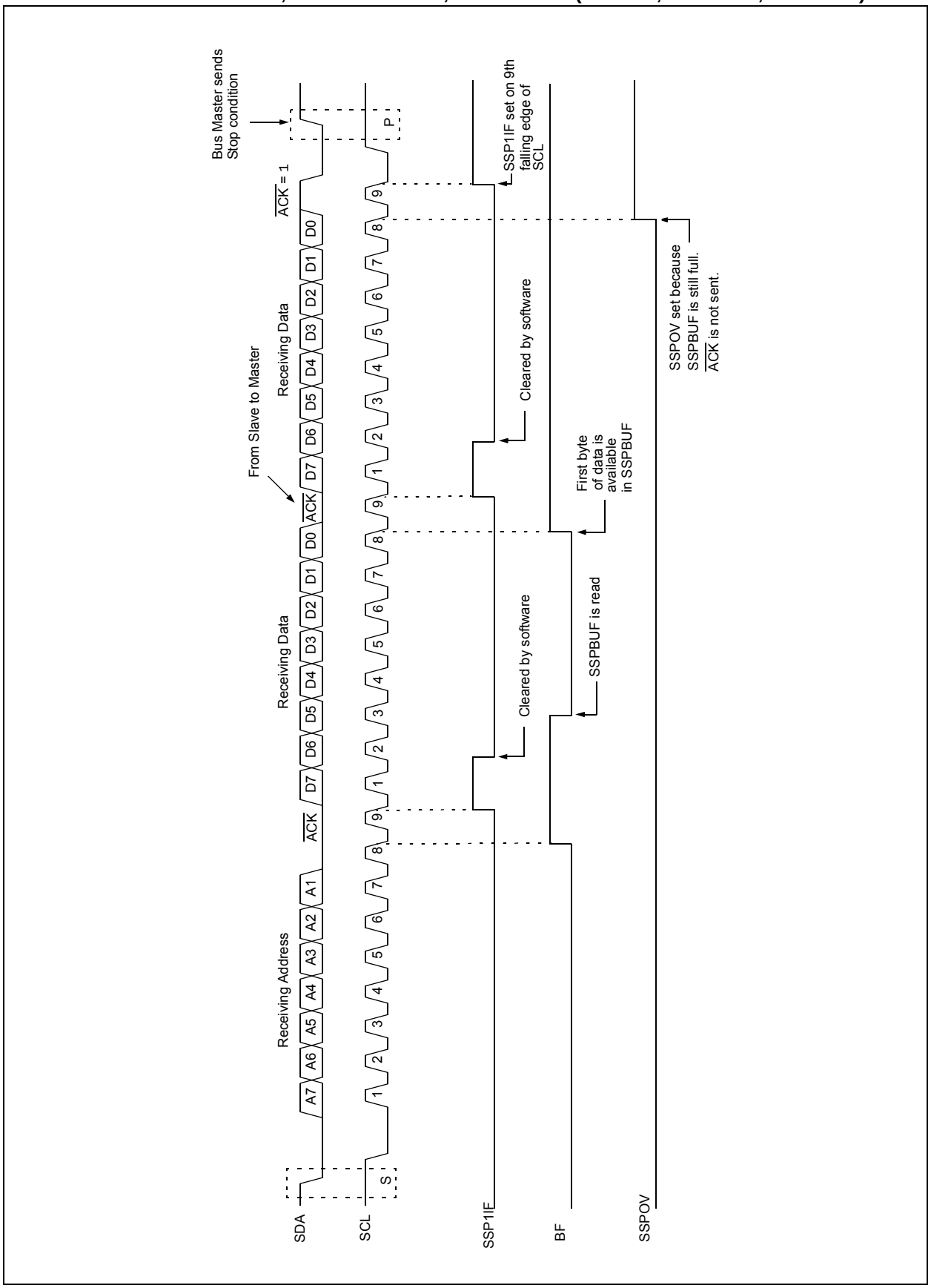


FIGURE 27-14: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 0, AHEN = 0, DHEN = 0)



27.6.7 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

Note:	The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

27.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

27.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

27.6.7.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

27.6.7.4 Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/$\overline{W}$ bit set.
5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the $\overline{ACK}$ bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
8. User sets the RCEN bit of the SSPCON2 register and the master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSP1IF and BF are set.
10. User clears the SSP1IF bit and reads the received byte from SSPUF, which clears the BF flag.
11. The user either clears the SSPCON2 register's ACKDT bit to receive another byte or sets the ADKDT bit to suppress further data and then initiates the acknowledge sequence by setting the ACKEN bit.
12. Master's ACK or $\overline{ACK}$ is clocked out to the slave and SSP1IF is set.
13. User clears SSP1IF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. If the ACKST bit was set in step 11 then the user can send a STOP to release the bus.

TABLE 28-5: BAUD RATES FOR ASYNCHRONOUS MODES

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	1221	1.73	255	1200	0.00	239	1200	0.00	143
2400	2404	0.16	207	2404	0.16	129	2400	0.00	119	2400	0.00	71
9600	9615	0.16	51	9470	-1.36	32	9600	0.00	29	9600	0.00	17
10417	10417	0.00	47	10417	0.00	29	10286	-1.26	27	10165	-2.42	16
19.2k	19.23k	0.16	25	19.53k	1.73	15	19.20k	0.00	14	19.20k	0.00	8
57.6k	55.55k	-3.55	3	—	—	—	57.60k	0.00	7	57.60k	0.00	2
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 0											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	300	0.16	207	300	0.00	191	300	0.16	51
1200	1202	0.16	103	1202	0.16	51	1200	0.00	47	1202	0.16	12
2400	2404	0.16	51	2404	0.16	25	2400	0.00	23	—	—	—
9600	9615	0.16	12	—	—	—	9600	0.00	5	—	—	—
10417	10417	0.00	11	10417	0.00	5	—	—	—	—	—	—
19.2k	—	—	—	—	—	—	19.20k	0.00	2	—	—	—
57.6k	—	—	—	—	—	—	57.60k	0.00	0	—	—	—
115.2k	—	—	—	—	—	—	—	—	—	—	—	—

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 0											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	—	—	—
1200	—	—	—	—	—	—	—	—	—	—	—	—
2400	—	—	—	—	—	—	—	—	—	—	—	—
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.82k	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.64k	2.12	16	113.64k	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

TABLE 28-5: BAUD RATES FOR ASYNCHRONOUS MODES (CONTINUED)

BAUD RATE	SYNC = 0, BRGH = 1, BRG16 = 0											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	—	—	—	—	—	—	—	—	—	300	0.16	207
1200	—	—	—	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19231	0.16	25	19.23k	0.16	12	19.2k	0.00	11	—	—	—
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—
115.2k	—	—	—	—	—	—	115.2k	0.00	1	—	—	—

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 32.000 MHz			Fosc = 20.000 MHz			Fosc = 18.432 MHz			Fosc = 11.0592 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	300.0	0.00	6666	300.0	-0.01	4166	300.0	0.00	3839	300.0	0.00	2303
1200	1200	-0.02	3332	1200	-0.03	1041	1200	0.00	959	1200	0.00	575
2400	2401	-0.04	832	2399	-0.03	520	2400	0.00	479	2400	0.00	287
9600	9615	0.16	207	9615	0.16	129	9600	0.00	119	9600	0.00	71
10417	10417	0.00	191	10417	0.00	119	10378	-0.37	110	10473	0.53	65
19.2k	19.23k	0.16	103	19.23k	0.16	64	19.20k	0.00	59	19.20k	0.00	35
57.6k	57.14k	-0.79	34	56.818	-1.36	21	57.60k	0.00	19	57.60k	0.00	11
115.2k	117.6k	2.12	16	113.636	-1.36	10	115.2k	0.00	9	115.2k	0.00	5

BAUD RATE	SYNC = 0, BRGH = 0, BRG16 = 1											
	Fosc = 8.000 MHz			Fosc = 4.000 MHz			Fosc = 3.6864 MHz			Fosc = 1.000 MHz		
	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)	Actual Rate	% Error	SPBRG value (decimal)
300	299.9	-0.02	1666	300.1	0.04	832	300.0	0.00	767	300.5	0.16	207
1200	1199	-0.08	416	1202	0.16	207	1200	0.00	191	1202	0.16	51
2400	2404	0.16	207	2404	0.16	103	2400	0.00	95	2404	0.16	25
9600	9615	0.16	51	9615	0.16	25	9600	0.00	23	—	—	—
10417	10417	0.00	47	10417	0.00	23	10473	0.53	21	10417	0.00	5
19.2k	19.23k	0.16	25	19.23k	0.16	12	19.20k	0.00	11	—	—	—
57.6k	55556	-3.55	8	—	—	—	57.60k	0.00	3	—	—	—
115.2k	—	—	—	—	—	—	115.2k	0.00	1	—	—	—

28.5.2 SYNCHRONOUS SLAVE MODE

The following bits are used to configure the EUSART for synchronous slave operation:

- SYNC = 1
- CSRC = 0
- SREN = 0 (for transmit); SREN = 1 (for receive)
- CREN = 0 (for transmit); CREN = 1 (for receive)
- SPEN = 1

Setting the SYNC bit of the TXSTA register configures the device for synchronous operation. Clearing the CSRC bit of the TXSTA register configures the device as a slave. Clearing the SREN and CREN bits of the RCSTA register ensures that the device is in the Transmit mode, otherwise the device will be configured to receive. Setting the SPEN bit of the RCSTA register enables the EUSART.

28.5.2.1 EUSART Synchronous Slave Transmit

The operation of the Synchronous Master and Slave modes are identical (see **Section 28.5.1.3 "Synchronous Master Transmission")**, except in the case of the Sleep mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

1. The first character will immediately transfer to the TSR register and transmit.
2. The second word will remain in TXREG register.
3. The TXIF bit will not be set.
4. After the first character has been shifted out of TSR, the TXREG register will transfer the second character to the TSR and the TXIF bit will now be set.
5. If the PEIE and TXIE bits are set, the interrupt will wake the device from Sleep and execute the next instruction. If the GIE bit is also set, the program will call the Interrupt Service Routine.

28.5.2.2 Synchronous Slave Transmission Set-up:

1. Set the SYNC and SPEN bits and clear the CSRC bit.
2. Clear the ANSEL bit for the CK pin (if applicable).
3. Clear the CREN and SREN bits.
4. If interrupts are desired, set the TXIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
5. If 9-bit transmission is desired, set the TX9 bit.
6. Enable transmission by setting the TXEN bit.
7. If 9-bit transmission is selected, insert the Most Significant bit into the TX9D bit.
8. Start transmission by writing the Least Significant eight bits to the TXREG register.

TABLE 28-9: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	132
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	356
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	355
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	147
TXREG	EUSART Transmit Data Register								346*
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	354

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous slave transmission.

* Page provides register information.

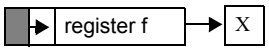
ADDWF	Add W and f
Syntax:	[*label*] ADDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) → (destination)
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ADDWFC	ADD W and CARRY bit to f
Syntax:	[*label*] ADDWFC f {,d}
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) + (f) + (C) → dest
Status Affected:	C, DC, Z
Description:	Add W, the Carry flag and data memory location 'f'. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is placed in data memory location 'f'.

ANDLW	AND literal with W
Syntax:	[*label*] ANDLW k
Operands:	$0 \le k \le 255$
Operation:	(W) .AND. (k) → (W)
Status Affected:	Z
Description:	The contents of W register are AND'ed with the 8-bit literal 'k'. The result is placed in the W register.

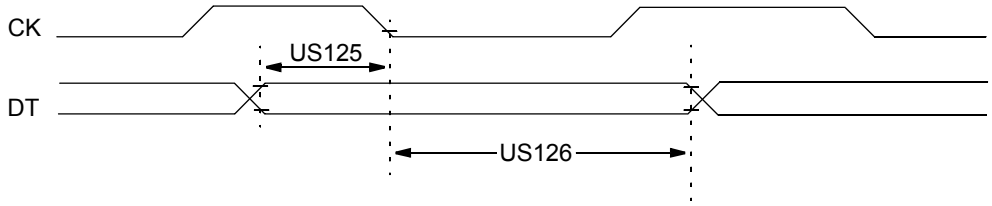
ANDWF	AND W with f
Syntax:	[*label*] ANDWF f,d
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(W) .AND. (f) → (destination)
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is '0', the result is stored in the W register. If 'd' is '1', the result is stored back in register 'f'.

ASRF	Arithmetic Right Shift
Syntax:	[*label*] ASRF f {,d}
Operands:	$0 \le f \le 127$ $d \in [0,1]$
Operation:	(f<7>)→ dest<7> (f<7:1>) → dest<6:0>, (f<0>) → C,
Status Affected:	C, Z
Description:	The contents of register 'f' are shifted one bit to the right through the Carry flag. The MSb remains unchanged. If 'd' is '0', the result is placed in W. If 'd' is '1', the result is stored back in register 'f'.



BCF	Bit Clear f
Syntax:	[*label*] BCF f,b
Operands:	$0 \le f \le 127$ $0 \le b \le 7$
Operation:	0 → (f<b>)
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

FIGURE 31-15: EUSART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING



Note: Refer to Figure 31-4 for load conditions.

TABLE 31-20: EUSART SYNCHRONOUS RECEIVE REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)						
Param. No.	**Symbol**	**Characteristic**	**Min.**	**Max.**	**Units**	**Conditions**
US125	TDTV2CKL	SYNC RCV (Master and Slave) Data-hold before CK ↓ (DT hold time)	10	—	ns	
US126	TCKL2DTL	Data-hold after CK ↓ (DT hold time)	15	—	ns	

Note the following details of the code protection feature on Microchip devices:

- Microchip products meet the specification contained in their particular Microchip Data Sheet.
- Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.
- There are dishonest and possibly illegal methods used to breach the code protection feature. All of these methods, to our knowledge, require using the Microchip products in a manner outside the operating specifications contained in Microchip's Data Sheets. Most likely, the person doing so is engaged in theft of intellectual property.
- Microchip is willing to work with the customer who is concerned about the integrity of their code.
- Neither Microchip nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Code protection is constantly evolving. We at Microchip are committed to continuously improving the code protection features of our products. Attempts to break Microchip's code protection feature may be a violation of the Digital Millennium Copyright Act. If such acts allow unauthorized access to your software or other copyrighted work, you may have a right to sue for relief under that Act.

ISBN: 978-1-5224-0058-5

QUALITY MANAGEMENT SYSTEM
CERTIFIED BY DNV
═ ISO/TS 16949 ═

Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC® MCUs and dsPIC® DSCs, KEELOQ® code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.