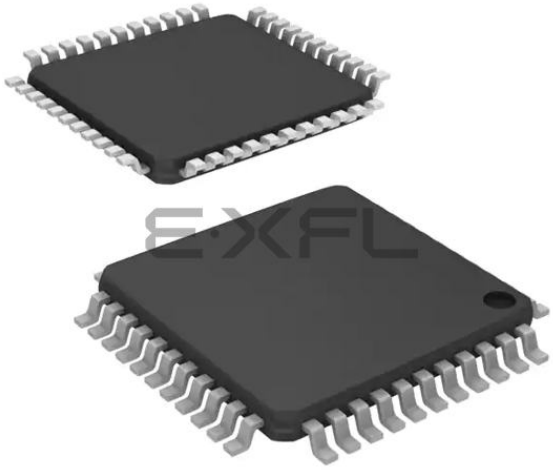

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Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	2.3V ~ 5.5V
Data Converters	A/D 14x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16f1789t-i-pt

TABLE 1-2: PIC16(L)F1788 PINOUT DESCRIPTION (CONTINUED)

Name	Function	Input Type	Output Type	Description
RB4/AN11/C3IN1+/$\overline{SS}$(1)	RB4	TTL/ST	CMOS	General purpose I/O.
	AN11	AN	—	ADC Channel 11 input.
	C3IN1+	AN	—	Comparator C3 positive input.
	$\overline{SS}$	ST	—	Slave Select input.
RB5/AN13/C4IN2-/T1G/CCP3(1) SDO(1)/C3OUT	RB5	TTL/ST	CMOS	General purpose I/O.
	AN13	AN	—	ADC Channel 13 input.
	C4IN2-	AN	—	Comparator C4 negative input.
	T1G	ST	—	Timer1 gate input.
	CCP3	ST	CMOS	Capture/Compare/PWM3.
	SDO	—	CMOS	SPI data output.
	C3OUT	—	CMOS	Comparator C3 output.
RB6/C4IN1+/TX(1)/CK(1)/SDI(1)/ SDA(1)/ICSPCLK	RB6	TTL/ST	CMOS	General purpose I/O.
	C4IN1+	AN	—	Comparator C4 positive input.
	TX	—	CMOS	EUSART asynchronous transmit.
	CK	ST	CMOS	EUSART synchronous clock.
	SDI	ST	—	SPI data input.
	SDA	I^2C	OD	I^2C data input/output.
	ICSPCLK	ST	—	Serial Programming Clock.
RB7/DAC1OUT2/DAC2OUT2/ DAC3OUT2/DAC4OUT2/RX(1)/ DT(1)/SCK(1)/SCL(1)/ICSPDAT	RB7	TTL/ST	CMOS	General purpose I/O.
	DAC1OUT2	—	AN	Voltage Reference output.
	DAC2OUT2	—	AN	Voltage Reference output.
	DAC3OUT2	—	AN	Voltage Reference output.
	DAC4OUT2	—	AN	Voltage Reference output.
	RX	ST	—	EUSART asynchronous input.
	DT	ST	CMOS	EUSART synchronous data.
	SCK	ST	CMOS	SPI clock.
	SCL	I^2C	OD	I^2C clock.
	ICSPDAT	ST	CMOS	ICSP™ Data I/O.
RC0/T1OSO/T1CKI/PSMC1A	RC0	TTL/ST	CMOS	General purpose I/O.
	T1OSO	XTAL	XTAL	Timer1 Oscillator Connection.
	T1CKI	ST	—	Timer1 clock input.
	PSMC1A	—	CMOS	PSMC1 output A.
RC1/T1OSI/PSMC1B/CCP2	RC1	TTL/ST	CMOS	General purpose I/O.
	T1OSI	XTAL	XTAL	Timer1 Oscillator Connection.
	PSMC1B	—	CMOS	PSMC1 output B.
	CCP2	ST	CMOS	Capture/Compare/PWM2.
RC2/PSMC1C/PSMC3B/CCP1	RC2	TTL/ST	CMOS	General purpose I/O.
	PSMC1C	—	CMOS	PSMC1 output C.
	PSMC3B	—	CMOS	PSMC3 output B.
	CCP1	ST	CMOS	Capture/Compare/PWM1.

Legend: AN = Analog input or output CMOS = CMOS compatible input or output OD = Open-Drain
TTL = TTL compatible input ST = Schmitt Trigger input with CMOS levels I^2C = Schmitt Trigger input with I^2C
HV = High Voltage XTAL = Crystal levels

Note 1: Pin functions can be assigned to one of two locations via software. See **Register 13-1**.
2: All pins have interrupt-on-change functionality.

TABLE 3-12: SPECIAL FUNCTION REGISTER SUMMARY (CONTINUED)

Addr	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other Resets
Bank 11-15											
58Ch — 590h	—	Unimplemented								—	—
591h	DAC2CON0	DAC2EN	---	DAC2OE1	DAC2OE2	DAC2PSS<1:0>		---	---	0-00 00--	0-00 00--
592h	DAC2CON1	---	---	---	DAC2R<4:0>					---0 0000	---0 0000
593h	DAC3CON0	DAC3EN	---	DAC3OE1	DAC3OE2	DAC3PSS<1:0>		---	---	0-00 00--	0-00 00--
594h	DAC3CON1	---	---	---	DAC3R<4:0>					---0 0000	---0 0000
595h	DAC4CON0	DAC4EN	---	DAC4OE1	DAC4OE2	DAC4PSS<1:0>		---	---	0-00 00--	0-00 00--
596h	DAC4CON1	---	---	---	DAC4R<4:0>					---0 0000	---0 0000
597h — 59Fh	—	Unimplemented								—	—
Bank 16-28											
x0Ch or x8Ch to x1Fh or x9Fh	—	Unimplemented								—	—

Legend: x = unknown, u = unchanged, q = value depends on condition, - = unimplemented, read as '0', r = reserved. Shaded locations are unimplemented, read as '0'.

Note 1: These registers can be addressed from any bank.
2: Unimplemented, read as '1'.
3: PIC16(L)F1789 only.
4: PIC16F1788/9 only.

FIGURE 3-5: ACCESSING THE STACK EXAMPLE 2

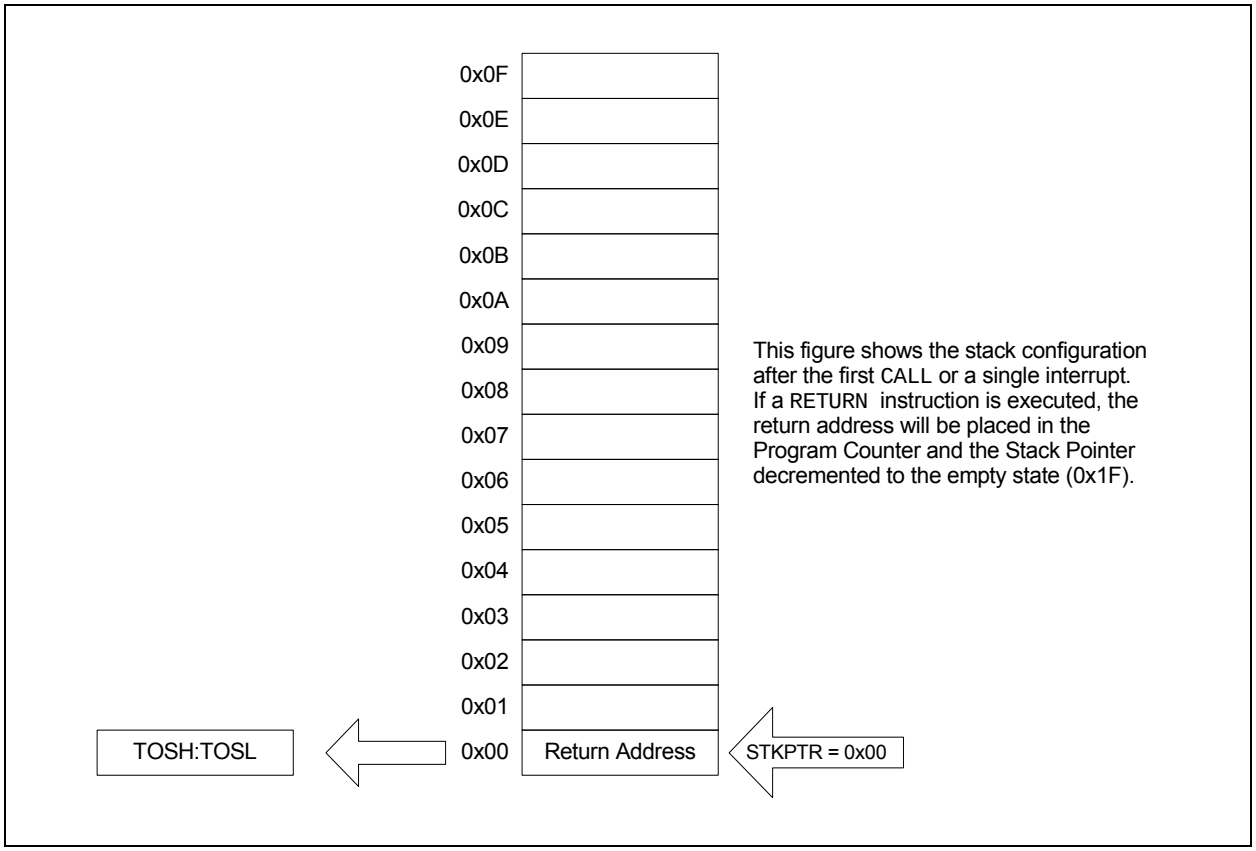
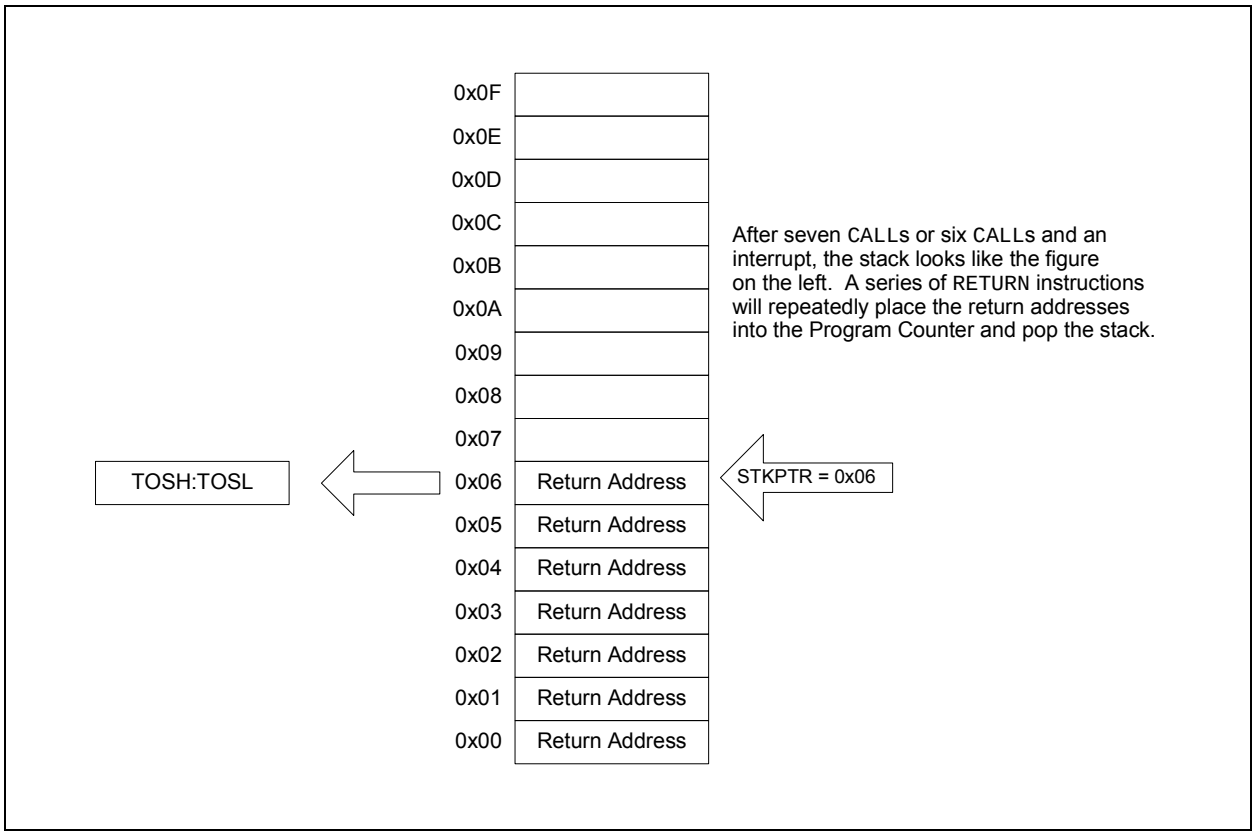


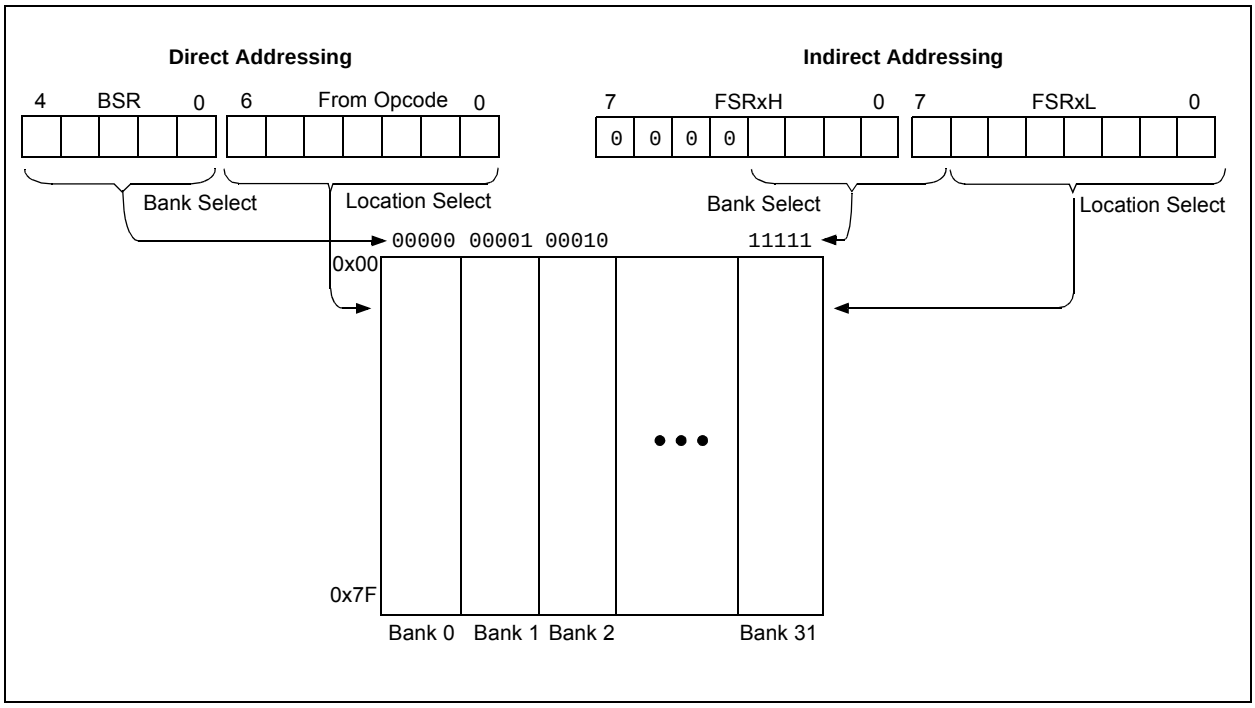
FIGURE 3-6: ACCESSING THE STACK EXAMPLE 3



3.6.1 TRADITIONAL DATA MEMORY

The traditional data memory is a region from FSR address 0x000 to FSR address 0xFFF. The addresses correspond to the absolute addresses of all SFR, GPR and common registers.

FIGURE 3-9: TRADITIONAL DATA MEMORY MAP



6.2.1.4 4x PLL

The oscillator module contains a 4x PLL that can be used with both external and internal clock sources to provide a system clock source. The input frequency for the 4x PLL must fall within specifications. See the PLL Clock Timing Specifications in **Section 30.0 "Electrical Specifications"**.

The 4x PLL may be enabled for use by one of two methods:

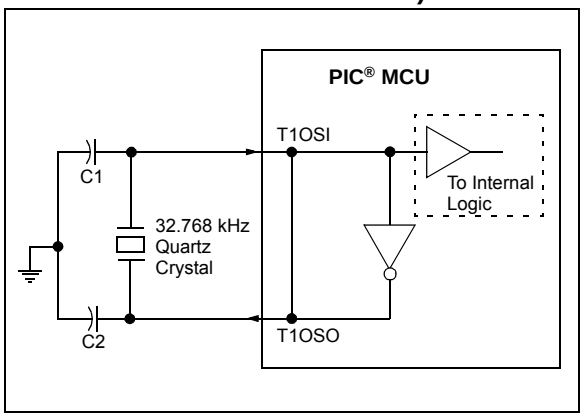
1. Program the PLLEN bit in Configuration Words to a '1'.
2. Write the SPLLEN bit in the OSCCON register to a '1'. If the PLLEN bit in Configuration Words is programmed to a '1', then the value of SPLLEN is ignored.

6.2.1.5 TIMER1 Oscillator

The Timer1 oscillator is a separate crystal oscillator that is associated with the Timer1 peripheral. It is optimized for timekeeping operations with a 32.768 kHz crystal connected between the T1OSO and T1OSI device pins.

The Timer1 oscillator can be used as an alternate system clock source and can be selected during run-time using clock switching. Refer to **Section 6.3 "Clock Switching"** for more information.

FIGURE 6-5: QUARTZ CRYSTAL OPERATION (TIMER1 OSCILLATOR)



Note 1:	Quartz crystal characteristics vary according to type, package and manufacturer. The user should consult the manufacturer data sheets for specifications and recommended application.
2:	Always verify oscillator performance over the V_{DD} and temperature range that is expected for the application.
3:	For oscillator design assistance, reference the following Microchip Applications Notes: • AN826, "*Crystal Oscillator Basics and Crystal Selection for rfPIC® and PIC® Devices*" (DS00826) • AN849, "*Basic PIC® Oscillator Design*" (DS00849) • AN943, "*Practical PIC® Oscillator Analysis and Design*" (DS00943) • AN949, "*Making Your Oscillator Work*" (DS00949) • TB097, "*Interfacing a Micro Crystal MS1V-T1K 32.768 kHz Tuning Fork Crystal to a PIC16F690/SS*" (DS91097) • AN1288, "*Design Practices for Low-Power External Oscillators*" (DS01288)

10.0 LOW DROPOUT (LDO) VOLTAGE REGULATOR

The “F” devices have an internal Low Dropout Regulator (LDO) which provide operation above 3.6V. The LDO regulates a voltage for the internal device logic while permitting the VDD and I/O pins to operate at a higher voltage. There is no user enable/disable control available for the LDO, it is always active. The “LF” devices operate at a maximum VDD of 3.6V and does not incorporate an LDO.

A device I/O pin may be configured as the LDO voltage output, identified as the VCAP pin. Although not required, an external low-ESR capacitor may be connected to the VCAP pin for additional regulator stability.

The $\overline{\text{VCAPEN}}$ bit of Configuration Words determines if which pin is assigned as the VCAP pin. Refer to Table 10-1.

TABLE 10-1: $\overline{\text{VCAPEN}}$ SELECT BIT

$\overline{\text{VCAPEN}}$	Pin
1	No VCAP
0	RA6

On power-up, the external capacitor will load the LDO voltage regulator. To prevent erroneous operation, the device is held in Reset while a constant current source charges the external capacitor. After the cap is fully charged, the device is released from Reset. For more information on the constant current rate, refer to the LDO Regulator Characteristics Table in **Section 31.0 “Electrical Specifications”**.

TABLE 10-2: SUMMARY OF CONFIGURATION WORD WITH LDO

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG2	13:8	—	—	LVP	$\overline{\text{DEBUG}}$	$\overline{\text{LPBOR}}$	BORV	STVREN	PLLEN	60
	7:0	—	—	$\overline{\text{VCAPEN}}$(1)	—	—	—	WRT<1:0>		

Legend: — = unimplemented locations read as ‘0’. Shaded cells are not used by LDO.

Note 1: “F” devices only.

TABLE 17-3: SUMMARY OF REGISTERS ASSOCIATED WITH ADC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ADCON0	ADRMD	CHS<4:0>					GO/$\overline{\text{DONE}}$	ADON	177
ADCON1	ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>		178
ADCON2	TRIGSEL<3:0>				CHSN<3:0>				179
ADRESH	A/D Result Register High								180, 181
ADRESL	A/D Result Register Low								180, 181
ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	137
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	143
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	136
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	142
FVRCON	FVREN	FVRRDY	TSEN	TSRNG	CDAFVR<1:0>		ADFVR<1:0>		167

Legend: x = unknown, u = unchanged, – = unimplemented read as '0', q = value depends on condition. Shaded cells are not used for the ADC module.

FIGURE 20-1: DIGITAL-TO-ANALOG CONVERTER BLOCK DIAGRAM

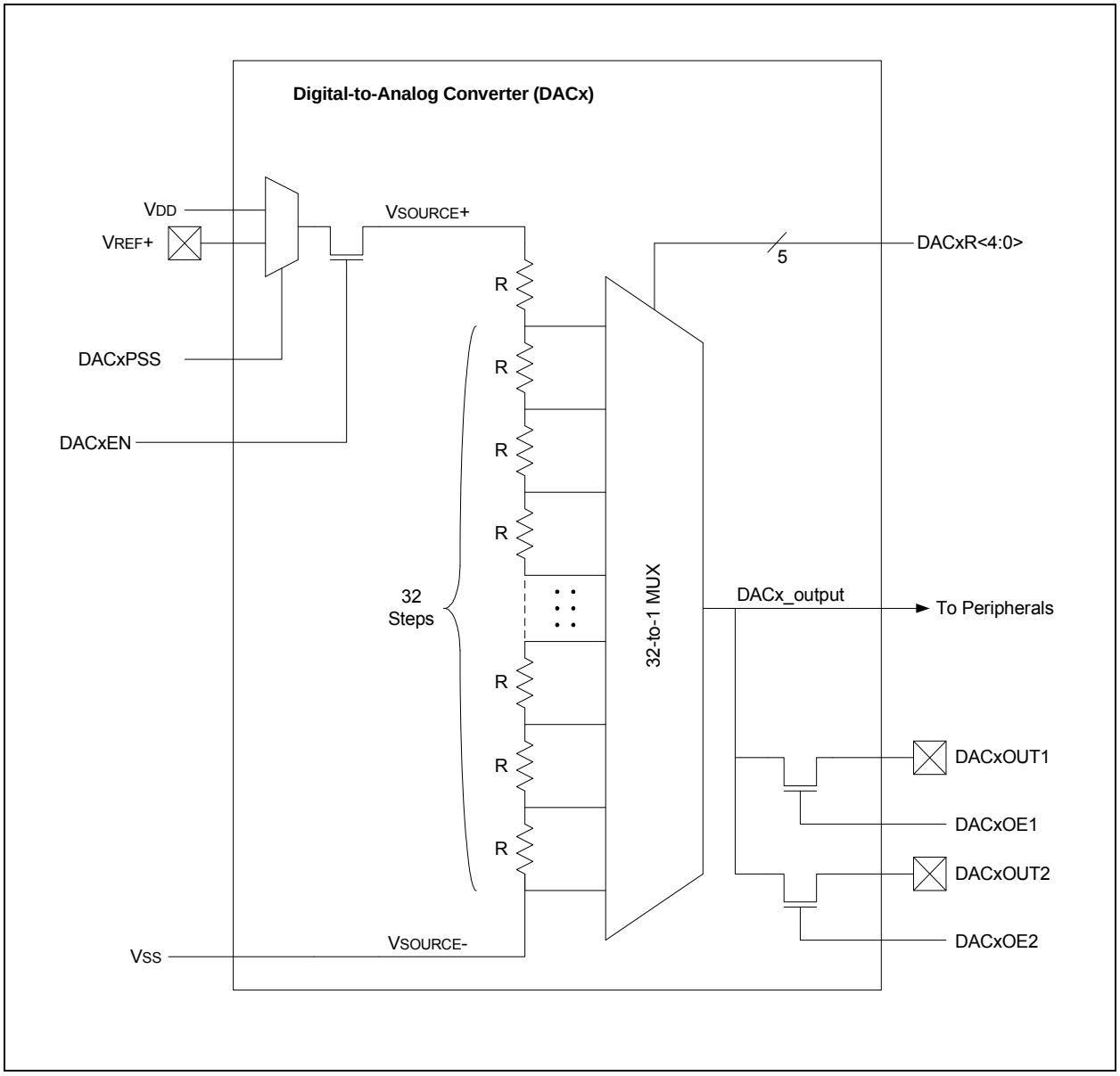
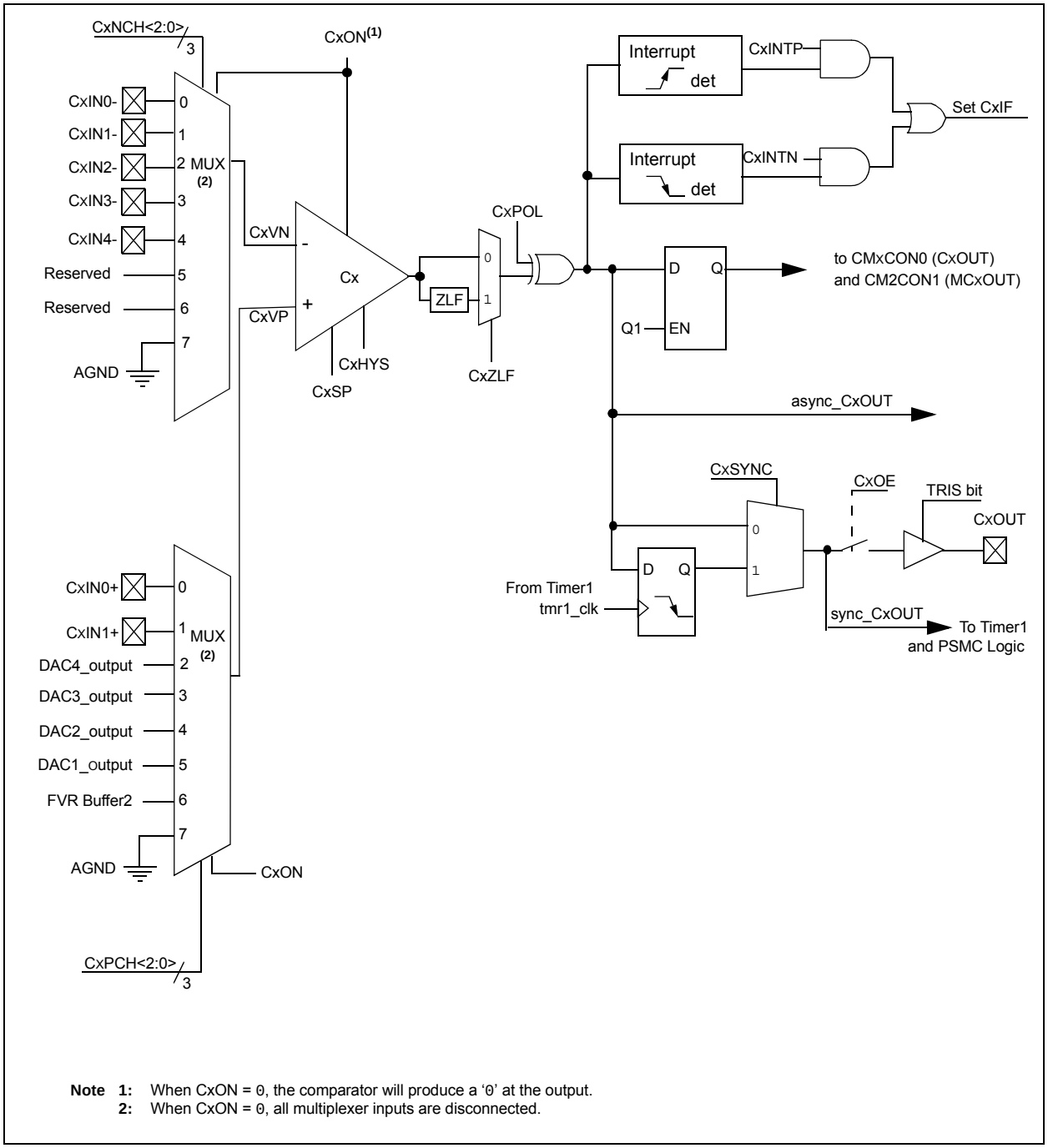


FIGURE 21-2: COMPARATOR MODULE SIMPLIFIED BLOCK DIAGRAM



Note 1: When CxON = 0, the comparator will produce a '0' at the output.
2: When CxON = 0, all multiplexer inputs are disconnected.

TABLE 23-5: SUMMARY OF REGISTERS ASSOCIATED WITH TIMER1

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	143
CCP1CON	—	—	DC1B<1:0>		CCP1M<3:0>				231
CCP2CON	—	—	DC2B<1:0>		CCP2M<3:0>				231
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								209*
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								209*
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	142
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	147
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	$\overline{\text{T1SYNC}}$	—	TMR1ON	217
T1GCON	TMR1GE	T1GPOL	T1GTM	T1GSPM	T1GGO/$\overline{\text{DONE}}$	T1GVAL	T1GSS<1:0>		218

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by the Timer1 module.

* Page provides register information.

26.2.1.4 16-bit Duty Cycle Register

The PSMCxDC Duty Cycle register is used to determine a synchronous falling edge event referenced to the 16-bit PSMCxTMR digital counter. A match between the PSMCxTMR and PSMCxDC register values will generate a falling edge event.

The match will generate a duty cycle match interrupt, thereby setting the PxTDCIF bit of the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 26-34).

The 16-bit duty cycle value is accessible to software as two 8-bit registers:

- PSMC Duty Cycle Count Low Byte (PSMCxDCL) register (Register 26-23)
- PSMC Duty Cycle Count High Byte (PSMCxDCH) register (Register 26-24)

The 16-bit duty cycle value is double-buffered before it is presented to the 16-bit time base for comparison. The buffered registers are updated on the first period event Reset after the PSMCxLD bit of the PSMCxCON register is set.

When the period, phase, and duty cycle are all determined from the time base, the effective PWM duty cycle can be expressed as shown in Equation 26-2.

EQUATION 26-2: PWM DUTY CYCLE

$$DUTYCYCLE = \frac{\text{PSMCxDC[15:0]} - \text{PSMCxPH[15:0]}}{(\text{PSMCxPR[15:0]} + 1)}$$

26.2.2 0% DUTY CYCLE OPERATION USING TIME BASE

To configure the PWM for 0% duty cycle set PSMCxDC<15:0> = PSMCxPH<15:0>. This will trigger a falling edge event simultaneous with the rising edge event and prevent the PWM from being asserted.

26.2.3 100% DUTY CYCLE OPERATION USING TIME BASE

To configure the PWM for 100% duty cycle set PSMCxDC<15:0> > PSMCxPR<15:0>.

This will prevent a falling edge event from occurring as the PSMCxDC<15:0> value and the time base value PSMCxTMR<15:0> will never be equal.

26.2.4 TIME BASE INTERRUPT GENERATION

The Time Base section can generate four unique interrupts:

- Time Base Counter Overflow Interrupt
- Time Base Phase Register Match Interrupt
- Time Base Duty Cycle Register Match Interrupt
- Time Base Period Register Match Interrupt

Each interrupt has an interrupt flag bit and an interrupt enable bit. The interrupt flag bit is set anytime a given event occurs, regardless of the status of the enable bit.

Time base interrupt enables and flags are located in the PSMC Time Base Interrupt Control (PSMCxINT) register (Register 26-34).

PSMC time base interrupts also require that the PSMCxTIE bit in the PIE4 register and the PEIE and GIE bits in the INTCON register be set in order to generate an interrupt. The PSMCxTIF interrupt flag in the PIR4 register will only be set by a time base interrupt when one or more of the enable bits in the PSMCxINT register is set.

The interrupt flag bits need to be cleared in software. However, all PMSCx time base interrupt flags, except PSMCxTIF, are cleared when the PSMCxEN bit is cleared.

Interrupt bits that are set by software will generate an interrupt provided that the corresponding interrupt is enabled.

Note:	Interrupt flags in both the PIE4 and PSMCxINT registers must be cleared to clear the interrupt. The PSMCxINT flags must be cleared first.

26.2.5 PSMC TIME BASE CLOCK SOURCES

There are three clock sources available to the module:

- Internal 64 MHz clock
- Fosc system clock
- External clock input pin

The clock source is selected with the PxCSRC<1:0> bits of the PSMCx Clock Control (PSMCxCLK) register (Register 26-7).

When the Internal 64 MHz clock is selected as the source, the HFINTOSC continues to operate and clock the PSMC circuitry in Sleep. However, the system clock to other peripherals and the CPU is suppressed.

Note:	When the 64 MHz clock is selected, the clock continues to operate in Sleep, even when the PSMC is disabled (PSMCxEN = 0). Select a clock other than the 64 MHz clock to minimize power consumption when the PSMC is not enabled.

The Internal 64 MHz clock utilizes the system clock 4x PLL. When the system clock source is external and the PSMC is using the Internal 64 MHz clock, the 4x PLL should not be used for the system clock.

REGISTER 26-5: PSMC3SYNC: PSMC3 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P3POFST	P3PRPOL	P3DCPOL	—	—	P3SYNC<2:0>		
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **P3POFST:** PSMC3 Phase Offset Control bit
1 = sync_out source is phase event and latch set source is synchronous period event
0 = sync_out source is period event and latch set source is phase event

bit 6 **P3PRPOL:** PSMC3 Period Polarity Event Control bit
1 = Selected asynchronous period event inputs are inverted
0 = Selected asynchronous period event inputs are not inverted

bit 5 **P3DCPOL:** PSMC3 Duty-cycle Event Polarity Control bit
1 = Selected asynchronous duty-cycle event inputs are inverted
0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **P3SYNC<2:0>:** PSMC3 Period Synchronization Mode bits
1xx = Reserved - Do not use
100 = PSMC3 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)
011 = PSMC3 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
010 = PSMC3 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)
001 = PSMC3 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)
000 = PSMC3 is synchronized with period event

REGISTER 26-19: PSMCxTMRL: PSMC TIME BASE COUNTER LOW REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxTMRL<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PSMCxTMRL<7:0>:** 16-bit PSMCx Time Base Counter Least Significant bits
= PSMCxTMR<7:0>

REGISTER 26-20: PSMCxTMRH: PSMC TIME BASE COUNTER HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-1/1
PSMCxTMRH<7:0>							
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7-0 **PSMCxTMRH<7:0>:** 16-bit PSMCx Time Base Counter Most Significant bits
= PSMCxTMR<15:8>

27.2 SPI Mode Overview

The Serial Peripheral Interface (SPI) bus is a synchronous serial data communication bus that operates in Full-Duplex mode. Devices communicate in a master/slave environment where the master device initiates the communication. A slave device is controlled through a Chip Select known as Slave Select.

The SPI bus specifies four signal connections:

- Serial Clock (SCK)
- Serial Data Out (SDO)
- Serial Data In (SDI)
- Slave Select ($\overline{SS}$)

Figure 27-1 shows the block diagram of the MSSP module when operating in SPI mode.

The SPI bus operates with a single master device and one or more slave devices. When multiple slave devices are used, an independent Slave Select connection is required from the master device to each slave device.

Figure 27-4 shows a typical connection between a master device and multiple slave devices.

The master selects only one slave at a time. Most slave devices have tri-state outputs so their output signal appears disconnected from the bus when they are not selected.

Transmissions involve two shift registers, eight bits in size, one in the master and one in the slave. With either the master or the slave device, data is always shifted out one bit at a time, with the Most Significant bit (MSb) shifted out first. At the same time, a new Least Significant bit (LSb) is shifted into the same register.

Figure 27-5 shows a typical connection between two processors configured as master and slave devices.

Data is shifted out of both shift registers on the programmed clock edge and latched on the opposite edge of the clock.

The master device transmits information out on its SDO output pin which is connected to, and received by, the slave's SDI input pin. The slave device transmits information out on its SDO output pin, which is connected to, and received by, the master's SDI input pin.

To begin communication, the master device first sends out the clock signal. Both the master and the slave devices should be configured for the same clock polarity.

The master device starts a transmission by sending out the MSb from its shift register. The slave device reads this bit from that same line and saves it into the LSb position of its shift register.

During each SPI clock cycle, a full-duplex data transmission occurs. This means that while the master device is sending out the MSb from its shift register (on its SDO pin) and the slave device is reading this bit and saving it as the LSb of its shift register, that the slave device is also sending out the MSb from its shift register (on its SDO pin) and the master device is reading this bit and saving it as the LSb of its shift register.

After eight bits have been shifted out, the master and slave have exchanged register values.

If there is more data to exchange, the shift registers are loaded with new data and the process repeats itself.

Whether the data is meaningful or not (dummy data), depends on the application software. This leads to three scenarios for data transmission:

- Master sends useful data and slave sends dummy data.
- Master sends useful data and slave sends useful data.
- Master sends dummy data and slave sends useful data.

Transmissions may involve any number of clock cycles. When there is no more data to be transmitted, the master stops sending the clock signal and it deselects the slave.

Every slave device connected to the bus that has not been selected through its slave select line must disregard the clock and transmission signals and must not transmit out any data of its own.

27.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

TABLE 27-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	137
APFCON1	C2OUTSEL	CCP1SEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	132
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								294*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				340
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	342
SSP1STAT	SMP	CKE	D/$\overline{A}$	P	S	R/$\overline{W}$	UA	BF	338
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	136
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISA0	147

Legend: — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

* Page provides register information.

Note 1: PIC16(L)F1789 only.

FIGURE 27-29: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)

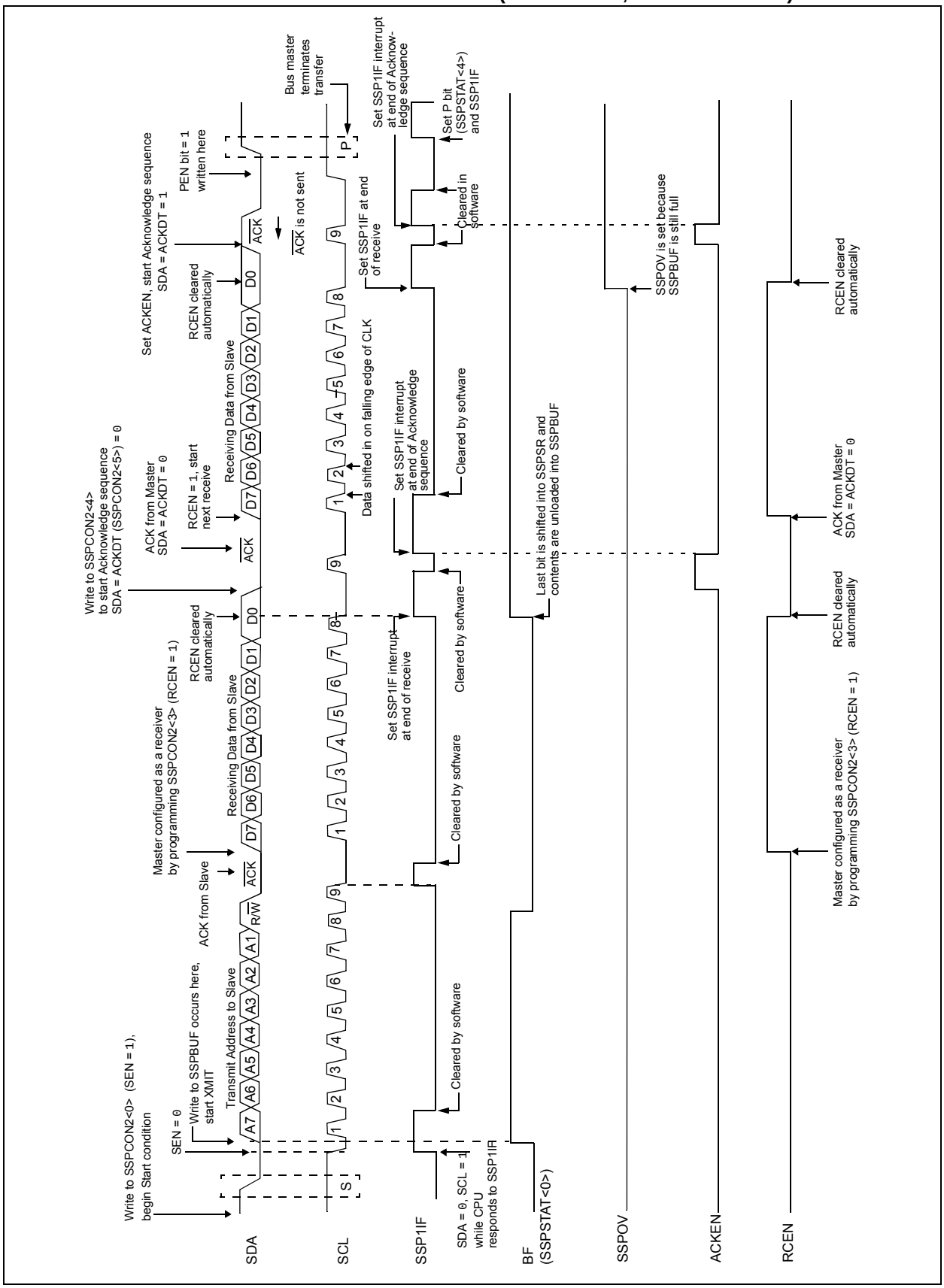
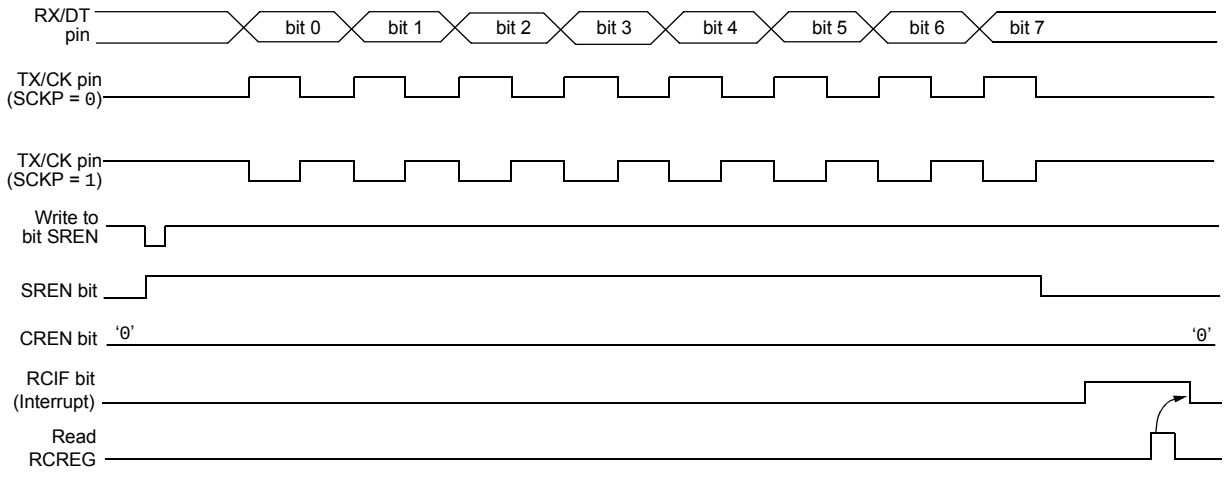


FIGURE 28-12: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



Note: Timing diagram demonstrates Sync Master mode with bit SREN = 1 and bit BRGH = 0.

TABLE 28-8: SUMMARY OF REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	132
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	356
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
RCREG	EUSART Receive Data Register								349*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	355
SPBRGL	BRG<7:0>								357
SPBRGH	BRG<15:8>								357
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	147
TXSTA	CSRC	TX9	TXEN	SYNC	SENDB	BRGH	TRMT	TX9D	354

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for synchronous master reception.

* Page provides register information.

31.3 DC Characteristics

TABLE 31-1: SUPPLY VOLTAGE

PIC16LF1788/9			Standard Operating Conditions (unless otherwise stated)				
PIC16F1788/9							
Param. No.	Sym.	Characteristic	Min.	Typ†	Max.	Units	Conditions
D001	VDD	**Supply Voltage (VDDMIN, VDDMAX)**					
			1.8 2.5	— —	3.6 3.6	V V	FOSC ≤ 16 MHz: FOSC ≤ 32 MHz (**Note 2**)
D001			2.3 2.5	— —	5.5 5.5	V V	FOSC ≤ 16 MHz: FOSC ≤ 32 MHz (**Note 2**)
D002*	VDR	**RAM Data Retention Voltage(1)**					
			1.5	—	—	V	Device in Sleep mode
D002*			1.7	—	—	V	Device in Sleep mode
	VPOR*	**Power-on Reset Release Voltage**	—	1.6	—	V	
	VPORR*	**Power-on Reset Rearm Voltage**					
			—	0.8	—	V	Device in Sleep mode
			—	1.5	—	V	Device in Sleep mode
D003	VFVR	**Fixed Voltage Reference Voltage(3)**	-4	—	4	%	1.024V, VDD ≥ 2.5V
			-4	—	4	%	2.048V, VDD ≥ 2.5V
			-5	—	5	%	4.096V, VDD ≥ 4.75V
D004*	SVDD	**VDD Rise Rate** to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See **Section 5.1 "Power-On Reset (POR)"** for details.

* These parameters are characterized but not tested.

† Data in "Typ" column is at 3.3V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in Sleep mode without losing RAM data.

2: PLL required for 32 MHz operation.

3: Industrial temperature range only.

TABLE 31-17: 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: V_{DD} = 3V, Temperature = 25°C (unless otherwise stated).							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DAC01*	C_{LSB}5	Step Size	—	V_{DD}/32	—	V	
DAC02*	C_{ACC}5	Absolute Accuracy	—	—	± 1/2	LSb	
DAC03*	C_R5	Unit Resistor Value (R)	—	5K	—	Ω	
DAC04*	C_{ST}5	Settling Time(2)	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: See **Section 32.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

2: Settling time measured while DACR<7:0> transitions from '00000' to '01111'.

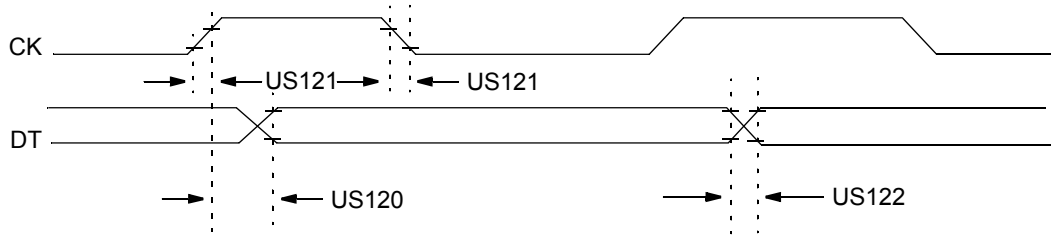
TABLE 31-18: 8-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: V_{DD} = 3V, Temperature = 25°C (unless otherwise stated).							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DAC05*	C_{LSB}8	Step Size	—	V_{DD}/256	—	V	
DAC06*	C_{ACC}8	Absolute Accuracy	—	—	± 1.5	LSb	
DAC07*	C_R8	Unit Resistor Value (R)	—	600	—	Ω	
DAC08*	C_{ST}8	Settling Time(1)	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<7:0> transitions from '0x00' to '0xFF'.

FIGURE 31-14: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



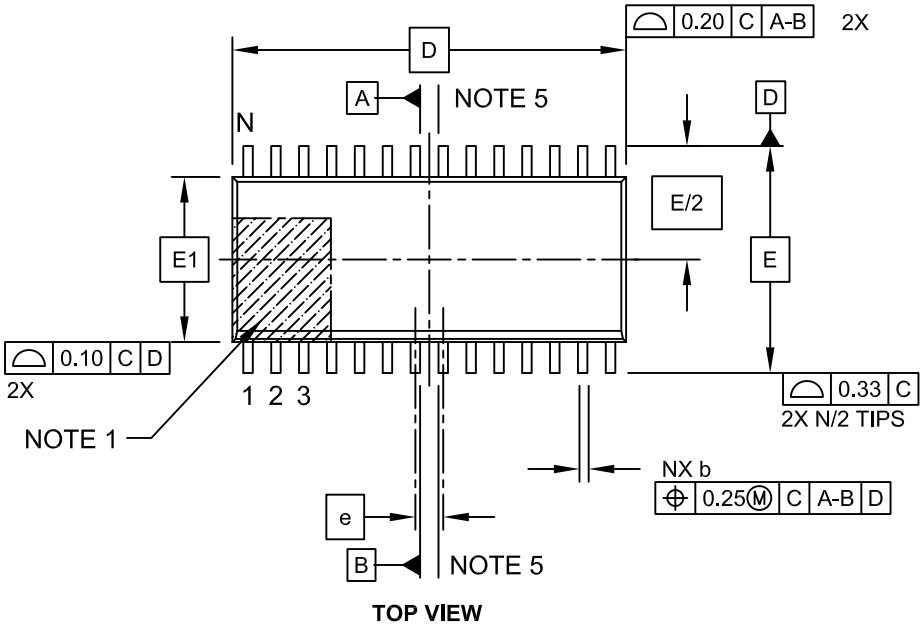
Note: Refer to Figure 31-4 for load conditions.

TABLE 31-19: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

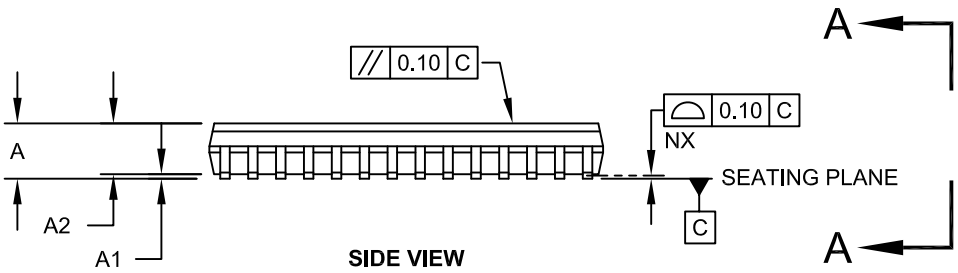
Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
US120	$T_{CK}H2_{DT}V$	SYNC XMIT (Master and Slave) Clock high to data-out valid	3.0-5.5V	—	80	ns	
			1.8-5.5V	—	100	ns	
US121	T_{CKRF}	Clock out rise time and fall time (Master mode)	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	
US122	T_{DTRF}	Data-out rise time and fall time	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	

28-Lead Plastic Small Outline (SO) - Wide, 7.50 mm Body [SOIC]

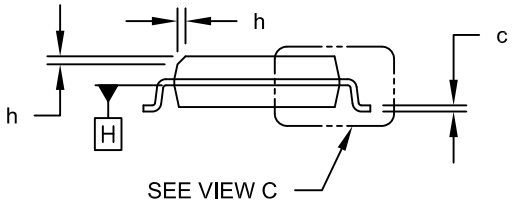
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW



VIEW A-A

Microchip Technology Drawing C04-052C Sheet 1 of 2