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Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	24
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 11x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-VQFN Exposed Pad
Supplier Device Package	28-QFN (6x6)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1788t-i-ml

PIN ALLOCATION TABLE

TABLE 1: 28-PIN ALLOCATION TABLE (PIC16(L)F1788)

I/O	28-Pin SPDIP, SOIC, SSOP	28-Pin QFN,	ADC	Reference	Comparator	Operation Amplifiers	8-bit/ 5-bit DAC	Timers	PSMC	CCP	EUSART	MSSP	Interrupt	Pull-up	Basic
RA0	2	27	AN0	—	C1IN0- C2IN0- C3IN0- C4IN0-	—	—	—	—	—	—	SS ⁽¹⁾	IOC	Y	—
RA1	3	28	AN1	—	C1IN1- C2IN1- C3IN1- C4IN1-	OPA1OUT	—	—	—	—	—	—	IOC	Y	—
RA2	4	1	AN2	VREF- DAC1VREF-	C1IN0+ C2IN0+ C3IN0+ C4IN0+	—	DAC1OUT1	—	—	—	—	—	IOC	Y	—
RA3	5	2	AN3	VREF+ DAC1VREF+ DAC2VREF+ DAC3VREF+ DAC4VREF+	C1IN1+	—	—	—	—	—	—	—	IOC	Y	—
RA4	6	3	—	—	C1OUT	OPA1IN+	DAC4OUT1	T0CKI	—	—	—	—	IOC	Y	—
RA5	7	4	AN4	—	C2OUT	OPA1IN-	DAC2OUT1	—	—	—	—	SS	IOC	Y	—
RA6	10	7	—	—	C2OUT ⁽¹⁾	—	—	—	—	—	—	—	IOC	Y	VCAP OSC2 CLKOUT
RA7	9	6	—	—	—	—	—	—	PSMC1CLK PSMC2CLK PSMC3CLK PSMC4CLK	—	—	—	IOC	Y	CLKIN OSC1
RB0	21	18	AN12	—	C2IN1+	—	—	—	PSMC1IN PSMC2IN PSMC3IN PSMC4IN	CCP1 ⁽¹⁾	—	—	INT IOC	Y	—
RB1	22	19	AN10	—	C1IN3- C2IN3- C3IN3- C4IN3-	OPA2OUT	—	—	—	—	—	—	IOC	Y	—
RB2	23	20	AN8	—	—	OPA2IN-	DAC3OUT1	—	—	—	—	—	IOC	Y	CLKR
RB3	24	21	AN9	—	C1IN2- C2IN2- C3IN2-	OPA2IN+	—	—	—	CCP2 ⁽¹⁾	—	—	IOC	Y	—
RB4	25	22	AN11	—	C3IN1+	—	—	—	—	—	—	SS ⁽¹⁾	IOC	Y	—
RB5	26	23	AN13	—	C4IN2- C3OUT	—	—	T1G	—	CCP3 ⁽¹⁾	—	SDO ⁽¹⁾	IOC	Y	—
RB6	27	24	—	—	C4IN1+	—	—	—	—	—	TX ⁽¹⁾ CK ⁽¹⁾	SDI ⁽¹⁾ SDA ⁽¹⁾	IOC	Y	ICSPCLK
RB7	28	25	—	—	—	—	DAC1OUT2 DAC2OUT2 DAC3OUT2 DAC4OUT2	—	—	—	RX ⁽¹⁾ DT ⁽¹⁾	SCK ⁽¹⁾ SCL ⁽¹⁾	IOC	Y	ICSPDAT
RC0	11	8	—	—	—	—	—	T1CKI T1OSO	PSMC1A	—	—	—	IOC	Y	—
RC1	12	9	—	—	—	—	—	T1OSI	PSMC1B	CCP2	—	—	IOC	Y	—
RC2	13	10	—	—	—	—	—	—	PSMC1C PSMC3B	CCP1	—	—	IOC	Y	—
RC3	14	11	—	—	—	—	—	—	PSMC1D PSMC4A	—	—	SCK SCL	IOC	Y	—
RC4	15	12	—	—	—	—	—	—	PSMC1E PSMC4B	—	—	SDI SDA	IOC	Y	—
RC5	16	13	—	—	—	—	—	—	PSMC1F PSMC3A	—	—	SDO	IOC	Y	—

Note 1: Alternate pin function selected with the APFCON1 (Register 13-1) and APFCON2 (Register 13-2) registers.

TABLE 3-4: PIC16(L)F1789 MEMORY MAP (BANKS 0-7)

BANK 0		BANK 1		BANK 2		BANK 3		BANK 4		BANK 5		BANK 6		BANK 7	
000h	Core Registers (Table 3-2)	080h	Core Registers (Table 3-2)	100h	Core Registers (Table 3-2)	180h	Core Registers (Table 3-2)	200h	Core Registers (Table 3-2)	280h	Core Registers (Table 3-2)	300h	Core Registers (Table 3-2)	380h	Core Registers (Table 3-2)
00Bh		08Bh		10Bh		18Bh		20Bh		28Bh		30Bh		38Bh	
00Ch	PORTA	08Ch	TRISA	10Ch	LATA	18Ch	ANSELA	20Ch	WPUA	28Ch	ODCONA	30Ch	SLRCONA	38Ch	INLVLA
00Dh	PORTB	08Dh	TRISB	10Dh	LATB	18Dh	ANSELB	20Dh	WPUB	28Dh	ODCONB	30Dh	SLRCONB	38Dh	INLVLB
00Eh	PORTC	08Eh	TRISC	10Eh	LATC	18Eh	ANSELC	20Eh	WPUC	28Eh	ODCONC	30Eh	SLRCONC	38Eh	INLVLC
00Fh	PORTD	08Fh	TRISD	10Fh	LATD	18Fh	ANSELD	20Fh	WPUD	28Fh	ODCOND	30Fh	SLRCOND	38Fh	INLVLD
010h	PORTE	090h	TRISE	110h	LATE	190h	ANSELE	210h	WPUE	290h	ODCONE	310h	SLRCONE	390h	INLVLE
011h	PIR1	091h	PIE1	111h	CM1CON0	191h	EEADRL	211h	SSP1BUF	291h	CCPR1L	311h	CCPR3L	391h	IOCAP
012h	PIR2	092h	PIE2	112h	CM1CON1	192h	EEADRH	212h	SSP1ADD	292h	CCPR1H	312h	CCPR3H	392h	IOCAN
013h	PIR3	093h	PIE3	113h	CM2CON0	193h	EEDATL	213h	SSP1MSK	293h	CCP1CON	313h	CCP3CON	393h	IOCAF
014h	PIR4	094h	PIE4	114h	CM2CON1	194h	EEDATH	214h	SSP1STAT	294h	—	314h	—	394h	IOCBP
015h	TMR0	095h	OPTION_REG	115h	CMOUT	195h	EECON1	215h	SSP1CON1	295h	—	315h	—	395h	IOCBN
016h	TMR1L	096h	PCON	116h	BORCON	196h	EECON2	216h	SSP1CON2	296h	—	316h	—	396h	IOCBF
017h	TMR1H	097h	WDTCON	117h	FVRCON	197h	VREGCON ⁽¹⁾	217h	SSP1CON3	297h	—	317h	—	397h	IOCCP
018h	T1CON	098h	OSCTUNE	118h	DAC1CON0	198h	—	218h	—	298h	CCPR2L	318h	—	398h	IOCCN
019h	T1GCON	099h	OSCCON	119h	DAC1CON1	199h	RC1REG	219h	—	299h	CCPR2H	319h	—	399h	IOCCF
01Ah	TMR2	09Ah	OSCSTAT	11Ah	CM4CON0	19Ah	TX1REG	21Ah	—	29Ah	CCP2CON	31Ah	—	39Ah	—
01Bh	PR2	09Bh	ADRESL	11Bh	CM4CON1	19Bh	SP1BRGL	21Bh	—	29Bh	—	31Bh	—	39Bh	—
01Ch	T2CON	09Ch	ADRESH	11Ch	APFCON2	19Ch	SP1BRGH	21Ch	—	29Ch	—	31Ch	—	39Ch	—
01Dh	—	09Dh	ADCON0	11Dh	APFCON1	19Dh	RC1STA	21Dh	—	29Dh	—	31Dh	—	39Dh	IOCEP
01Eh	—	09Eh	ADCON1	11Eh	CM3CON0	19Eh	TX1STA	21Eh	—	29Eh	—	31Eh	—	39Eh	IOCEN
01Fh	—	09Fh	ADCON2	11Fh	CM3CON1	19Fh	BAUD1CON	21Fh	—	29Fh	—	31Fh	—	39Fh	IOCEF
020h	General Purpose Register 80 Bytes	0A0h	General Purpose Register 80 Bytes	120h	General Purpose Register 80 Bytes	1A0h	General Purpose Register 80 Bytes	220h	General Purpose Register 80 Bytes	2A0h	General Purpose Register 80 Bytes	320h	General Purpose Register 80 Bytes	3A0h	General Purpose Register 80 Bytes
06Fh		0EFh		16Fh		1EFh		26Fh		2EFh		36Fh		3EFh	
070h	Common RAM 70h – 7Fh	0F0h	Accesses 70h – 7Fh	170h	Accesses 70h – 7Fh	1F0h	Accesses 70h – 7Fh	270h	Accesses 70h – 7Fh	2F0h	Accesses 70h – 7Fh	370h	Accesses 70h – 7Fh	3F0h	Accesses 70h – 7Fh
07Fh		0FFh		17Fh		1FFh		27Fh		2FFh		37Fh		3FFh	

Legend: = Unimplemented data memory locations, read as '0'.

Note 1: PIC16F1789 only.

13.3 PORTA Registers

13.3.1 DATA REGISTER

PORTA is an 8-bit wide, bidirectional port. The corresponding data direction register is TRISA (Register 13-4). Setting a TRISA bit (= 1) will make the corresponding PORTA pin an input (i.e., disable the output driver). Clearing a TRISA bit (= 0) will make the corresponding PORTA pin an output (i.e., enables output driver and puts the contents of the output latch on the selected pin). Example 13-1 shows how to initialize PORTA.

Reading the PORTA register (Register 13-3) reads the status of the pins, whereas writing to it will write to the PORT latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified and then written to the PORT data latch (LATA).

13.3.2 DIRECTION CONTROL

The TRISA register (Register 13-4) controls the PORTA pin output drivers, even when they are being used as analog inputs. The user should ensure the bits in the TRISA register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

13.3.3 OPEN-DRAIN CONTROL

The ODCONA register (Register 13-8) controls the open-drain feature of the port. Open-drain operation is independently selected for each pin. When an ODCONA bit is set, the corresponding port output becomes an open-drain driver capable of sinking current only. When an ODCONA bit is cleared, the corresponding port output pin is the standard push-pull drive capable of sourcing and sinking current.

13.3.4 SLEW RATE CONTROL

The SLRCONA register (Register 13-9) controls the slew rate option for each port pin. Slew rate control is independently selectable for each port pin. When an SLRCONA bit is set, the corresponding port pin drive is slew rate limited. When an SLRCONA bit is cleared, The corresponding port pin drive slews at the maximum rate possible.

13.3.5 INPUT THRESHOLD CONTROL

The INLVLA register (Register 13-10) controls the input voltage threshold for each of the available PORTA input pins. A selection between the Schmitt Trigger CMOS or the TTL Compatible thresholds is available. The input threshold is important in determining the value of a read of the PORTA register and also the level at which an interrupt-on-change occurs, if that feature is enabled. See **Section TABLE 31-1: "Supply Voltage"** for more information on threshold levels.

Note: Changing the input threshold selection should be performed while all peripheral modules are disabled. Changing the threshold level during the time a module is active may inadvertently generate a transition associated with an input pin, regardless of the actual voltage level on that pin.

13.3.6 ANALOG CONTROL

The ANSELA register (Register 13-6) is used to configure the Input mode of an I/O pin to analog. Setting the appropriate ANSELA bit high will cause all digital reads on the pin to be read as '0' and allow analog functions on the pin to operate correctly.

The state of the ANSELA bits has no effect on digital output functions. A pin with TRIS clear and ANSEL set will still operate as a digital output, but the Input mode will be analog. This can cause unexpected behavior when executing read-modify-write instructions on the affected port.

Note: The ANSELA bits default to the Analog mode after Reset. To use any pins as digital general purpose or peripheral inputs, the corresponding ANSEL bits must be initialized to '0' by user software.

EXAMPLE 13-1: INITIALIZING PORTA

```
; This code example illustrates
; initializing the PORTA register. The
; other ports are initialized in the same
; manner.

BANKSEL PORTA      ;
CLRF   PORTA       ;Init PORTA
BANKSEL LATA       ;Data Latch
CLRF   LATA        ;
BANKSEL ANSELA     ;
CLRF   ANSELA      ;digital I/O
BANKSEL TRISA      ;
MOVLW  B'00111000' ;Set RA<5:3> as inputs
MOVWF  TRISA       ;and set RA<2:0> as
                  ;outputs
```

TABLE 13-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSEL	—	—	—	—	—	ANSD2	ANSD1	ANSD0	152
INLVLD	INLVLD7	INLVLD6	INLVLD5	INLVLD4	INLVLD3	INLVLD2	INLVLD1	INLVLD0	153
LATD	LATD7	LATD6	LATD5	LATD4	LATD3	LATD2	LATD1	LATD0	151
ODCOND	ODD7	ODD6	ODD5	ODD4	ODD3	ODD2	ODD1	ODD0	153
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	151
SLRCOND	SLRD7	SLRD6	SLRD5	SLRD4	SLRD3	SLRD2	SLRD1	SLRD0	153
TRISD	TRISD7	TRISD6	TRISD5	TRISD4	TRISD3	TRISD2	TRISD1	TRISD0	151
WPUD	WPUD7	WPUD6	WPUD5	WPUD4	WPUD3	WPUD2	WPUD1	WPUD0	152

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTD.

14.6 Register Definitions: Interrupt-on-Change Control

REGISTER 14-1: IOCxP: INTERRUPT-ON-CHANGE POSITIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCxP7	IOCxP6	IOCxP5	IOCxP4	IOCxP3	IOCxP2	IOCxP1	IOCxP0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **IOCxP<7:0>:** Interrupt-on-Change Positive Edge Enable bits⁽¹⁾

1 = Interrupt-on-Change enabled on the pin for a positive going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

Note 1: For IOCEP register, bit 3 (IOCEP3) is the only implemented bit in the register.

REGISTER 14-2: IOCxN: INTERRUPT-ON-CHANGE NEGATIVE EDGE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
IOCxN7	IOCxN6	IOCxN5	IOCxN4	IOCxN3	IOCxN2	IOCxN1	IOCxN0
bit 7							bit 0

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-0 **IOCxN<7:0>:** Interrupt-on-Change Negative Edge Enable bits⁽¹⁾

1 = Interrupt-on-Change enabled on the pin for a negative going edge. Associated Status bit and interrupt flag will be set upon detecting an edge.

0 = Interrupt-on-Change disabled for the associated pin.

Note 1: For IOCEN register, bit 3 (IOCEN3) is the only implemented bit in the register.

25.3.2 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for standard PWM operation:

1. Disable the CCPx pin output driver by setting the associated TRIS bit.
2. Load the PR2 register with the PWM period value.
3. Configure the CCP module for the PWM mode by loading the CCPxCON register with the appropriate values.
4. Load the CCPRxL register and the DCxBx bits of the CCPxCON register, with the PWM duty cycle value.
5. Configure and start Timer2:
 - Clear the TMR2IF interrupt flag bit of the PIRx register. See Note below.
 - Configure the T2CKPS bits of the T2CON register with the Timer prescale value.
 - Enable the Timer by setting the TMR2ON bit of the T2CON register.
6. Enable PWM output pin:
 - Wait until the Timer overflows and the TMR2IF bit of the PIR1 register is set. See Note below.
 - Enable the CCPx pin output driver by clearing the associated TRIS bit.

Note: In order to send a complete duty cycle and period on the first PWM output, the above steps must be included in the setup sequence. If it is not critical to start with a complete PWM signal on the first output, then step 6 may be ignored.

25.3.3 TIMER2 TIMER RESOURCE

The PWM standard mode makes use of the 8-bit Timer2 timer resources to specify the PWM period.

25.3.4 PWM PERIOD

The PWM period is specified by the PR2 register of Timer2. The PWM period can be calculated using the formula of Equation 25-1.

EQUATION 25-1: PWM PERIOD

$$PWM\ Period = [(PR2) + 1] \cdot 4 \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

Note 1: $TOSC = 1/FOSC$

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCPx pin is set. (Exception: If the PWM duty cycle = 0%, the pin will not be set.)
- The PWM duty cycle is latched from CCPRxL into CCPRxH.

Note: The Timer postscaler (see **Section 24.1 “Timer2 Operation”**) is not used in the determination of the PWM frequency.

25.3.5 PWM DUTY CYCLE

The PWM duty cycle is specified by writing a 10-bit value to multiple registers: CCPRxL register and DCxB<1:0> bits of the CCPxCON register. The CCPRxL contains the eight MSBs and the DCxB<1:0> bits of the CCPxCON register contain the two LSBs. CCPRxL and DCxB<1:0> bits of the CCPxCON register can be written to at any time. The duty cycle value is not latched into CCPRxH until after the period completes (i.e., a match between PR2 and TMR2 registers occurs). While using the PWM, the CCPRxH register is read-only.

Equation 25-2 is used to calculate the PWM pulse width.

Equation 25-3 is used to calculate the PWM duty cycle ratio.

EQUATION 25-2: PULSE WIDTH

$$Pulse\ Width = (CCPRxL:CCPxCON<5:4>) \cdot TOSC \cdot (TMR2\ Prescale\ Value)$$

EQUATION 25-3: DUTY CYCLE RATIO

$$Duty\ Cycle\ Ratio = \frac{(CCPRxL:CCPxCON<5:4>)}{4(PR2 + 1)}$$

The CCPRxH register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

The 8-bit timer TMR2 register is concatenated with either the 2-bit internal system clock (FOSC), or two bits of the prescaler, to create the 10-bit time base. The system clock is used if the Timer2 prescaler is set to 1:1.

When the 10-bit time base matches the CCPRxH and 2-bit latch, then the CCPx pin is cleared (see Figure 25-4).

26.3.12 3-PHASE PWM

The 3-Phase mode of operation is used in 3-phase power supply and motor drive applications configured as three half-bridges. A half-bridge configuration consists of two power driver devices in series, between the positive power rail (high side) and negative power rail (low side). The three outputs come from the junctions between the two drivers in each half-bridge. When the steering control selects a phase drive, power flows from the positive rail through a high-side power device to the load and back to the power supply through a low-side power device.

In this mode of operation, all six PSMC outputs are used, but only two are active at a time.

The two active outputs consist of a high-side driver and low-side driver output.

26.3.12.1 Mode Features

- No dead-band control is available
- PWM can be steered to the following six pairs:
 - PSMCxA and PSMCxD
 - PSMCxA and PSMCxF
 - PSMCxC and PSMCxF
 - PSMCxC and PSMCxB
 - PSMCxE and PSMCxB
 - PSMCxE and PSMCxD

26.3.12.2 Waveform Generation

3-phase steering has a more complex waveform generation scheme than the other modes. There are several factors which go into what waveforms are created.

The PSMC outputs are grouped into three sets of drivers: one for each phase. Each phase has two associated PWM outputs: one for the high-side drive and one for the low-side drive.

High Side drives are indicated by 1H, 2H and 3H.

Low Side drives are indicated by 1L, 2L, 3L.

Phase grouping is mapped as shown in Table 26-1. There are six possible phase drive combinations. Each phase drive combination activates two of the six outputs and deactivates the other four. Phase drive is selected with the steering control as shown in Table 26-2.

TABLE 26-1: PHASE GROUPING

PSMC grouping	
PSMCxA	1H
PSMCxB	1L
PSMCxC	2H
PSMCxD	2L
PSMCxE	3H
PSMCxF	3L

TABLE 26-2: 3-PHASE STEERING CONTROL

PSMC outputs		PSMCxSTR0 Value ⁽¹⁾						
		00h	01h	02h	04h	08h	10h	20h
PSMCxA	1H	inactive	active	active	inactive	inactive	inactive	inactive
PSMCxB	1L	inactive	inactive	inactive	inactive	active	active	inactive
PSMCxC	2H	inactive	inactive	inactive	active	active	inactive	inactive
PSMCxD	2L	inactive	active	inactive	inactive	inactive	inactive	active
PSMCxE	3H	inactive	inactive	inactive	inactive	inactive	active	active
PSMCxF	3L	inactive	inactive	active	active	inactive	inactive	inactive

Note 1: Steering for any value other than those shown will default to the output combination of the Least Significant steering bit that is set.

High/Low Side Modulation Enable

It is also possible to enable the PWM output on the low side or high side drive independently using the PxLSMEN and PxHSMEN bits of the PSMC Steering Control 1 (PSMCxSTR1) register (Register 26-33).

When the PxHSMEN bit is set, the active-high side output listed in Table 26-2 is modulated using the normal rising edge and falling edge events.

When the PxLSMEN bit is set, the active-low side output listed in Table 26-2 is modulated using the normal rising edge and falling edge events.

When both the PxHSMEN and PxLSMEN bits are cleared, the active outputs listed in Table 26-2 go immediately to the rising edge event states and do not change.

Rising Edge Event

- Active outputs are set to their active states

Falling Edge Event

- Active outputs are set to their inactive state

REGISTER 26-5: PSMC3SYNC: PSMC3 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P3POFST	P3PRPOL	P3DCPOL	—	—	P3SYNC<2:0>		
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7 **P3POFST:** PSMC3 Phase Offset Control bit
1 = sync_out source is phase event and latch set source is synchronous period event
0 = sync_out source is period event and latch set source is phase event
- bit 6 **P3PRPOL:** PSMC3 Period Polarity Event Control bit
1 = Selected asynchronous period event inputs are inverted
0 = Selected asynchronous period event inputs are not inverted
- bit 5 **P3DCPOL:** PSMC3 Duty-cycle Event Polarity Control bit
1 = Selected asynchronous duty-cycle event inputs are inverted
0 = Selected asynchronous duty-cycle event inputs are not inverted
- bit 4-3 **Unimplemented:** Read as '0'
- bit 2-0 **P3SYNC<2:0>:** PSMC3 Period Synchronization Mode bits
1xx = Reserved - Do not use
100 = PSMC3 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)
011 = PSMC3 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)
010 = PSMC3 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)
001 = PSMC3 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)
000 = PSMC3 is synchronized with period event

REGISTER 26-16: PSMCxASDC: PSMC AUTO-SHUTDOWN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	U-0	U-0	R/W-0/0
PxASE	PxASDEN	PxARSEN	—	—	—	—	PxASDOV
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7 **PxASE:** PWM Auto-Shutdown Event Status bit⁽¹⁾

1 = A shutdown event has occurred, PWM outputs are inactive and in their shutdown states

0 = PWM outputs are operating normally

bit 6 **PxASDEN:** PWM Auto-Shutdown Enable bit

1 = Auto-shutdown is enabled. If any of the sources in PSMCxASDS assert a logic '1', then the outputs will go into their auto-shutdown state and PSMCxSIF flag will be set.

0 = Auto-shutdown is disabled

bit 5 **PxARSEN:** PWM Auto-Restart Enable bit

1 = PWM restarts automatically when the shutdown condition is removed.

0 = The PxASE bit must be cleared in firmware to restart PWM after the auto-shutdown condition is cleared.

bit 4-1 **Unimplemented:** Read as '0'

bit 0 **PxASDOV:** PWM Auto-Shutdown Override bit

PxASDEN = 1:

1 = Force PxASDL[n] levels on the PSMCx[n] pins without causing a PSMCxSIF interrupt

0 = Normal PWM and auto-shutdown execution

PxASDEN = 0:

No effect

Note 1: PASE bit may be set in software. When this occurs the functionality is the same as that caused by hardware.

REGISTER 26-18: PSMCxASDS: PSMC AUTO-SHUTDOWN SOURCE REGISTER

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxASDSIN	—	—	PxASDSC4	PxASDSC3	PxASDSC2	PxASDSC1	—
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7 **PxASDSIN:** Auto-shutdown occurs on PSMCxIN pin
1 = Auto-shutdown will occur when PSMCxIN pin goes true
0 = PSMCxIN pin will not cause auto-shutdown
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **PxASDSC4:** Auto-shutdown occurs on sync_C4OUT output
1 = Auto-shutdown will occur when sync_C4OUT output goes true
0 = sync_C4OUT will not cause auto-shutdown
- bit 3 **PxASDSC3:** Auto-shutdown occurs on sync_C3OUT output
1 = Auto-shutdown will occur when sync_C3OUT output goes true
0 = sync_C3OUT will not cause auto-shutdown
- bit 2 **PxASDSC2:** Auto-shutdown occurs on sync_C2OUT output
1 = Auto-shutdown will occur when sync_C2OUT output goes true
0 = sync_C2OUT will not cause auto-shutdown
- bit 1 **PxASDSC1:** Auto-shutdown occurs on sync_C1OUT output
1 = Auto-shutdown will occur when sync_C1OU output goes true
0 = sync_C1OU will not cause auto-shutdown
- bit 0 **Unimplemented:** Read as '0'

REGISTER 26-21: PSMCxPHL: PSMC PHASE COUNT LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxPHL<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0 **PSMCxPHL<7:0>**: 16-bit Phase Count Least Significant bits
 = PSMCxPH<7:0>

REGISTER 26-22: PSMCxPHH: PSMC PHASE COUNT HIGH BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxPHH<7:0>							
bit 7				bit 0			

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

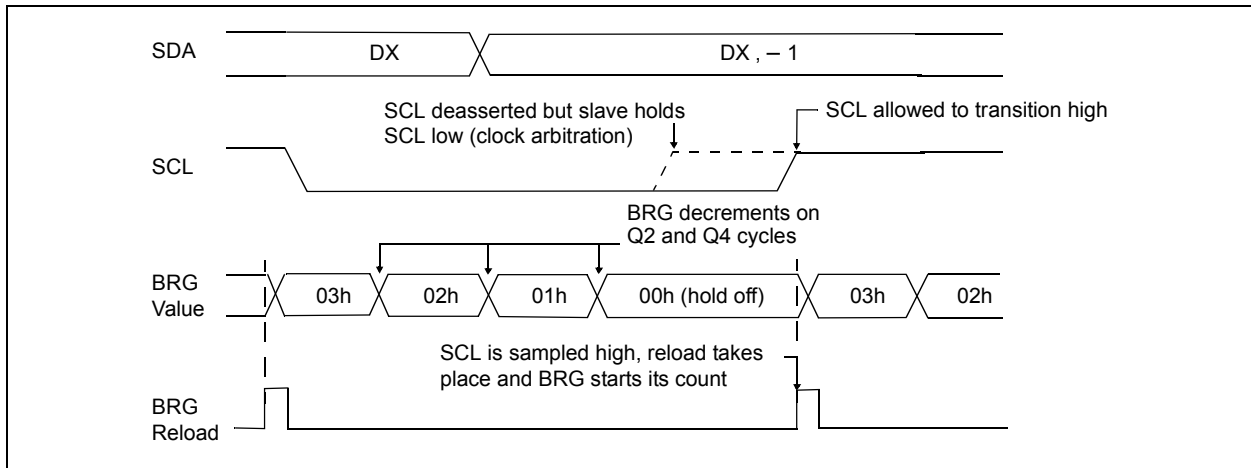
'0' = Bit is cleared

bit 7-0 **PSMCxPHH<7:0>**: 16-bit Phase Count Most Significant bits
 = PSMCxPH<15:8>

27.6.2 CLOCK ARBITRATION

Clock arbitration occurs when the master, during any receive, transmit or Repeated Start/Stop condition, releases the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the Baud Rate Generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is sampled high, the Baud Rate Generator is reloaded with the contents of SSPADD<7:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count in the event that the clock is held low by an external device (Figure 27-25).

FIGURE 27-25: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



27.6.3 WCOL STATUS FLAG

If the user writes the SSPBUF when a Start, Restart, Stop, Receive or Transmit sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write does not occur). Any time the WCOL bit is set it indicates that an action on SSPBUF was attempted while the module was not idle.

Note: Because queuing of events is not allowed, writing to the lower five bits of SSPCON2 is disabled until the Start condition is complete.

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27.6.8 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge Sequence Enable bit, ACKEN bit of the SSPCON2 register. When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The Baud Rate Generator then counts for one rollover period (TBRG) and the SCL pin is deasserted (pulled high). When the SCL pin is sampled high (clock arbitration), the Baud Rate Generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the Baud Rate Generator is turned off and the MSSP module then goes into Idle mode (Figure 27-29).

27.6.8.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write does not occur).

27.6.9 STOP CONDITION TIMING

A Stop bit is asserted on the SDA pin at the end of a receive/transmit by setting the Stop Sequence Enable bit, PEN bit of the SSPCON2 register. At the end of a receive/transmit, the SCL line is held low after the falling edge of the ninth clock. When the PEN bit is set, the master will assert the SDA line low. When the SDA line is sampled low, the Baud Rate Generator is reloaded and counts down to '0'. When the Baud Rate Generator times out, the SCL pin will be brought high and one TBRG (Baud Rate Generator rollover count) later, the SDA pin will be deasserted. When the SDA pin is sampled high while SCL is high, the P bit of the SSPSTAT register is set. A TBRG later, the PEN bit is cleared and the SSP1IF bit is set (Figure 27-30).

27.6.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Stop sequence is in progress, then the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

FIGURE 27-30: ACKNOWLEDGE SEQUENCE WAVEFORM

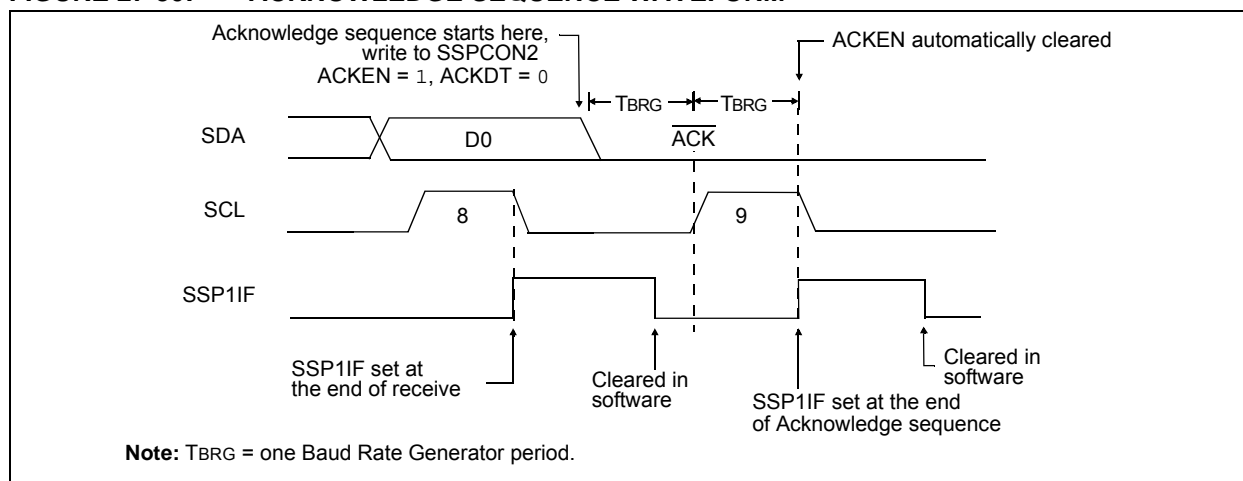


TABLE 28-2: SUMMARY OF REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
APFCON1	C2OUTSEL	CC1PSEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	132
BAUDCON	ABDOVF	RCIDL	—	SCKP	BRG16	—	WUE	ABDEN	356
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
RCREG	EUSART Receive Data Register								349*
RCSTA	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	355
SPBRGL	BRG<7:0>								357
SPBRGH	BRG<15:8>								357
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISC0	147
TXSTA	CSRC	TX9	TXEN	SYNC	SENDER	BRGH	TRMT	TX9D	354

Legend: — = unimplemented location, read as '0'. Shaded cells are not used for asynchronous reception.

* Page provides register information.

28.4 EUSART Baud Rate Generator (BRG)

The Baud Rate Generator (BRG) is an 8-bit or 16-bit timer that is dedicated to the support of both the asynchronous and synchronous EUSART operation. By default, the BRG operates in 8-bit mode. Setting the BRG16 bit of the BAUDCON register selects 16-bit mode.

The SPBRGH, SPBRGL register pair determines the period of the free running baud rate timer. In Asynchronous mode the multiplier of the baud rate period is determined by both the BRGH bit of the TXSTA register and the BRG16 bit of the BAUDCON register. In Synchronous mode, the BRGH bit is ignored.

Table 28-3 contains the formulas for determining the baud rate. Example 28-1 provides a sample calculation for determining the baud rate and baud rate error.

Typical baud rates and error values for various asynchronous modes have been computed for your convenience and are shown in Table 28-3. It may be advantageous to use the high baud rate (BRGH = 1), or the 16-bit BRG (BRG16 = 1) to reduce the baud rate error. The 16-bit BRG mode is used to achieve slow baud rates for fast oscillator frequencies.

Writing a new value to the SPBRGH, SPBRGL register pair causes the BRG timer to be reset (or cleared). This ensures that the BRG does not wait for a timer overflow before outputting the new baud rate.

If the system clock is changed during an active receive operation, a receive error or data loss may result. To avoid this problem, check the status of the RCIDL bit to make sure that the receive operation is idle before changing the system clock.

EXAMPLE 28-1: CALCULATING BAUD RATE ERROR

For a device with FOSC of 16 MHz, desired baud rate of 9600, Asynchronous mode, 8-bit BRG:

$$\text{Desired Baud Rate} = \frac{F_{OSC}}{64(SPBRGH:SPBRGL + 1)}$$

Solving for SPBRGH:SPBRGL:

$$X = \frac{\frac{F_{OSC}}{\text{Desired Baud Rate}}}{64} - 1$$

$$= \frac{\frac{16000000}{9600}}{64} - 1$$

$$= [25.042] = 25$$

$$\text{Calculated Baud Rate} = \frac{16000000}{64(25 + 1)}$$

$$= 9615$$

$$\text{Error} = \frac{\text{Calc. Baud Rate} - \text{Desired Baud Rate}}{\text{Desired Baud Rate}}$$

$$= \frac{(9615 - 9600)}{9600} = 0.16\%$$

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FIGURE 31-16: SPI MASTER MODE TIMING (CKE = 0, SMP = 0)

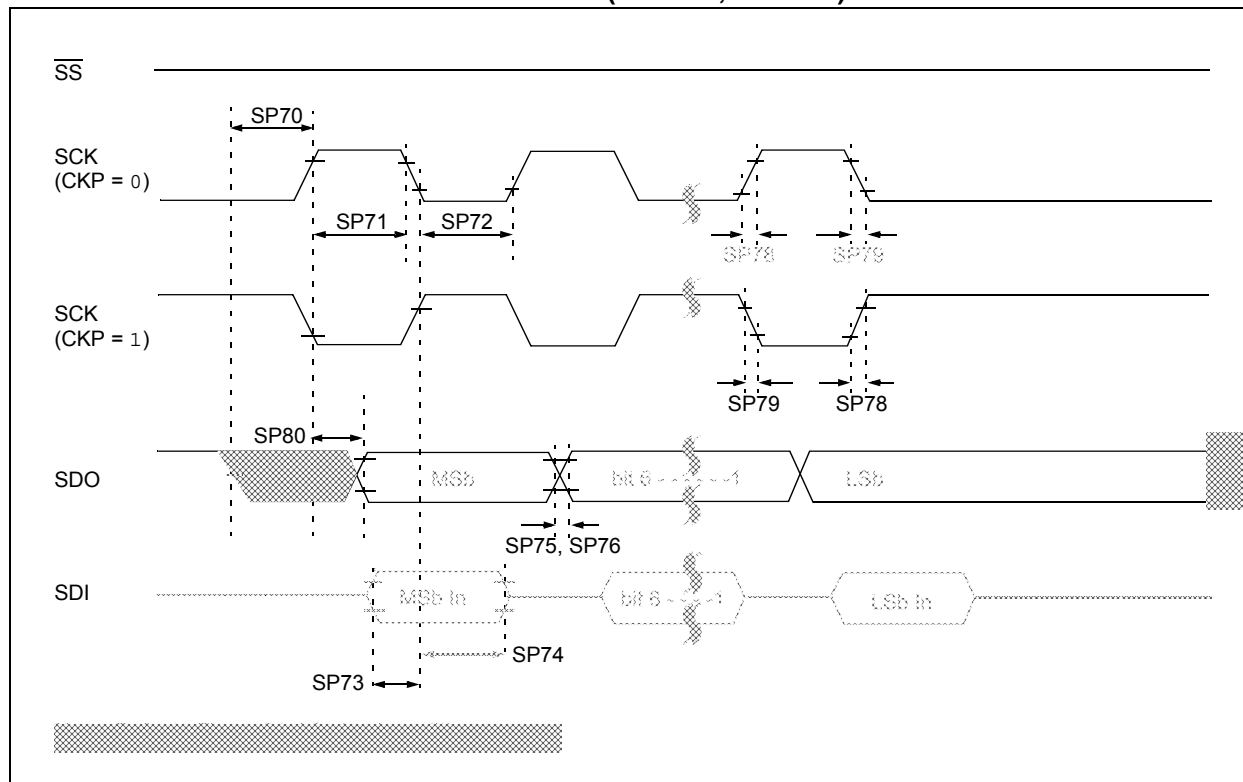
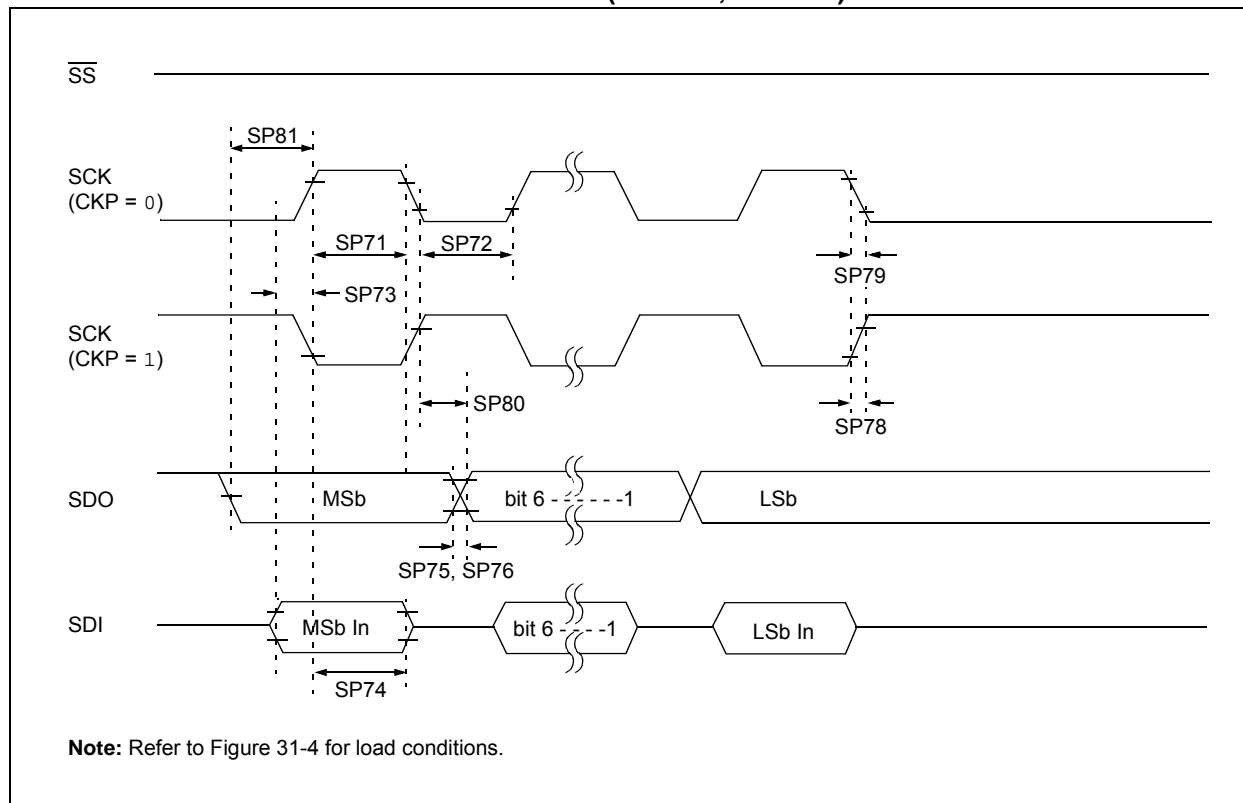


FIGURE 31-17: SPI MASTER MODE TIMING (CKE = 1, SMP = 1)



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Note: Unless otherwise noted, $V_{IN} = 5V$, $F_{OSC} = 300\text{ kHz}$, $C_{IN} = 0.1\text{ }\mu F$, $T_A = 25^\circ C$.

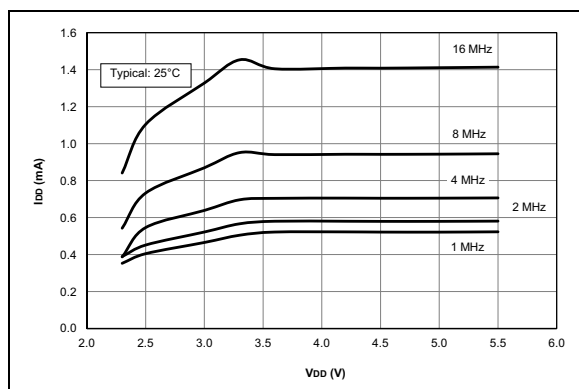


FIGURE 32-25: I_{DD} Typical, HFINTOSC Mode, PIC16F1788/9 Only.

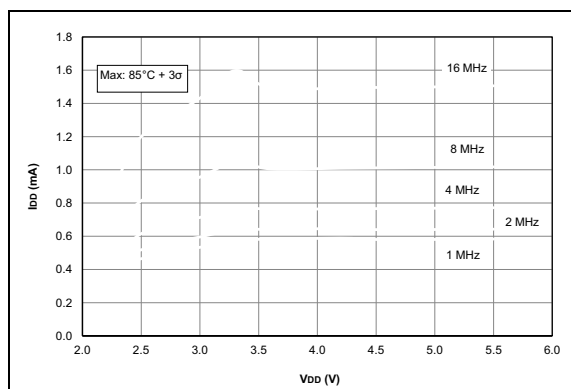


FIGURE 32-26: I_{DD} Maximum, HFINTOSC Mode, PIC16F1788/9 Only.

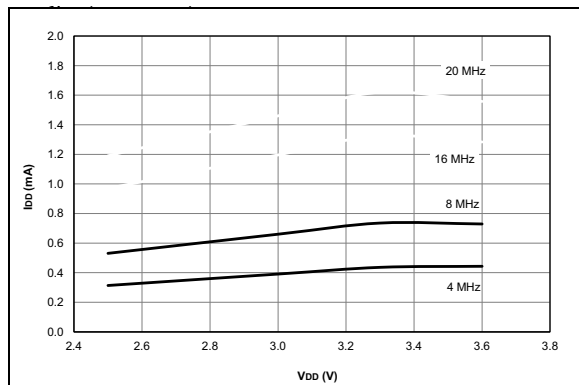


FIGURE 32-27: I_{DD} Typical, HS Oscillator, $25^\circ C$, PIC16LF1788/9 Only.

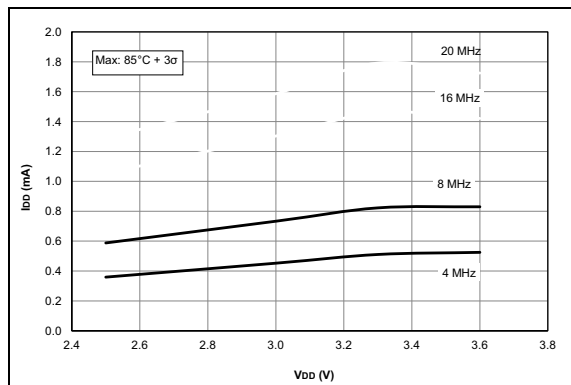


FIGURE 32-28: I_{DD} Maximum, HS Oscillator, PIC16LF1788/9 Only.

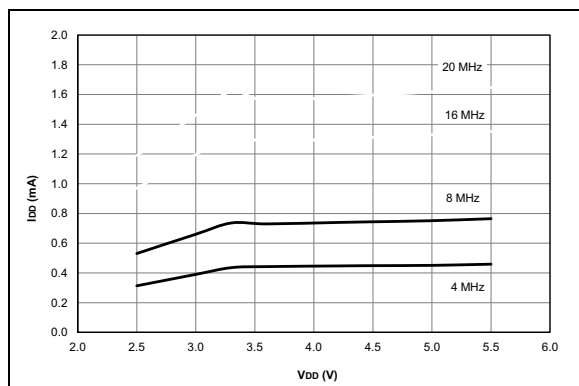


FIGURE 32-29: I_{DD} Typical, HS Oscillator, $25^\circ C$, PIC16F1788/9 Only.

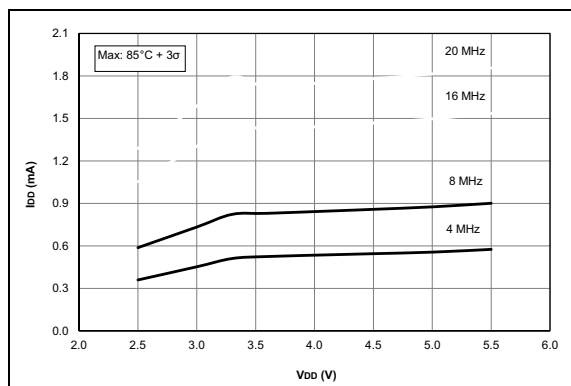
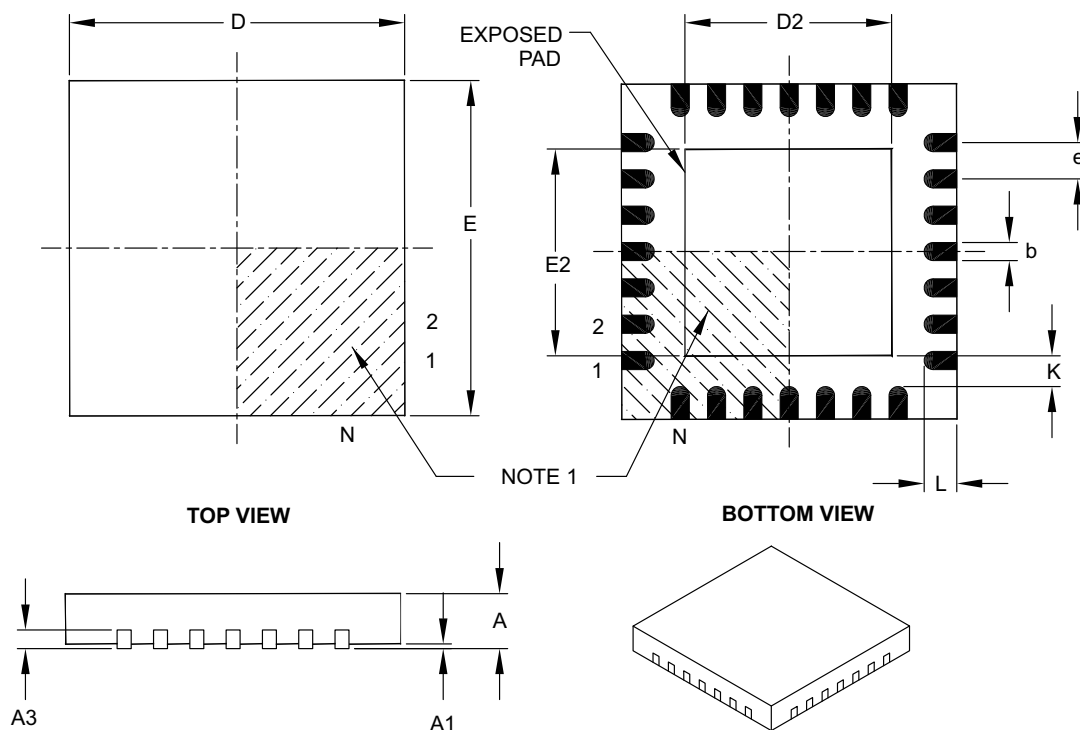


FIGURE 32-30: I_{DD} Maximum, HS Oscillator, PIC16F1788/9 Only.

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28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



		Units	MILLIMETERS		
Dimension Limits			MIN	NOM	MAX
Number of Pins	N		28		
Pitch	e		0.65 BSC		
Overall Height	A		0.80	0.90	1.00
Standoff	A1		0.00	0.02	0.05
Contact Thickness	A3		0.20 REF		
Overall Width	E		6.00 BSC		
Exposed Pad Width	E2		3.65	3.70	4.20
Overall Length	D		6.00 BSC		
Exposed Pad Length	D2		3.65	3.70	4.20
Contact Width	b		0.23	0.30	0.35
Contact Length	L		0.50	0.55	0.70
Contact-to-Exposed Pad	K		0.20	–	–

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.

2. Package is saw singulated.

3. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

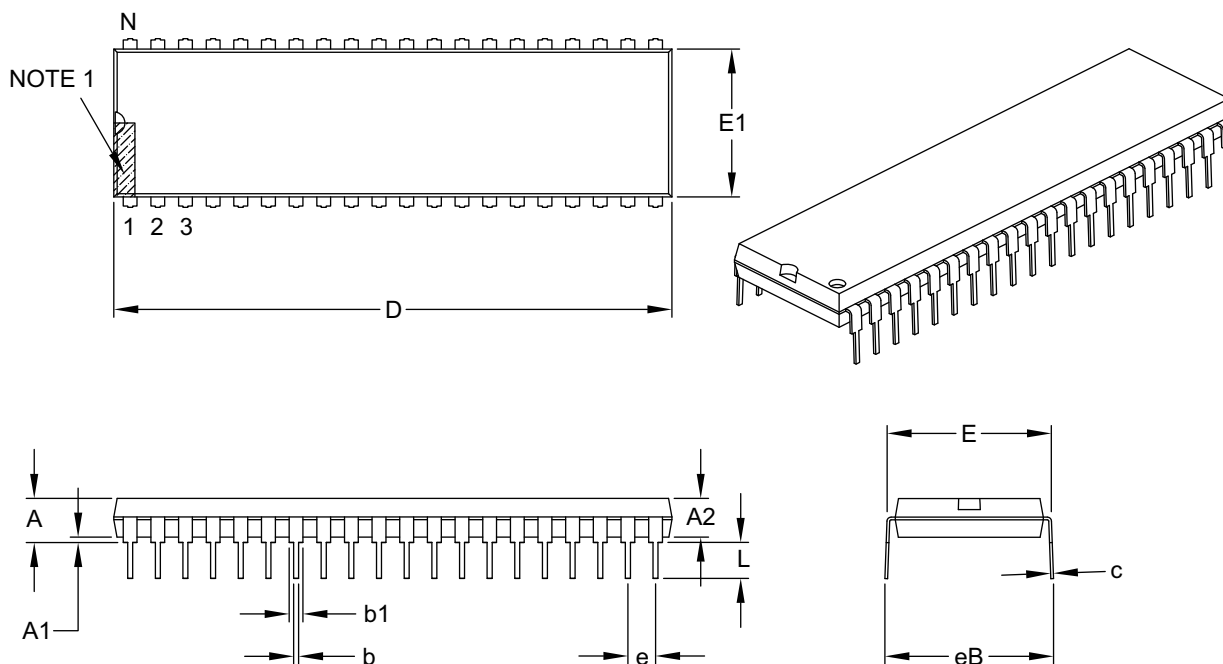
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-105B

PIC16(L)F1788/9

40-Lead Plastic Dual In-Line (P) – 600 mil Body [PDIP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	INCHES		
		MIN	NOM	MAX
Number of Pins	N	40		
Pitch	e	.100 BSC		
Top to Seating Plane	A	–	–	.250
Molded Package Thickness	A2	.125	–	.195
Base to Seating Plane	A1	.015	–	–
Shoulder to Shoulder Width	E	.590	–	.625
Molded Package Width	E1	.485	–	.580
Overall Length	D	1.980	–	2.095
Tip to Seating Plane	L	.115	–	.200
Lead Thickness	c	.008	–	.015
Upper Lead Width	b1	.030	–	.070
Lower Lead Width	b	.014	–	.023
Overall Row Spacing §	eB	–	–	.700

Notes:

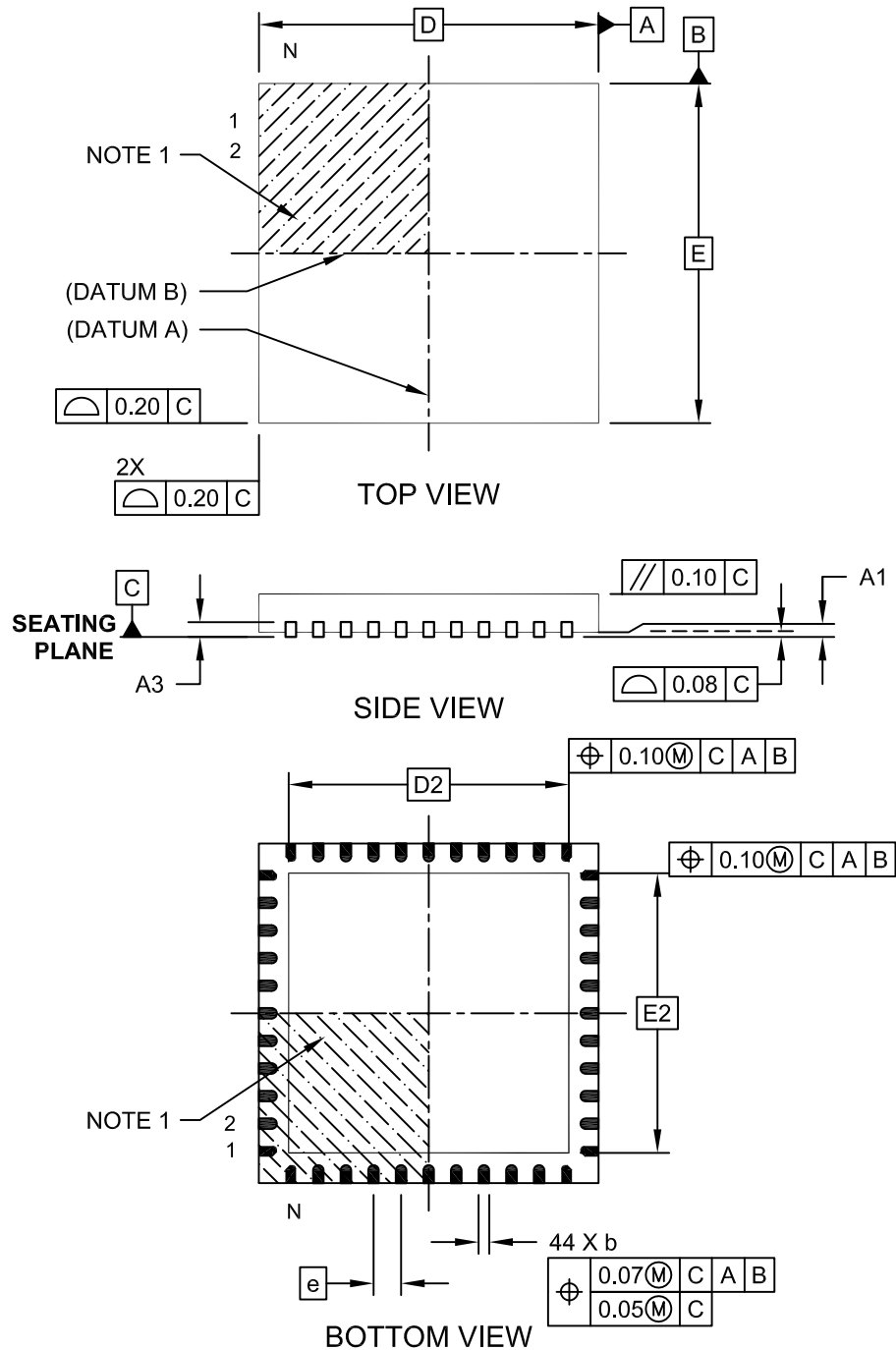
- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-016B

PIC16(L)F1788/9

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-103C Sheet 1 of 2