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#### Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I <sup>2</sup> C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Through Hole
Package / Case	40-DIP (0.600", 15.24mm)
Supplier Device Package	40-PDIP
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1789-e-p">https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1789-e-p</a>

# PIC16(L)F1788/9

**TABLE 1-2: PIC16(L)F1788 PINOUT DESCRIPTION (CONTINUED)**

Name	Function	Input Type	Output Type	Description
RA6/C2OUT <sup>(1)</sup> /OSC2/ CLKOUT/VCAP	RA6	TTL/ST	CMOS	General purpose I/O.
	C2OUT	—	CMOS	Comparator C2 output.
	OSC2	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
	CLKOUT	—	CMOS	Fosc/4 output.
	VCAP	Power	Power	Filter capacitor for Voltage Regulator.
RA7/PSMC1CLK/PSMC2CLK/ PSMC3CLK/PSMC4- CLK/OSC1/CLKIN	RA7	TTL/ST	CMOS	General purpose I/O.
	PSMC1CLK	ST	—	PSMC1 clock input.
	PSMC2CLK	ST	—	PSMC2 clock input.
	PSMC3CLK	ST	—	PSMC3 clock input.
	PSMC4CLK	ST	—	PSMC4 clock input.
	OSC1	—	XTAL	Crystal/Resonator (LP, XT, HS modes).
RB0/AN12/C2IN1+/PSMC1IN/ PSMC2IN/PSMC3IN/PSMC4IN/ CCP1 <sup>(1)</sup> /INT	RB0	TTL/ST	CMOS	General purpose I/O.
	AN12	AN	—	ADC Channel 12 input.
	C2IN1+	AN	—	Comparator C2 positive input.
	PSMC1IN	ST	—	PSMC1 Event Trigger input.
	PSMC2IN	ST	—	PSMC2 Event Trigger input.
	PSMC3IN	ST	—	PSMC3 Event Trigger input.
	PSMC4IN	ST	—	PSMC4 Event Trigger input.
	CCP1	ST	CMOS	Capture/Compare/PWM1.
RB1/AN10/C1IN3-/C2IN3-/ C3IN3-/C4IN3-/OPA2OUT	INT	ST	—	External interrupt.
	RB1	TTL/ST	CMOS	General purpose I/O.
	AN10	AN	—	ADC Channel 10 input.
	C1IN3-	AN	—	Comparator C1 negative input.
	C2IN3-	AN	—	Comparator C2 negative input.
	C3IN3-	AN	—	Comparator C3 negative input.
	C4IN3-	AN	—	Comparator C4 negative input.
RB2/AN8/OPA2IN-/CLKR/ DAC3OUT1	OPA2OUT	—	AN	Operational Amplifier 2 output.
	RB2	TTL/ST	CMOS	General purpose I/O.
	AN8	AN	—	ADC Channel 8 input.
	OPA2IN-	AN	—	Operational Amplifier 2 inverting input.
	CLKR	—	CMOS	Clock output.
RB3/AN9/C1IN2-/C2IN2-/ C3IN2-/OPA2IN+/CCP2 <sup>(1)</sup>	DAC3OUT1	—	AN	Digital-to-Analog Converter output.
	RB3	TTL/ST	CMOS	General purpose I/O.
	AN9	AN	—	ADC Channel 9 input.
	C1IN2-	AN	—	Comparator C1 negative input.
	C2IN2-	AN	—	Comparator C2 negative input.
	C3IN2-	AN	—	Comparator C3 negative input.
	OPA2IN+	AN	—	Operational Amplifier 2 non-inverting input.
	CCP2	ST	CMOS	Capture/Compare/PWM2.

**Legend:** AN = Analog input or output    CMOS = CMOS compatible input or output    OD = Open-Drain  
TTL = TTL compatible input    ST = Schmitt Trigger input with CMOS levels    I<sup>2</sup>C = Schmitt Trigger input with I<sup>2</sup>C  
HV = High Voltage    XTAL = Crystal levels

**Note 1:** Pin functions can be assigned to one of two locations via software. See **Register 13-1**.

**2:** All pins have interrupt-on-change functionality.

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**TABLE 5-5: SUMMARY OF REGISTERS ASSOCIATED WITH RESETS**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
BORCON	SBOREN	BORFS	—	—	—	—	—	BORRDY	65
PCON	STKOVF	STKUNF	—	$\overline{\text{RWDT}}$	$\overline{\text{RMCLR}}$	$\overline{\text{RI}}$	$\overline{\text{POR}}$	$\overline{\text{BOR}}$	69
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	31
WDTCON	—	—	WDTPS<4:0>					SWDTEN	114

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by Resets.

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**REGISTER 6-3: OSCTUNE: OSCILLATOR TUNING REGISTER**

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	TUN<5:0>					
bit 7							bit 0

**Legend:**

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                  x = Bit is unknown                  -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                          '0' = Bit is cleared

bit 7-6                      **Unimplemented:** Read as '0'

bit 5-0                      **TUN<5:0>:** Frequency Tuning bits

100000 = Minimum frequency

•

•

•

111111 =

000000 = Oscillator module is running at the factory-calibrated frequency.

000001 =

•

•

•

011110 =

011111 = Maximum frequency

**TABLE 6-2: SUMMARY OF REGISTERS ASSOCIATED WITH CLOCK SOURCES**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		86
OSCSTAT	T1OSCR	PLLRL	OSTS	HFIOFR	HFIOFL	MFIOFR	LFIOFR	HFIOFS	87
OSCTUNE	—	—	TUN<5:0>						88
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	99
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	103
T1CON	TMR1CS<1:0>		T1CKPS<1:0>		T1OSCEN	T1SYNC	—	TMR1ON	217

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

**TABLE 6-3: SUMMARY OF CONFIGURATION WORD WITH CLOCK SOURCES**

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0>		CPD	58
	7:0	CP	MCLRRE	PWRTE	WDTE<1:0>		FOSC<2:0>			

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by clock sources.

**Note 1:** PIC16F1788/9 only.

## 11.6 Register Definitions: Watchdog Control

**REGISTER 11-1: WDTCON: WATCHDOG TIMER CONTROL REGISTER**

U-0	U-0	R/W-0/0	R/W-1/1	R/W-0/0	R/W-1/1	R/W-1/1	R/W-0/0
—	—	WDTPS<4:0>					SWDTEN
bit 7							bit 0

**Legend:**

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-m/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-1 **WDTPS<4:0>:** Watchdog Timer Period Select bits<sup>(1)</sup>

Bit Value = Prescale Rate

11111 = Reserved. Results in minimum interval (1:32)

•  
•  
•

10011 = Reserved. Results in minimum interval (1:32)

10010 = 1:8388608 ( $2^{23}$ ) (Interval 256s nominal)

10001 = 1:4194304 ( $2^{22}$ ) (Interval 128s nominal)

10000 = 1:2097152 ( $2^{21}$ ) (Interval 64s nominal)

01111 = 1:1048576 ( $2^{20}$ ) (Interval 32s nominal)

01110 = 1:524288 ( $2^{19}$ ) (Interval 16s nominal)

01101 = 1:262144 ( $2^{18}$ ) (Interval 8s nominal)

01100 = 1:131072 ( $2^{17}$ ) (Interval 4s nominal)

01011 = 1:65536 (Interval 2s nominal) (Reset value)

01010 = 1:32768 (Interval 1s nominal)

01001 = 1:16384 (Interval 512 ms nominal)

01000 = 1:8192 (Interval 256 ms nominal)

00111 = 1:4096 (Interval 128 ms nominal)

00110 = 1:2048 (Interval 64 ms nominal)

00101 = 1:1024 (Interval 32 ms nominal)

00100 = 1:512 (Interval 16 ms nominal)

00011 = 1:256 (Interval 8 ms nominal)

00010 = 1:128 (Interval 4 ms nominal)

00001 = 1:64 (Interval 2 ms nominal)

00000 = 1:32 (Interval 1 ms nominal)

bit 0 **SWDTEN:** Software Enable/Disable for Watchdog Timer bit

If WDTE<1:0> = 1x:

This bit is ignored.

If WDTE<1:0> = 01:

1 = WDT is turned on

0 = WDT is turned off

If WDTE<1:0> = 00:

This bit is ignored.

**Note 1:** Times are approximate. WDT time is based on 31 kHz LFINTOSC.

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**TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		86
STATUS	—	—	—	$\overline{TO}$	$\overline{PD}$	Z	DC	C	31
WDTCON	—	—	WDTPS<4:0>					SWDTEN	114

**Legend:** x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

**TABLE 11-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER**

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	$\overline{CLKOUTEN}$	BOREN<1:0>		$\overline{CPD}$	58
	7:0	$\overline{CP}$	MCLRE	$\overline{PWRTE}$	WDTE<1:0>		FOSC<2:0>			

**Legend:** — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

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**TABLE 13-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELB	—	ANSB6	ANSB5	ANSB4	ANSB3	ANSB2	ANSB1	ANSB0	143
INLVLB	INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0	144
LATB	LATB7	LATB6	LATB5	LATB4	LATB3	LATB2	LATB1	LATB0	142
ODCONB	ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0	144
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	142
SLRCONB	SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0	144
TRISB	TRISB7	TRISB6	TRISB5	TRISB4	TRISB3	TRISB2	TRISB1	TRISB0	142
WPUB	WPUB7	WPUB6	WPUB5	WPUB4	WPUB3	WPUB2	WPUB1	WPUB0	143

**Legend:** x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by PORTB.

## 23.6.2 TIMER1 GATE SOURCE SELECTION

Timer1 gate source selections are shown in Table 23-4. Source selection is controlled by the T1GSS bits of the T1GCON register. The polarity for each available source is also selectable. Polarity selection is controlled by the T1GPOL bit of the T1GCON register.

**TABLE 23-4: TIMER1 GATE SOURCES**

T1GSS	Timer1 Gate Source
00	Timer1 Gate Pin
01	Overflow of Timer0 (TMR0 increments from FFh to 00h)
10	Comparator 1 Output sync_C1OUT (optionally Timer1 synchronized output)
11	Comparator 2 Output sync_C2OUT (optionally Timer1 synchronized output)

### 23.6.2.1 T1G Pin Gate Operation

The T1G pin is one source for Timer1 gate control. It can be used to supply an external source to the Timer1 gate circuitry.

### 23.6.2.2 Timer0 Overflow Gate Operation

When Timer0 increments from FFh to 00h, a low-to-high pulse will automatically be generated and internally supplied to the Timer1 gate circuitry.

### 23.6.2.3 Comparator C1 Gate Operation

The output resulting from a Comparator 1 operation can be selected as a source for Timer1 gate control. The Comparator 1 output (sync\_C1OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see **Section 21.4.1 “Comparator Output Synchronization”**.

### 23.6.2.4 Comparator C2 Gate Operation

The output resulting from a Comparator 2 operation can be selected as a source for Timer1 gate control. The Comparator 2 output (sync\_C2OUT) can be synchronized to the Timer1 clock or left asynchronous. For more information see **Section 21.4.1 “Comparator Output Synchronization”**.

## 23.6.3 TIMER1 GATE TOGGLE MODE

When Timer1 Gate Toggle mode is enabled, it is possible to measure the full-cycle length of a Timer1 gate signal, as opposed to the duration of a single level pulse.

The Timer1 gate source is routed through a flip-flop that changes state on every incrementing edge of the signal. See Figure 23-4 for timing details.

Timer1 Gate Toggle mode is enabled by setting the T1GTM bit of the T1GCON register. When the T1GTM bit is cleared, the flip-flop is cleared and held clear. This is necessary in order to control which edge is measured.

**Note:** Enabling Toggle mode at the same time as changing the gate polarity may result in indeterminate operation.

## 23.6.4 TIMER1 GATE SINGLE-PULSE MODE

When Timer1 Gate Single-Pulse mode is enabled, it is possible to capture a single-pulse gate event. Timer1 Gate Single-Pulse mode is enabled by first setting the T1GSPM bit in the T1GCON register. Next, the T1GGO/DONE bit in the T1GCON register must be set. The Timer1 will be fully enabled on the next incrementing edge. On the next trailing edge of the pulse, the T1GGO/DONE bit will automatically be cleared. No other gate events will be allowed to increment Timer1 until the T1GGO/DONE bit is once again set in software. See Figure 23-5 for timing details.

If the Single-Pulse Gate mode is disabled by clearing the T1GSPM bit in the T1GCON register, the T1GGO/DONE bit should also be cleared.

Enabling the Toggle mode and the Single-Pulse mode simultaneously will permit both sections to work together. This allows the cycle times on the Timer1 gate source to be measured. See Figure 23-6 for timing details.

## 23.6.5 TIMER1 GATE VALUE

When Timer1 Gate Value Status is utilized, it is possible to read the most current level of the gate control value. The value is accessible by reading the T1GVAL bit in the T1GCON register. The T1GVAL bit is valid even when the Timer1 gate is not enabled (TMR1GE bit is cleared).

## 23.6.6 TIMER1 GATE EVENT INTERRUPT

When Timer1 Gate Event Interrupt is enabled, it is possible to generate an interrupt upon the completion of a gate event. When the falling edge of T1GVAL occurs, the TMR1GIF flag bit in the PIR1 register will be set. If the TMR1GIE bit in the PIE1 register is set, then an interrupt will be recognized.

The TMR1GIF flag bit operates even when the Timer1 gate is not enabled (TMR1GE bit is cleared).



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## REGISTER 26-3: PSMC1SYNC: PSMC1 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P1POFST	P1PRPOL	P1DCPOL	—	—	P1SYNC<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                      x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                      '0' = Bit is cleared

- bit 7                      **P1POFST:** PSMC1 Phase Offset Control bit  
1 = sync\_out source is phase event and latch set source is synchronous period event  
0 = sync\_out source is period event and latch set source is phase event
- bit 6                      **P1PRPOL:** PSMC1 Period Polarity Event Control bit  
1 = Selected asynchronous period event inputs are inverted  
0 = Selected asynchronous period event inputs are not inverted
- bit 5                      **P1DCPOL:** PSMC1 Duty-cycle Event Polarity Control bit  
1 = Selected asynchronous duty-cycle event inputs are inverted  
0 = Selected asynchronous duty-cycle event inputs are not inverted
- bit 4-3                      **Unimplemented:** Read as '0'
- bit 2-0                      **P1SYNC<2:0>:** PSMC1 Period Synchronization Mode bits  
1xx = Reserved - Do not use  
100 = PSMC1 is synchronized with the PSMC4 module (sync\_in comes from PSMC4 sync\_out)  
011 = PSMC1 is synchronized with the PSMC3 module (sync\_in comes from PSMC3 sync\_out)  
010 = PSMC1 is synchronized with the PSMC2 module (sync\_in comes from PSMC3 sync\_out)  
001 = PSMC1 is synchronized with the PSMC1 module (sync\_in comes from PSMC3 sync\_out)  
000 = PSMC1 is synchronized with period event

## REGISTER 26-4: PSMC2SYNC: PSMC2 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P2POFST	P2PRPOL	P2DCPOL	—	—	P2SYNC<2:0>		
bit 7							bit 0

### Legend:

R = Readable bit                      W = Writable bit                      U = Unimplemented bit, read as '0'  
u = Bit is unchanged                      x = Bit is unknown                      -n/n = Value at POR and BOR/Value at all other Resets  
'1' = Bit is set                      '0' = Bit is cleared

- bit 7                      **P2POFST:** PSMC2 Phase Offset Control bit  
1 = sync\_out source is phase event and latch set source is synchronous period event  
0 = sync\_out source is period event and latch set source is phase event
- bit 6                      **P2PRPOL:** PSMC2 Period Polarity Event Control bit  
1 = Selected asynchronous period event inputs are inverted  
0 = Selected asynchronous period event inputs are not inverted
- bit 5                      **P2DCPOL:** PSMC2 Duty-cycle Event Polarity Control bit  
1 = Selected asynchronous duty-cycle event inputs are inverted  
0 = Selected asynchronous duty-cycle event inputs are not inverted
- bit 4-3                      **Unimplemented:** Read as '0'
- bit 2-0                      **P2SYNC<2:0>:** PSMC2 Period Synchronization Mode bits  
1xx = Reserved - Do not use  
100 = PSMC2 is synchronized with the PSMC4 module (sync\_in comes from PSMC4 sync\_out)  
011 = PSMC2 is synchronized with the PSMC3 module (sync\_in comes from PSMC3 sync\_out)  
010 = PSMC2 is synchronized with the PSMC2 module (sync\_in comes from PSMC3 sync\_out)  
001 = PSMC2 is synchronized with the PSMC1 module (sync\_in comes from PSMC3 sync\_out)  
000 = PSMC2 is synchronized with period event

# PIC16(L)F1788/9

## REGISTER 26-23: PSMCxDCL: PSMC DUTY CYCLE COUNT LOW BYTE REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxDCL<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0      **PSMCxDCL<7:0>**: 16-bit Duty Cycle Count Least Significant bits  
= PSMCxDC<7:0>

## REGISTER 26-24: PSMCxDCH: PSMC DUTY CYCLE COUNT HIGH REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
PSMCxDCH<7:0>							
bit 7							bit 0

### Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7-0      **PSMCxDCH<7:0>**: 16-bit Duty Cycle Count Most Significant bits  
= PSMCxDC<15:8>

## 27.2.6 SPI OPERATION IN SLEEP MODE

In SPI Master mode, module clocks may be operating at a different speed than when in Full-Power mode; in the case of the Sleep mode, all clocks are halted.

Special care must be taken by the user when the MSSP clock is much faster than the system clock.

In Slave mode, when MSSP interrupts are enabled, after the master completes sending data, an MSSP interrupt will wake the controller from Sleep.

If an exit from Sleep mode is not desired, MSSP interrupts should be disabled.

In SPI Master mode, when the Sleep mode is selected, all module clocks are halted and the transmission/reception will remain in that state until the device wakes. After the device returns to Run mode, the module will resume transmitting and receiving data.

In SPI Slave mode, the SPI Transmit/Receive Shift register operates asynchronously to the device. This allows the device to be placed in Sleep mode and data to be shifted into the SPI Transmit/Receive Shift register. When all eight bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device.

**TABLE 27-1: SUMMARY OF REGISTERS ASSOCIATED WITH SPI OPERATION**

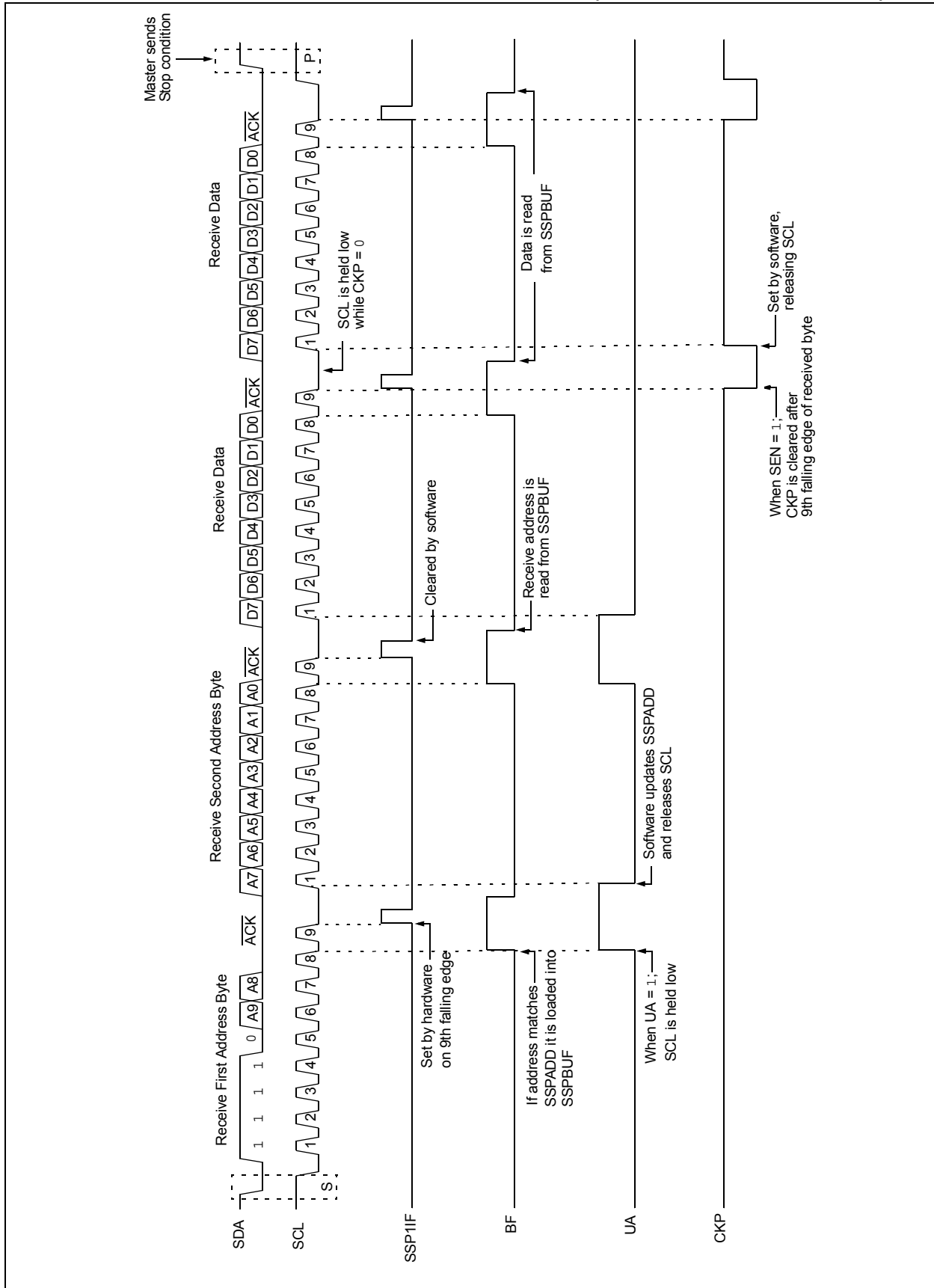
Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
ANSELA	ANSA7	—	ANSA5	ANSA4	ANSA3	ANSA2	ANSA1	ANSA0	137
APFCON1	C2OUTSEL	CCP1SEL	SDOSEL	SCKSEL	SDISEL	TXSEL	RXSEL	CCP2SEL	132
INTCON	GIE	PEIE	TMR0IE	INTE	IOCIE	TMR0IF	INTF	IOCIF	97
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	102
SSP1BUF	Synchronous Serial Port Receive Buffer/Transmit Register								294*
SSP1CON1	WCOL	SSPOV	SSPEN	CKP	SSPM<3:0>				340
SSP1CON3	ACKTIM	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	342
SSP1STAT	SMP	CKE	D/ $\bar{A}$	P	S	R/ $\bar{W}$	UA	BF	338
TRISA	TRISA7	TRISA6	TRISA5	TRISA4	TRISA3	TRISA2	TRISA1	TRISA0	136
TRISC	TRISC7	TRISC6	TRISC5	TRISC4	TRISC3	TRISC2	TRISC1	TRISA0	147

**Legend:** — = Unimplemented location, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

\* Page provides register information.

**Note 1:** PIC16(L)F1789 only.

**FIGURE 27-20: I<sup>2</sup>C SLAVE, 10-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)**



## 27.6.7 I<sup>2</sup>C MASTER MODE RECEPTION

Master mode reception is enabled by programming the Receive Enable bit, RCEN bit of the SSPCON2 register.

**Note:** The MSSP module must be in an Idle state before the RCEN bit is set or the RCEN bit will be disregarded.

The Baud Rate Generator begins counting and on each rollover, the state of the SCL pin changes (high-to-low/low-to-high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSP1IF flag bit is set and the Baud Rate Generator is suspended from counting, holding SCL low. The MSSP is now in Idle state awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge bit at the end of reception by setting the Acknowledge Sequence Enable, ACKEN bit of the SSPCON2 register.

### 27.6.7.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

### 27.6.7.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when eight bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

### 27.6.7.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write does not occur).

### 27.6.7.4 Typical Receive Sequence:

1. The user generates a Start condition by setting the SEN bit of the SSPCON2 register.
2. SSP1IF is set by hardware on completion of the Start.
3. SSP1IF is cleared by software.
4. User writes SSPBUF with the slave address to transmit and the R/W bit set.
5. Address is shifted out the SDA pin until all eight bits are transmitted. Transmission begins as soon as SSPBUF is written to.
6. The MSSP module shifts in the  $\overline{\text{ACK}}$  bit from the slave device and writes its value into the ACKSTAT bit of the SSPCON2 register.
7. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSP1IF bit.
8. User sets the RCEN bit of the SSPCON2 register and the master clocks in a byte from the slave.
9. After the 8th falling edge of SCL, SSP1IF and BF are set.
10. User clears the SSP1IF bit and reads the received byte from SSPBUF, which clears the BF flag.
11. The user either clears the SSPCON2 register's ACKDT bit to receive another byte or sets the ACKDT bit to suppress further data and then initiates the acknowledge sequence by setting the ACKEN bit.
12. Master's ACK or  $\overline{\text{ACK}}$  is clocked out to the slave and SSP1IF is set.
13. User clears SSP1IF.
14. Steps 8-13 are repeated for each received byte from the slave.
15. If the ACKST bit was set in step 11 then the user can send a STOP to release the bus.

## 28.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

### 28.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see **Section 28.5.2.4 “Synchronous Slave Reception Set-up:”**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

### 28.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave transmission (see **Section 28.5.2.2 “Synchronous Slave Transmission Set-up:”**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the SLEEP instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

### 28.6.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 “Alternate Pin Function”** for more information.

# PIC16(L)F1788/9

**TABLE 30-4: ENHANCED MID-RANGE INSTRUCTION SET (CONTINUED)**

Mnemonic, Operands		Description	Cycles	14-Bit Opcode				Status Affected	Notes
				MSb		LSb			
CONTROL OPERATIONS									
BRA	k	Relative Branch	2	11	001k	kkkk	kkkk		
BRW	–	Relative Branch with W	2	00	0000	0000	1011		
CALL	k	Call Subroutine	2	10	0kkk	kkkk	kkkk		
CALLW	–	Call Subroutine with W	2	00	0000	0000	1010		
GOTO	k	Go to address	2	10	1kkk	kkkk	kkkk		
RETFIE	k	Return from interrupt	2	00	0000	0000	1001		
RETLW	k	Return with literal in W	2	11	0100	kkkk	kkkk		
RETURN	–	Return from Subroutine	2	00	0000	0000	1000		
INHERENT OPERATIONS									
CLRWDT	–	Clear Watchdog Timer	1	00	0000	0110	0100	$\overline{TO}, \overline{PD}$	
NOP	–	No Operation	1	00	0000	0000	0000		
OPTION	–	Load OPTION_REG register with W	1	00	0000	0110	0010		
RESET	–	Software device Reset	1	00	0000	0000	0001	$\overline{TO}, \overline{PD}$	
SLEEP	–	Go into Standby mode	1	00	0000	0110	0011		
TRIS	f	Load TRIS register with W	1	00	0000	0110	0fff		
C-COMPILER OPTIMIZED									
ADDFSR	n, k	Add Literal k to FSRn	1	11	0001	0nkk	kkkk	Z	2, 3
MOVIW	n mm	Move Indirect FSRn to W with pre/post inc/dec modifier, mm	1	00	0000	0001	0nmm kkkk		
	k[n]	Move INDFn to W, Indexed Indirect.	1	11	1111	0nkk	1nmm	Z	2
MOVWI	n mm	Move W to Indirect FSRn with pre/post inc/dec modifier, mm	1	00	0000	0001	kkkk		
	k[n]	Move W to INDFn, Indexed Indirect.	1	11	1111	1nkk			2

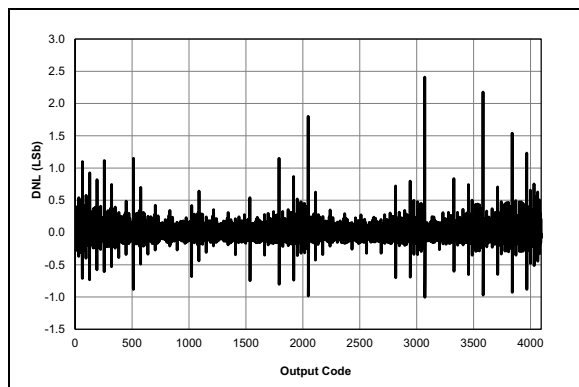
- Note 1:** If the Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 2:** If this instruction addresses an INDF register and the MSb of the corresponding FSR is set, this instruction will require one additional instruction cycle.
- 3:** See Table in the MOVIW and MOVWI instruction descriptions.

## 30.2 Instruction Descriptions

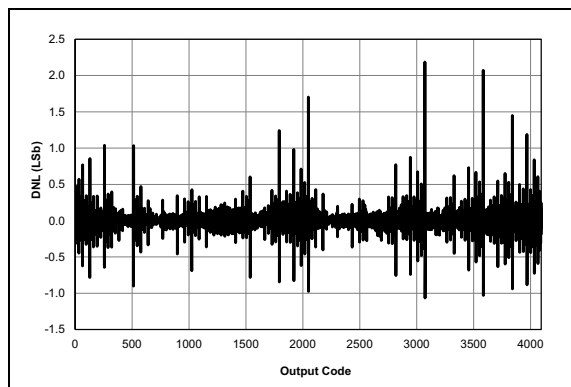
ADDFSR		ADDLW	
Add Literal to FSRn		Add literal and W	
Syntax:	[ <i>label</i> ] ADDFSR FSRn, k	Syntax:	[ <i>label</i> ] ADDLW k
Operands:	-32 ≤ k ≤ 31 n ∈ [ 0, 1 ]	Operands:	0 ≤ k ≤ 255
Operation:	FSR(n) + k → FSR(n)	Operation:	(W) + k → (W)
Status Affected:	None	Status Affected:	C, DC, Z
Description:	The signed 6-bit literal 'k' is added to the contents of the FSRnH:FSRnL register pair.	Description:	The contents of the W register are added to the 8-bit literal 'k' and the result is placed in the W register.
	FSRn is limited to the range 0000h - FFFFh. Moving beyond these bounds will cause the FSR to wrap-around.		

# PIC16(L)F1788/9

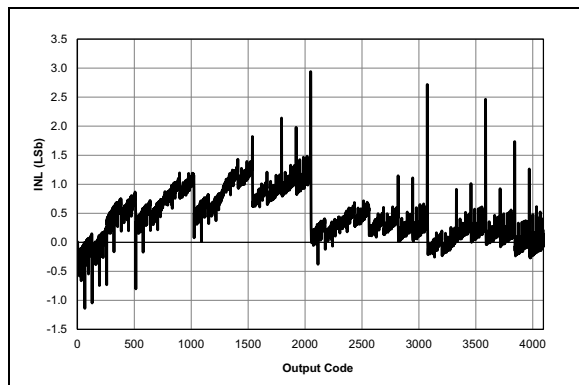
**Note:** Unless otherwise noted,  $V_{IN} = 5V$ ,  $F_{OSC} = 300\text{ kHz}$ ,  $C_{IN} = 0.1\text{ }\mu F$ ,  $T_A = 25^\circ C$ .



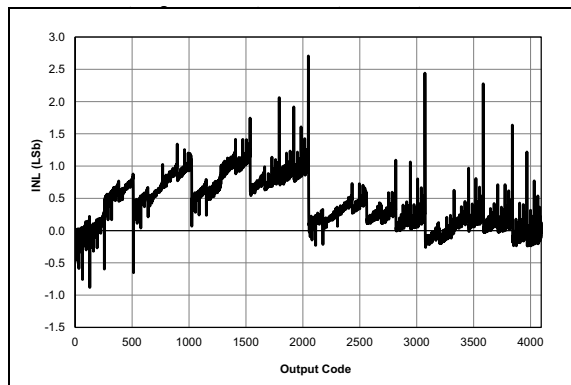
**FIGURE 32-85:** ADC 12-bit Mode, Single-Ended DNL,  $V_{DD} = 3.0V$ ,  $T_{AD} = 1\text{ }\mu s$ ,  $25^\circ C$ .



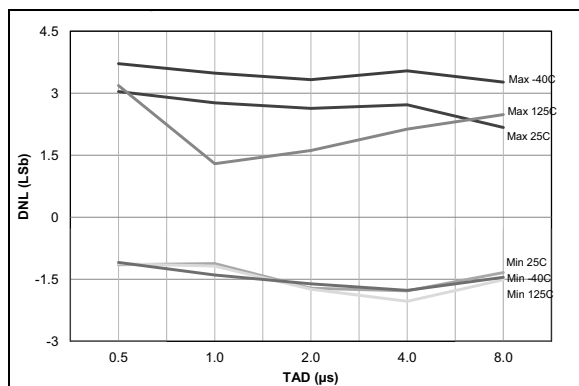
**FIGURE 32-86:** ADC 12-bit Mode, Single-Ended DNL,  $V_{DD} = 3.0V$ ,  $T_{AD} = 4\text{ }\mu s$ ,  $25^\circ C$ .



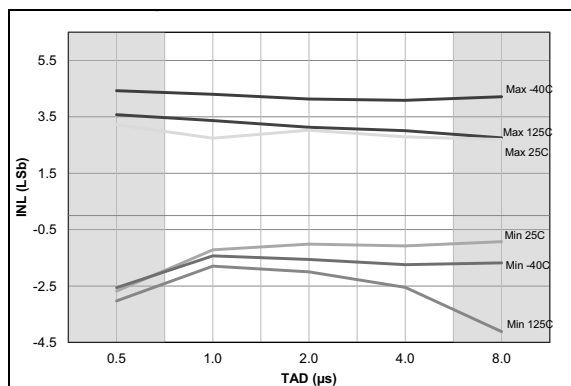
**FIGURE 32-87:** ADC 12-bit Mode, Single-Ended INL,  $V_{DD} = 3.0V$ ,  $T_{AD} = 1\text{ }\mu s$ ,  $25^\circ C$ .



**FIGURE 32-88:** ADC 12-bit Mode, Single-Ended INL,  $V_{DD} = 3.0V$ ,  $T_{AD} = 4\text{ }\mu s$ ,  $25^\circ C$ .



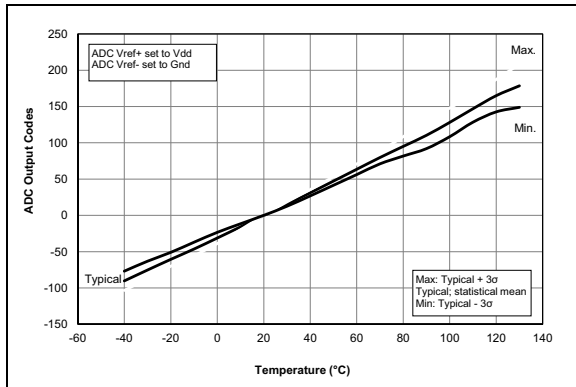
**FIGURE 32-89:** ADC 12-bit Mode, Single-Ended DNL,  $V_{DD} = 3.0V$ ,  $V_{REF} = 3.0V$ .



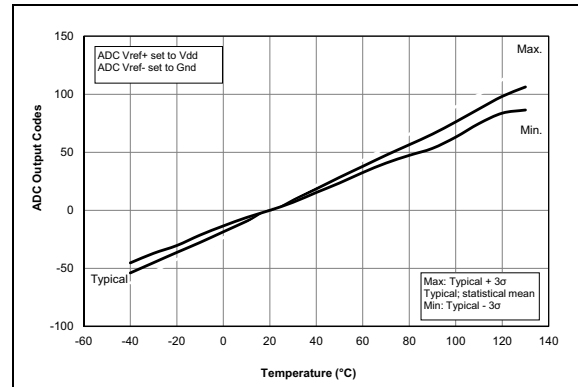
**FIGURE 32-90:** ADC 12-bit Mode, Single-Ended INL,  $V_{DD} = 3.0V$ ,  $V_{REF} = 3.0V$ .



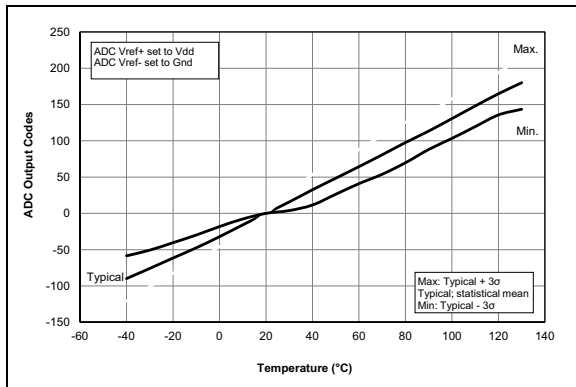
**Note:** Unless otherwise noted,  $V_{IN} = 5V$ ,  $F_{OSC} = 300\text{ kHz}$ ,  $C_{IN} = 0.1\text{ }\mu F$ ,  $T_A = 25^\circ C$ .



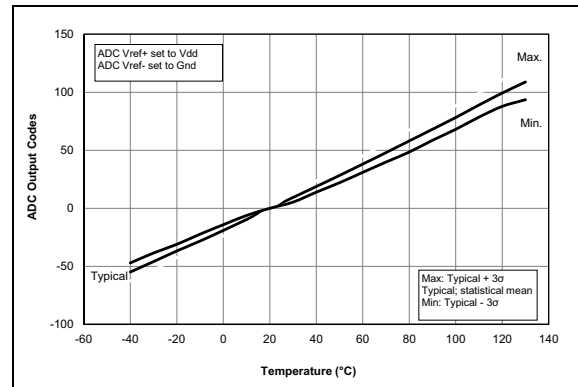
**FIGURE 32-103:** Temp. Indicator Slope Normalized to  $20^\circ C$ , High Range,  $V_{DD} = 3.6V$ , PIC16F1788/9 Only.



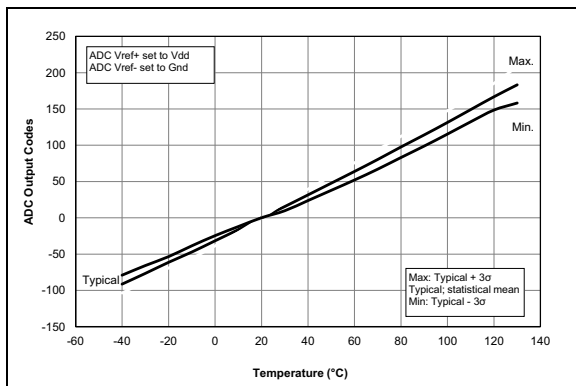
**FIGURE 32-104:** Temp. Indicator Slope Normalized to  $20^\circ C$ , Low Range,  $V_{DD} = 3.0V$ , PIC16F1788/9 Only.



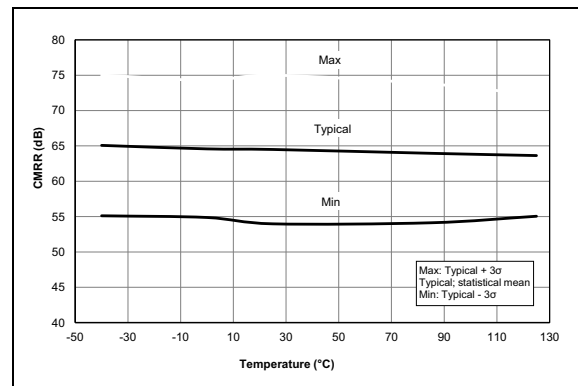
**FIGURE 32-105:** Temp. Indicator Slope Normalized to  $20^\circ C$ , Low Range,  $V_{DD} = 1.8V$ , PIC16LF1788/9 Only.



**FIGURE 32-106:** Temp. Indicator Slope Normalized to  $20^\circ C$ , Low Range,  $V_{DD} = 3.0V$ , PIC16LF1788/9 Only.



**FIGURE 32-107:** Temp. Indicator Slope Normalized to  $20^\circ C$ , High Range,  $V_{DD} = 3.6V$ , PIC16LF1788/9 Only.

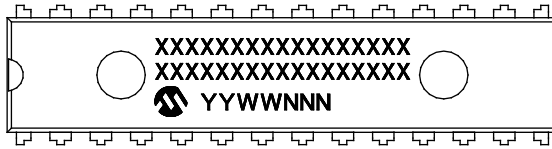


**FIGURE 32-108:** Op Amp, Common Mode Rejection Ratio (CMRR),  $V_{DD} = 3.0V$ .

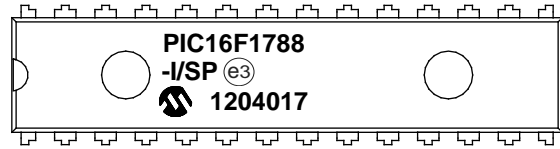
## 34.0 PACKAGING INFORMATION

### 34.1 Package Marking Information

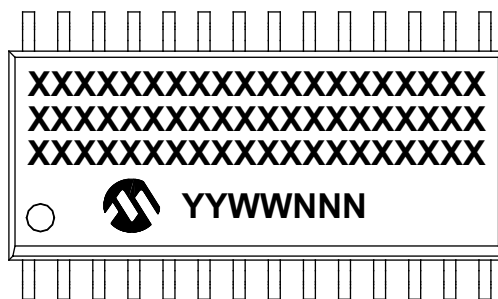
28-Lead SPDIP (.300")



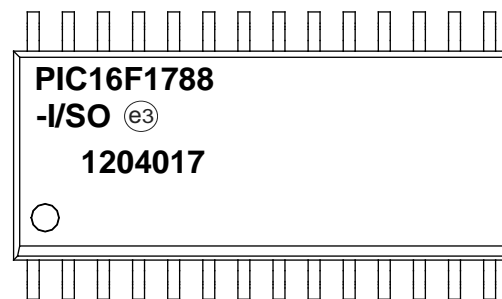
Example



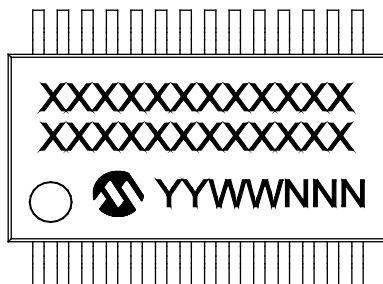
28-Lead SOIC (7.50 mm)



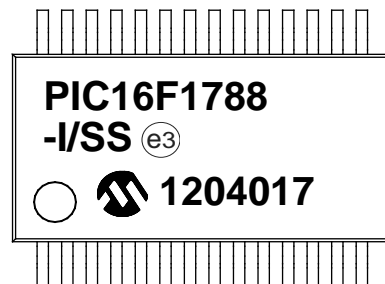
Example



28-Lead SSOP (5.30 mm)



Example



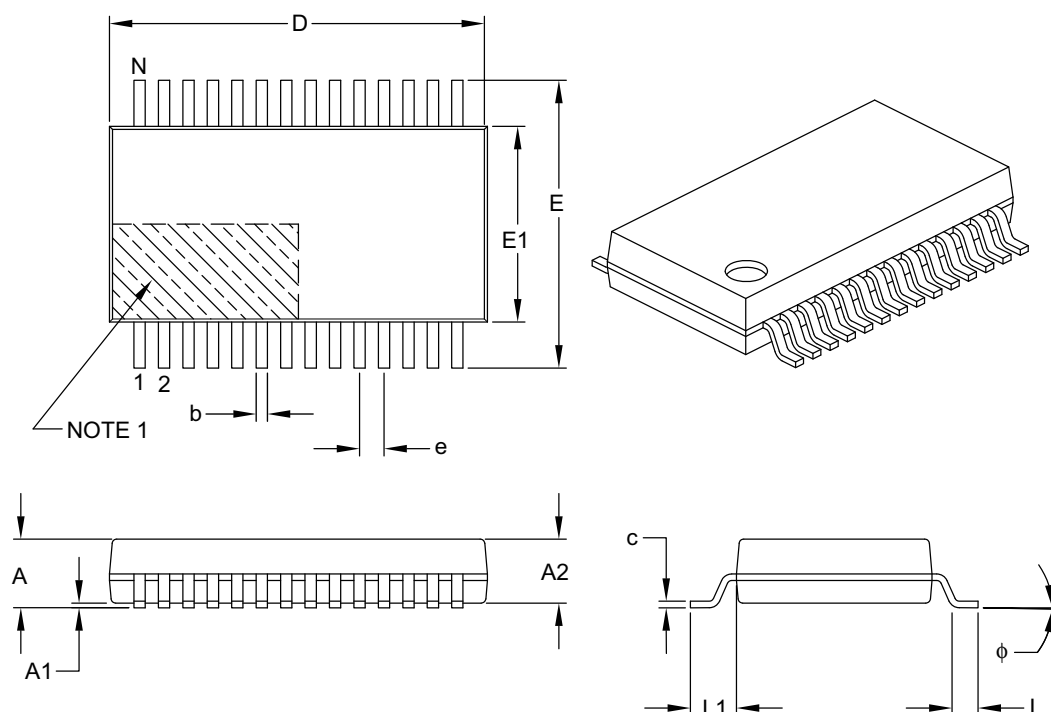
<b>Legend:</b>	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week '01')
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC® designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator (e3) can be found on the outer packaging for this package.

**Note:** In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

# PIC16(L)F1788/9

## 28-Lead Plastic Shrink Small Outline (SS) – 5.30 mm Body [SSOP]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	28		
Pitch	e	0.65 BSC		
Overall Height	A	–	–	2.00
Molded Package Thickness	A2	1.65	1.75	1.85
Standoff	A1	0.05	–	–
Overall Width	E	7.40	7.80	8.20
Molded Package Width	E1	5.00	5.30	5.60
Overall Length	D	9.90	10.20	10.50
Foot Length	L	0.55	0.75	0.95
Footprint	L1	1.25 REF		
Lead Thickness	c	0.09	–	0.25
Foot Angle	φ	0°	4°	8°
Lead Width	b	0.22	–	0.38

### Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.20 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

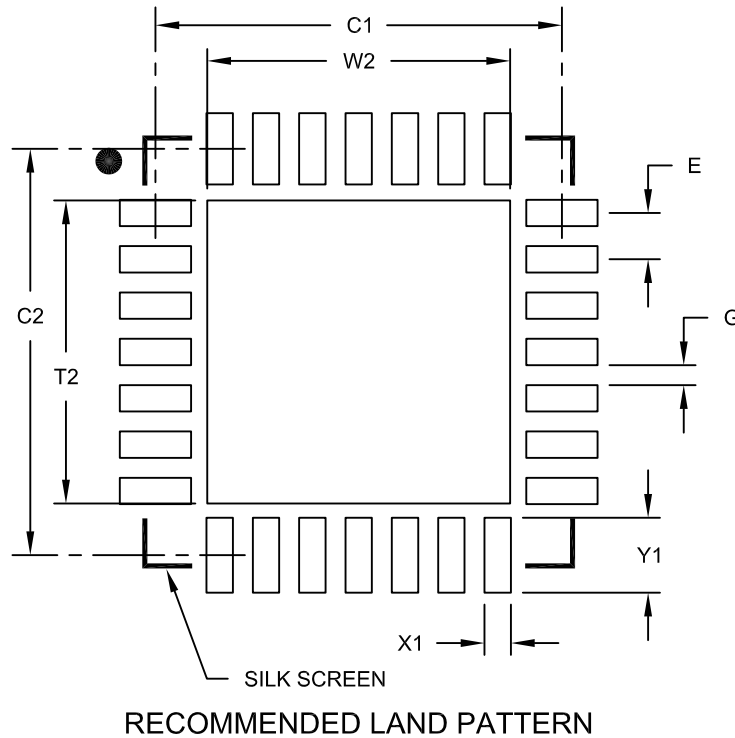
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-073B

## 28-Lead Plastic Quad Flat, No Lead Package (ML) – 6x6 mm Body [QFN] with 0.55 mm Contact Length

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.25
Optional Center Pad Length	T2			4.25
Contact Pad Spacing	C1		5.70	
Contact Pad Spacing	C2		5.70	
Contact Pad Width (X28)	X1			0.37
Contact Pad Length (X28)	Y1			1.00
Distance Between Pads	G	0.20		

**Notes:**

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2105A

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- **General Technical Support** – Frequently Asked Questions (FAQ), technical support requests, online discussion groups, Microchip consultant program member listing
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