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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I ² C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	44-VQFN Exposed Pad
Supplier Device Package	44-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1789-i-ml

EXAMPLE 3-2: ACCESSING PROGRAM MEMORY VIA FSR

```
constants
    DW    DATA0    ;First constant
    DW    DATA1    ;Second constant
    DW    DATA2
    DW    DATA3
my_function
    ;... LOTS OF CODE...
    MOVLW  DATA_INDEX
    ADDLW  LOW constants
    MOVWF  FSR1L
    MOVLW  HIGH constants ;MSb is set
    automatically
    MOVWF  FSR1H
    BTFSC  STATUS,C      ;carry from ADDLW?
    INCF   FSR1H,f        ;yes
    MOVIW  0[FSR1]
;THE PROGRAM MEMORY IS IN W
```

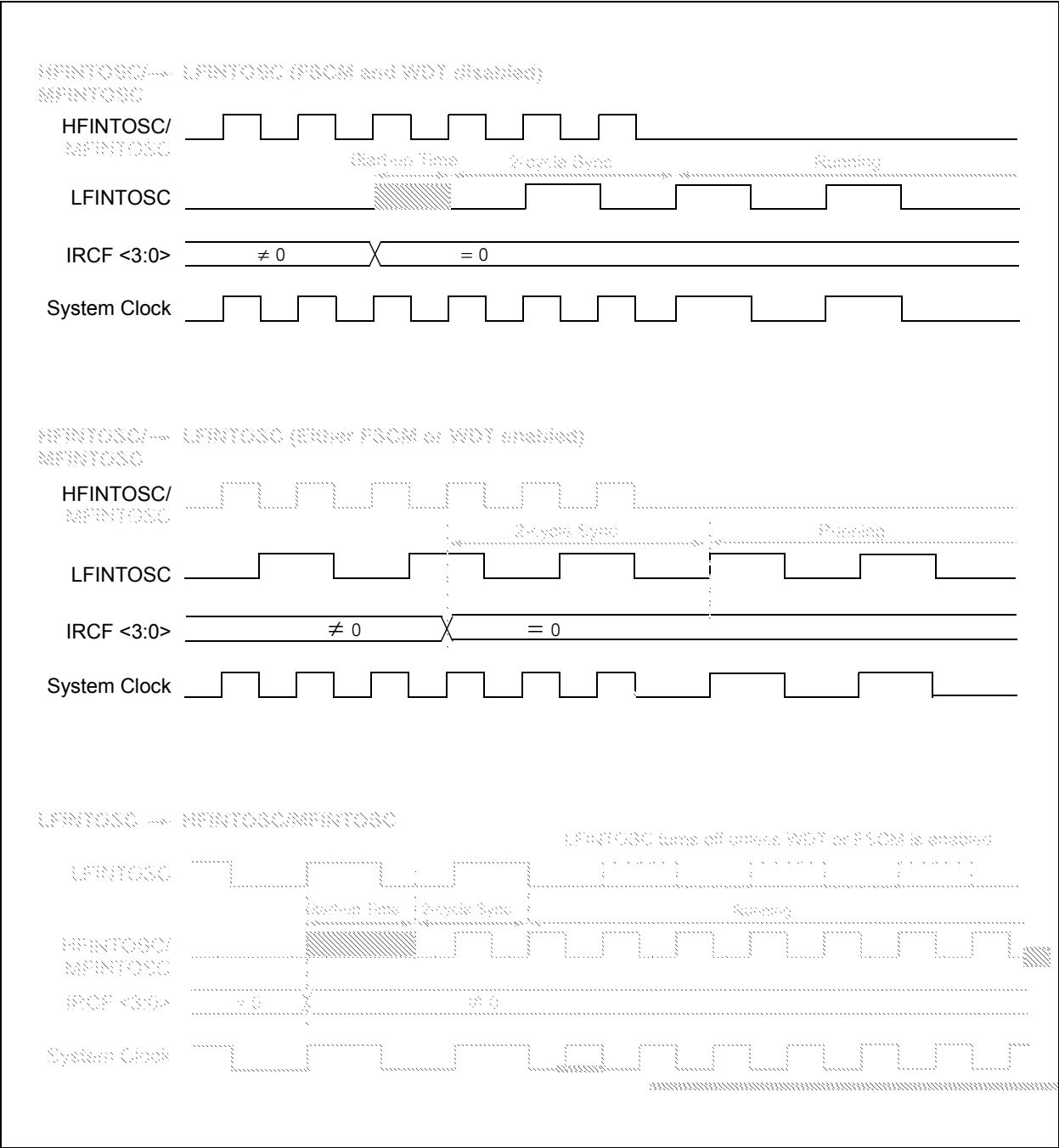
TABLE 3-5: PIC16(L)F1788/9 MEMORY MAP (BANKS 8-28)

BANK 8		BANK 9		BANK 10		BANK 11		BANK 12		BANK 13		BANK 14		BANK 15	
400h	Core Registers (Table 3-2)	480h	Core Registers (Table 3-2)	500h	Core Registers (Table 3-2)	580h	Core Registers (Table 3-2)	600h	Core Registers (Table 3-2)	680h	Core Registers (Table 3-2)	700h	Core Registers (Table 3-2)	780h	Core Registers (Table 3-2)
40Bh	Unimplemented Read as '0'	48Bh	Unimplemented Read as '0'	50Bh	See Table 3-6	58Bh	See Table 3-7	60Bh	Unimplemented Read as '0'	68Bh	Unimplemented Read as '0'	70Bh	Unimplemented Read as '0'	78Bh	Unimplemented Read as '0'
40Ch		48Ch		50Ch		58Ch		60Ch		68Ch		70Ch		78Ch	
41Fh	General Purpose Register 80 Bytes	49Fh	General Purpose Register 80 Bytes	51Fh	General Purpose Register 80 Bytes	59Fh	General Purpose Register 80 Bytes	61Fh	General Purpose Register 80 Bytes	69Fh	General Purpose Register 80 Bytes	71Fh	General Purpose Register 80 Bytes	79Fh	General Purpose Register 80 Bytes
420h		4A0h		520h		5A0h		620h		6A0h		720h		7A0h	
46Fh	Common RAM (Accesses 70h – 7Fh)	4EFh	Common RAM (Accesses 70h – 7Fh)	56Fh	Common RAM (Accesses 70h – 7Fh)	5EFh	Common RAM (Accesses 70h – 7Fh)	66Fh	Common RAM (Accesses 70h – 7Fh)	6EFh	Common RAM (Accesses 70h – 7Fh)	76Fh	Common RAM (Accesses 70h – 7Fh)	7EFh	Common RAM (Accesses 70h – 7Fh)
470h		4F0h		570h		5F0h		670h		6F0h		770h		7F0h	
47Fh		4FFh		57Fh		5FFh		67Fh		6FFh		77Fh		7FFh	
BANK 16		BANK 17		BANK 18		BANK 19		BANK 20		BANK 21		BANK 22		BANK 23	
800h	Core Registers (Table 3-2)	880h	Core Registers (Table 3-2)	900h	Core Registers (Table 3-2)	980h	Core Registers (Table 3-2)	A00h	Core Registers (Table 3-2)	A80h	Core Registers (Table 3-2)	B00h	Core Registers (Table 3-2)	B80h	Core Registers (Table 3-2)
80Bh	Unimplemented Read as '0'	88Bh	Unimplemented Read as '0'	90Bh	Unimplemented Read as '0'	98Bh	Unimplemented Read as '0'	A0Bh	Unimplemented Read as '0'	A8Bh	Unimplemented Read as '0'	B0Bh	Unimplemented Read as '0'	B8Bh	Unimplemented Read as '0'
80Ch		88Ch		90Ch		98Ch		A0Ch		A8Ch		B0Ch		B8Ch	
81Fh	General Purpose Register 80 Bytes	89Fh	General Purpose Register 80 Bytes	91Fh	General Purpose Register 80 Bytes	99Fh	General Purpose Register 80 Bytes	A1Fh	General Purpose Register 80 Bytes	A9Fh	General Purpose Register 80 Bytes	B1Fh	General Purpose Register 80 Bytes	B9Fh	General Purpose Register 80 Bytes
820h		8A0h		920h		9A0h		A20h		AA0h		B20h		BA0h	
86Fh	Common RAM (Accesses 70h – 7Fh)	8EFh	Common RAM (Accesses 70h – 7Fh)	96Fh	Common RAM (Accesses 70h – 7Fh)	9EFh	Common RAM (Accesses 70h – 7Fh)	A6Fh	Common RAM (Accesses 70h – 7Fh)	AEFh	Common RAM (Accesses 70h – 7Fh)	B6Fh	Common RAM (Accesses 70h – 7Fh)	BEFh	Common RAM (Accesses 70h – 7Fh)
870h		8F0h		970h		9F0h		A70h		AF0h		B70h		BF0h	
87Fh		8FFh		97Fh		9FFh		A7Fh		AFFh		B7Fh		BFFh	
BANK 24		BANK 25		BANK 26		BANK 27		BANK 28		BANK 29		BANK 30		BANK 31	
C00h	Core Registers (Table 3-2)	C80h	Core Registers (Table 3-2)	D00h	Core Registers (Table 3-2)	D80h	Core Registers (Table 3-2)	E00h	Core Registers (Table 3-2)	E80h	Core Registers (Table 3-2)	F00h	Core Registers (Table 3-2)	F80h	Core Registers (Table 3-2)
C0Bh	Unimplemented Read as '0'	C8Bh	Unimplemented Read as '0'	D0Bh		D8Bh		E0Bh		E8Bh		F0Bh		F8Bh	
C0Ch		C8Ch		D0Ch		D8Ch		E0Ch		E8Ch		F0Ch		F8Ch	
C1Fh	General Purpose Register 80 Bytes	C9Fh	General Purpose Register 32 Bytes	Unimplemented Read as '0'		Unimplemented Read as '0'		Unimplemented Read as '0'		See Figure 3-9	See Figure 3-9	See Figure 3-10	See Figure 3-10	See Figure 3-8	See Figure 3-8
C20h		CA0h													
	CC0h	Unimplemented Read as '0'													
C6Fh		CEFh													
C70h	Common RAM (Accesses 70h – 7Fh)	CF0h	Common RAM (Accesses 70h – 7Fh)	D70h	Common RAM (Accesses 70h – 7Fh)	DF0h	Common RAM (Accesses 70h – 7Fh)	E70h	Common RAM (Accesses 70h – 7Fh)	EF0h	Common RAM (Accesses 70h – 7Fh)	F70h	Common RAM (Accesses 70h – 7Fh)	FF0h	Common RAM (Accesses 70h – 7Fh)
C7Fh		CFFh		D7Fh		DFh		E7Fh		EFh		F7Fh		FFh	

Legend: = Unimplemented data memory locations, read as '0'

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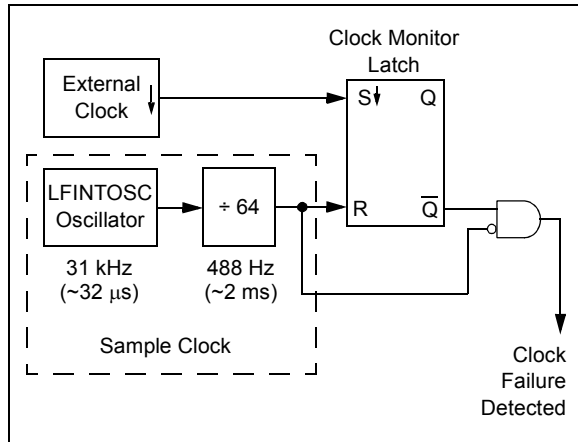
FIGURE 6-7: INTERNAL OSCILLATOR SWITCH TIMING



6.5 Fail-Safe Clock Monitor

The Fail-Safe Clock Monitor (FSCM) allows the device to continue operating should the external oscillator fail. The FSCM can detect oscillator failure any time after the Oscillator Start-up Timer (OST) has expired. The FSCM is enabled by setting the FCMEN bit in the Configuration Words. The FSCM is applicable to all external Oscillator modes (LP, XT, HS, EC, Timer1 Oscillator and RC).

FIGURE 6-9: FSCM BLOCK DIAGRAM



6.5.1 FAIL-SAFE DETECTION

The FSCM module detects a failed oscillator by comparing the external oscillator to the FSCM sample clock. The sample clock is generated by dividing the LFINTOSC by 64. See Figure 6-9. Inside the fail detector block is a latch. The external clock sets the latch on each falling edge of the external clock. The sample clock clears the latch on each rising edge of the sample clock. A failure is detected when an entire half-cycle of the sample clock elapses before the external clock goes low.

6.5.2 FAIL-SAFE OPERATION

When the external clock fails, the FSCM switches the device clock to an internal clock source and sets the bit flag OSFIF of the PIR2 register. Setting this flag will generate an interrupt if the OSFIE bit of the PIE2 register is also set. The device firmware can then take steps to mitigate the problems that may arise from a failed clock. The system clock will continue to be sourced from the internal clock source until the device firmware successfully restarts the external oscillator and switches back to external operation.

The internal clock source chosen by the FSCM is determined by the IRCF<3:0> bits of the OSCCON register. This allows the internal oscillator to be configured before a failure occurs.

6.5.3 FAIL-SAFE CONDITION CLEARING

The Fail-Safe condition is cleared after a Reset, executing a `SLEEP` instruction or changing the SCS bits of the OSCCON register. When the SCS bits are changed, the OST is restarted. While the OST is running, the device continues to operate from the INTOSC selected in OSCCON. When the OST times out, the Fail-Safe condition is cleared after successfully switching to the external clock source. The OSFIF bit should be cleared prior to switching to the external clock source. If the Fail-Safe condition still exists, the OSFIF flag will again become set by hardware.

6.5.4 RESET OR WAKE-UP FROM SLEEP

The FSCM is designed to detect an oscillator failure after the Oscillator Start-up Timer (OST) has expired. The OST is used after waking up from Sleep and after any type of Reset. The OST is not used with the EC or RC Clock modes so that the FSCM will be active as soon as the Reset or wake-up has completed. When the FSCM is enabled, the Two-Speed Start-up is also enabled. Therefore, the device will always be executing code while the OST is operating.

Note: Due to the wide range of oscillator start-up times, the Fail-Safe circuit is not active during oscillator start-up (i.e., after exiting Reset or Sleep). After an appropriate amount of time, the user should check the Status bits in the OSCSTAT register to verify the oscillator start-up and that the system clock switchover has successfully completed.

PIC16(L)F1788/9

8.6 Register Definitions: Interrupt Control

REGISTER 8-1: INTCON: INTERRUPT CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R-0/0
GIE	PEIE	TMR0IE	INTE	IOCFE	TMR0IF	INTF	IOCF ⁽¹⁾
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

- bit 7 **GIE:** Global Interrupt Enable bit
1 = Enables all active interrupts
0 = Disables all interrupts
- bit 6 **PEIE:** Peripheral Interrupt Enable bit
1 = Enables all active peripheral interrupts
0 = Disables all peripheral interrupts
- bit 5 **TMR0IE:** Timer0 Overflow Interrupt Enable bit
1 = Enables the Timer0 interrupt
0 = Disables the Timer0 interrupt
- bit 4 **INTE:** INT External Interrupt Enable bit
1 = Enables the INT external interrupt
0 = Disables the INT external interrupt
- bit 3 **IOCFE:** Interrupt-on-Change Enable bit
1 = Enables the interrupt-on-change
0 = Disables the interrupt-on-change
- bit 2 **TMR0IF:** Timer0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed
0 = TMR0 register did not overflow
- bit 1 **INTF:** INT External Interrupt Flag bit
1 = The INT external interrupt occurred
0 = The INT external interrupt did not occur
- bit 0 **IOCF:** Interrupt-on-Change Interrupt Flag bit⁽¹⁾
1 = When at least one of the interrupt-on-change pins changed state
0 = None of the interrupt-on-change pins have changed state

Note 1: The IOCF Flag bit is read-only and cleared when all the Interrupt-on-change flags in the IOCBF register have been cleared by software.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the Global Enable bit, GIE, of the INTCON register. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

9.0 POWER-DOWN MODE (SLEEP)

The Power-down mode is entered by executing a `SLEEP` instruction.

Upon entering Sleep mode, the following conditions exist:

1. WDT will be cleared but keeps running, if enabled for operation during Sleep.
2. \overline{PD} bit of the STATUS register is cleared.
3. \overline{TO} bit of the STATUS register is set.
4. CPU clock is disabled.
5. 31 kHz LFINTOSC is unaffected and peripherals that operate from it may continue operation in Sleep.
6. Timer1 and peripherals that operate from Timer1 continue operation in Sleep when the Timer1 clock source selected is:
 - LFINTOSC
 - T1CKI
 - Timer1 oscillator
7. ADC is unaffected, if the dedicated FRC oscillator is selected.
8. I/O ports maintain the status they had before `SLEEP` was executed (driving high, low or high-impedance).
9. Resets other than WDT are not affected by Sleep mode.

Refer to individual chapters for more details on peripheral operation during Sleep.

To minimize current consumption, the following conditions should be considered:

- I/O pins should not be floating
- External circuitry sinking current from I/O pins
- Internal circuitry sourcing current from I/O pins
- Current draw from pins with internal weak pull-ups
- Modules using 31 kHz LFINTOSC
- Modules using Timer1 oscillator

I/O pins that are high-impedance inputs should be pulled to V_{DD} or V_{SS} externally to avoid switching currents caused by floating inputs.

Examples of internal circuitry that might be sourcing current include modules such as the DAC and FVR modules. See **Section 19.0 “8-Bit Digital-to-Analog Converter (DAC) Module”** and **Section 15.0 “Fixed Voltage Reference (FVR)”** for more information on these modules.

9.1 Wake-up from Sleep

The device can wake-up from Sleep through one of the following events:

1. External Reset input on \overline{MCLR} pin, if enabled
2. BOR Reset, if enabled
3. POR Reset
4. Watchdog Timer, if enabled
5. Any external interrupt
6. Interrupts by peripherals capable of running during Sleep (see individual peripheral for more information)

The first three events will cause a device Reset. The last three events are considered a continuation of program execution. To determine whether a device Reset or wake-up event occurred, refer to **Section 5.12 “Determining the Cause of a Reset”**.

When the `SLEEP` instruction is being executed, the next instruction ($PC + 1$) is prefetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be enabled. Wake-up will occur regardless of the state of the GIE bit. If the GIE bit is disabled, the device continues execution at the instruction after the `SLEEP` instruction. If the GIE bit is enabled, the device executes the instruction after the `SLEEP` instruction, the device will then call the Interrupt Service Routine. In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

The WDT is cleared when the device wakes up from Sleep, regardless of the source of wake-up.

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9.3 Register Definitions: Voltage Regulator Control

REGISTER 9-1: VREGCON: VOLTAGE REGULATOR CONTROL REGISTER⁽¹⁾

U-0	U-0	U-0	U-0	U-0	U-0	R/W-0/0	R/W-1/1
—	—	—	—	—	—	VREGPM	Reserved
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set '0' = Bit is cleared

bit 7-2 **Unimplemented:** Read as '0'
bit 1 **VREGPM:** Voltage Regulator Power Mode Selection bit
 1 = Low-Power Sleep mode enabled in Sleep⁽²⁾
 Draws lowest current in Sleep, slower wake-up
 0 = Normal-Power mode enabled in Sleep⁽²⁾
 Draws higher current in Sleep, faster wake-up
bit 0 **Reserved:** Read as '1'. Maintain this bit set.

Note 1: "F" devices only.
2: See Section 31.0 "Electrical Specifications".

TABLE 9-1: SUMMARY OF REGISTERS ASSOCIATED WITH POWER-DOWN MODE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
INTCON	GIE	PEIE	TMR0IE	INTE	IOCFE	TMR0IF	INTF	RAIF	97
IOCBF	IOCBF7	IOCBF6	IOCBF5	IOCBF4	IOCBF3	IOCBF2	IOCBF1	IOCBF0	164
IOCBN	IOCBN7	IOCBN6	IOCBN5	IOCBN4	IOCBN3	IOCBN2	IOCBN1	IOCBN0	163
IOCBP	IOCBP7	IOCBP6	IOCBP5	IOCBP4	IOCBP3	IOCBP2	IOCBP1	IOCBP0	163
PIE1	TMR1GIE	ADIE	RCIE	TXIE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	98
PIE2	OSFIE	C2IE	C1IE	EEIE	BCL1IE	C4IE	C3IE	CCP2IE	99
PIE3	—	—	—	CCP3IE	—	—	—	—	100
PIE4	PSMC4TIE	PSMC3TIE	PSMC2TIE	PSMC1TIE	PSMC4SIE	PSMC3SIE	PSMC2SIE	PSMC1SIE	101
PIR1	TMR1GIF	ADIF	RCIF	TXIF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	98
PIR2	OSFIF	C2IF	C1IF	EEIF	BCL1IF	C4IF	C3IF	CCP2IF	103
PIR3	—	—	—	CCP3IF	—	—	—	—	104
PIR4	PSMC4TIF	PSMC3TIF	PSMC2TIF	PSMC1TIF	PSMC4SIF	PSMC3SIF	PSMC2SIF	PSMC1SIF	105
STATUS	—	—	—	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	31
VREGCON	—	—	—	—	—	—	VREGPM	Reserved	110
WDTCON	—	—	WDTPS<4:0>					SWDTEN	114

Legend: — = unimplemented location, read as '0'. Shaded cells are not used in Power-Down mode.

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TABLE 11-3: SUMMARY OF REGISTERS ASSOCIATED WITH WATCHDOG TIMER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Register on Page
OSCCON	SPLLEN	IRCF<3:0>				—	SCS<1:0>		86
STATUS	—	—	—	\overline{TO}	\overline{PD}	Z	DC	C	31
WDTCON	—	—	WDTPS<4:0>					SWDTEN	114

Legend: x = unknown, u = unchanged, — = unimplemented locations read as '0'. Shaded cells are not used by Watchdog Timer.

TABLE 11-4: SUMMARY OF CONFIGURATION WORD WITH WATCHDOG TIMER

Name	Bits	Bit -/7	Bit -/6	Bit 13/5	Bit 12/4	Bit 11/3	Bit 10/2	Bit 9/1	Bit 8/0	Register on Page
CONFIG1	13:8	—	—	FCMEN	IESO	CLKOUTEN	BOREN<1:0>		CPD	58
	7:0	CP	MCLRE	PWRTE	WDTE<1:0>		FOSC<2:0>			

Legend: — = unimplemented location, read as '0'. Shaded cells are not used by Watchdog Timer.

EXAMPLE 12-3: FLASH PROGRAM MEMORY READ

```
* This code block will read 1 word of program
* memory at the memory address:
  PROG_ADDR_HI : PROG_ADDR_LO
* data will be returned in the variables;
* PROG_DATA_HI, PROG_DATA_LO

  BANKSEL  EEADRL          ; Select Bank for EEPROM registers
  MOVLW    PROG_ADDR_LO    ;
  MOVWF    EEADRL          ; Store LSB of address
  MOVLW    PROG_ADDR_HI    ;
  MOVWL    EEADRH          ; Store MSB of address

  BCF      EECON1,CFGSR    ; Do not select Configuration Space
  BSF      EECON1,EEPGD    ; Select Program Memory
  BCF      INTCON,GIE      ; Disable interrupts
  BSF      EECON1,RD       ; Initiate read
  NOP                      ; Executed (Figure 12-1)
  NOP                      ; Ignored (Figure 12-1)
  BSF      INTCON,GIE      ; Restore interrupts

  MOVF     EEDATL,W        ; Get LSB of word
  MOVWF    PROG_DATA_LO    ; Store in user location
  MOVF     EEDATH,W        ; Get MSB of word
  MOVWF    PROG_DATA_HI    ; Store in user location
```

REGISTER 13-16: ODCONB: PORTB OPEN-DRAIN CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
ODB7	ODB6	ODB5	ODB4	ODB3	ODB2	ODB1	ODB0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-0 **ODB<7:0>**: PORTB Open-Drain Enable bits
 For RB<7:0> pins, respectively
 1 = Port pin operates as open-drain drive (sink current only)
 0 = Port pin operates as standard push-pull drive (source and sink current)

REGISTER 13-17: SLRCONB: PORTB SLEW RATE CONTROL REGISTER

R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1	R/W-1/1
SLRB7	SLRB6	SLRB5	SLRB4	SLRB3	SLRB2	SLRB1	SLRB0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-0 **SLRB<7:0>**: PORTB Slew Rate Enable bits
 For RB<7:0> pins, respectively
 1 = Port pin slew rate is limited
 0 = Port pin slews at maximum rate

REGISTER 13-18: INLVLB: PORTB INPUT LEVEL CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
INLVLB7	INLVLB6	INLVLB5	INLVLB4	INLVLB3	INLVLB2	INLVLB1	INLVLB0
bit 7							bit 0

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 u = Bit is unchanged x = Bit is unknown -n/n = Value at POR and BOR/Value at all other Resets
 '1' = Bit is set '0' = Bit is cleared

bit 7-0 **INLVLB<7:0>**: PORTB Input Level Select bits
 For RB<7:0> pins, respectively
 1 = ST input used for PORT reads and interrupt-on-change
 0 = TTL input used for PORT reads and interrupt-on-change

14.0 INTERRUPT-ON-CHANGE

All pins on the selected ports can be configured to operate as Interrupt-On-Change (IOC) pins. An interrupt can be generated by detecting a signal that has either a rising edge or a falling edge. Any individual pin, or combination of pins, can be configured to generate an interrupt. The interrupt-on-change module has the following features:

- Interrupt-on-Change enable (Master Switch)
- Individual pin configuration
- Rising and falling edge detection
- Individual pin interrupt flags

Figure 14-1 is a block diagram of the IOC module.

14.1 Enabling the Module

To allow individual pins to generate an interrupt, the IOCIE bit of the INTCON register must be set. If the IOCIE bit is disabled, the edge detection on the pin will still occur, but an interrupt will not be generated.

14.2 Individual Pin Configuration

For each pin, a rising edge detector and a falling edge detector are present. To enable a pin to detect a rising edge, the associated bit of the IOCxP register is set. To enable a pin to detect a falling edge, the associated bit of the IOCxN register is set.

A pin can be configured to detect rising and falling edges simultaneously by setting the associated bits in both of the IOCxP and IOCxN registers.

14.3 Interrupt Flags

The bits located in the IOCxF registers are status flags that correspond to the Interrupt-on-change pins of each port. If an expected edge is detected on an appropriately enabled pin, then the status flag for that pin will be set, and an interrupt will be generated if the IOCIE bit is set. The IOCIF bit of the INTCON register reflects the status of all IOCxF bits.

14.4 Clearing Interrupt Flags

The individual status flags, (IOCxF register bits), can be cleared by resetting them to zero. If another edge is detected during this clearing operation, the associated status flag will be set at the end of the sequence, regardless of the value actually being written.

In order to ensure that no detected edge is lost while clearing flags, only AND operations masking out known changed bits should be performed. The following sequence is an example of what should be performed.

EXAMPLE 14-1: CLEARING INTERRUPT FLAGS (PORTA EXAMPLE)

```
MOVLW    0xff
XORWF    IOCAF, W
ANDWF    IOCAF, F
```

14.5 Operation in Sleep

The interrupt-on-change interrupt sequence will wake the device from Sleep mode, if the IOCIE bit is set.

If an edge is detected while in Sleep mode, the affected IOCxF register will be updated prior to the first instruction executed out of Sleep.

17.0 ANALOG-TO-DIGITAL CONVERTER (ADC) MODULE

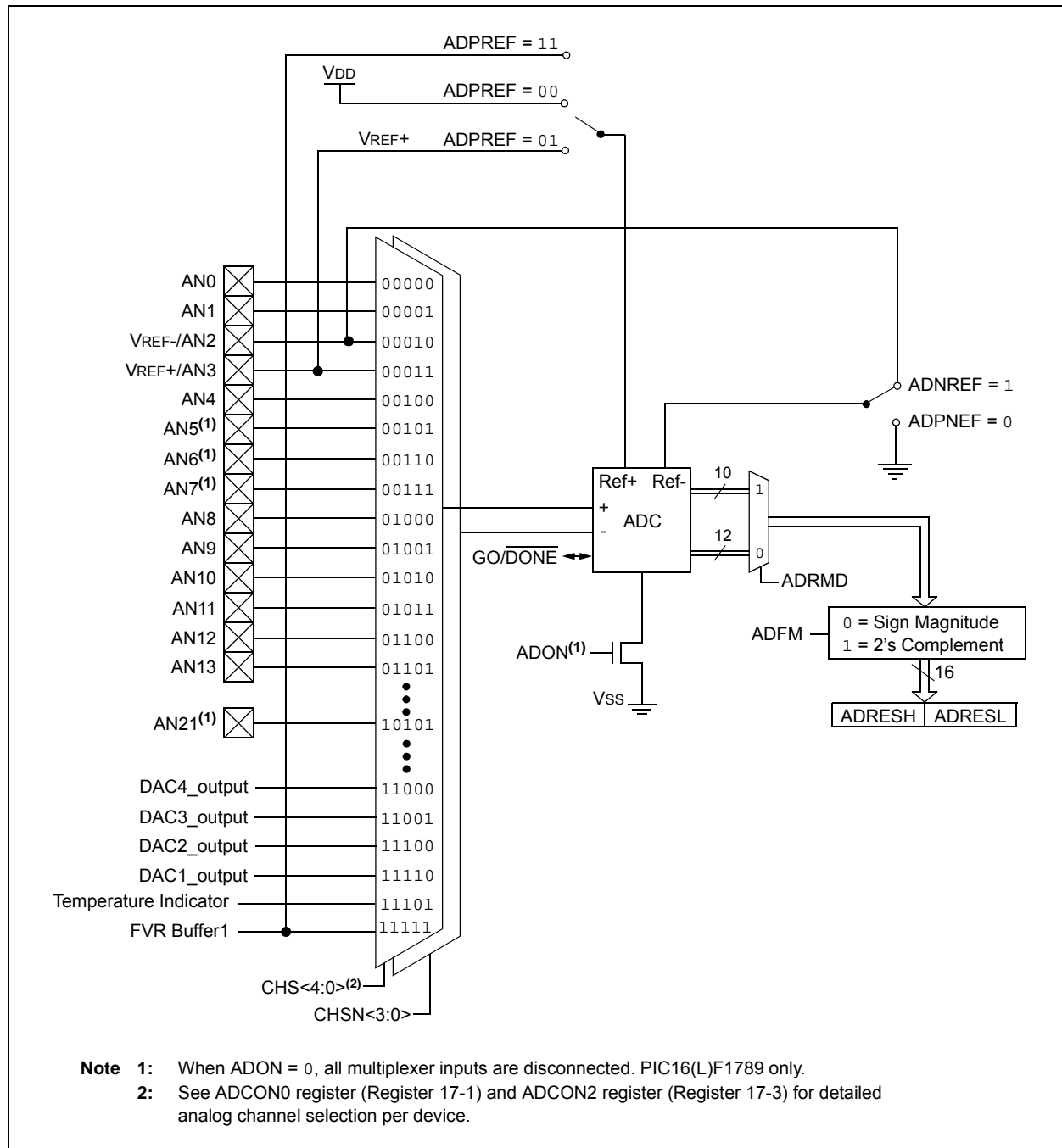
The Analog-to-Digital Converter (ADC) allows conversion of a single-ended and differential analog input signals to a 12-bit binary representation of that signal. This device uses analog inputs, which are multiplexed into a single sample and hold circuit. The output of the sample and hold is connected to the input of the converter. The converter generates a 12-bit binary result via successive approximation and stores

the conversion result into the ADC result registers (ADRESH:ADRESL register pair). Figure 17-1 shows the block diagram of the ADC.

The ADC voltage reference is software selectable to be either internally generated or externally supplied.

The ADC can generate an interrupt upon completion of a conversion. This interrupt can be used to wake-up the device from Sleep.

FIGURE 17-1: ADC BLOCK DIAGRAM



21.3 Comparator Hysteresis

A selectable amount of separation voltage can be added to the input pins of each comparator to provide a hysteresis function to the overall operation. Hysteresis is enabled by setting the CxHYS bit of the CMxCON0 register.

See **Section 30.0 “Electrical Specifications”** for more information.

21.4 Timer1 Gate Operation

The output resulting from a comparator operation can be used as a source for gate control of Timer1. See **Section 23.6 “Timer1 Gate”** for more information. This feature is useful for timing the duration or interval of an analog event.

It is recommended that the comparator output be synchronized to Timer1. This ensures that Timer1 does not increment while a change in the comparator is occurring.

21.4.1 COMPARATOR OUTPUT SYNCHRONIZATION

The output from a comparator can be synchronized with Timer1 by setting the CxSYNC bit of the CMxCON0 register.

Once enabled, the comparator output is latched on the falling edge of the Timer1 source clock. If a prescaler is used with Timer1, the comparator output is latched after the prescaling function. To prevent a race condition, the comparator output is latched on the falling edge of the Timer1 clock source and Timer1 increments on the rising edge of its clock source. See the Comparator Block Diagram (Figure 21-2) and the Timer1 Block Diagram (Figure 23-1) for more information.

21.5 Comparator Interrupt

An interrupt can be generated upon a change in the output value of the comparator for each comparator, a rising edge detector and a falling edge detector are present.

When either edge detector is triggered and its associated enable bit is set (CxINTP and/or CxINTN bits of the CMxCON1 register), the Corresponding Interrupt Flag bit (CxIF bit of the PIR2 register) will be set.

To enable the interrupt, you must set the following bits:

- CxON, CxPOL and CxSP bits of the CMxCON0 register
- CxIE bit of the PIE2 register
- CxINTP bit of the CMxCON1 register (for a rising edge detection)
- CxINTN bit of the CMxCON1 register (for a falling edge detection)
- PEIE and GIE bits of the INTCON register

The associated interrupt flag bit, CxIF bit of the PIR2 register, must be cleared in software. If another edge is detected while this flag is being cleared, the flag will still be set at the end of the sequence.

Note: Although a comparator is disabled, an interrupt can be generated by changing the output polarity with the CxPOL bit of the CMxCON0 register, or by switching the comparator on or off with the CxON bit of the CMxCON0 register.

21.6 Comparator Positive Input Selection

Configuring the CxPCH<2:0> bits of the CMxCON1 register directs an internal voltage reference or an analog pin to the non-inverting input of the comparator:

- CxIN+ analog pin
- DAC output
- FVR (Fixed Voltage Reference)
- Vss (Ground)

See **Section 15.0 “Fixed Voltage Reference (FVR)”** for more information on the Fixed Voltage Reference module.

See **Section 19.0 “8-Bit Digital-to-Analog Converter (DAC) Module”** for more information on the DAC input signal.

Any time the comparator is disabled (CxON = 0), all comparator inputs are disabled.

26.1.1 PERIOD EVENT

The period event determines the frequency of the active pulse. Period event sources include any combination of the following:

- PSMCxTMR counter match
- PSMC input pin
- sync_C1OUT
- sync_C2OUT
- sync_C3OUT
- sync_C4OUT

Period event sources are selected with the PSMC Period Source (PSMCxPRS) register (Register 26-15).

Section 26.2.1.2 “16-bit Period Register” contains details on configuring the PSMCxTMR counter match for synchronous period events.

All period events cause the PSMCxTMR counter to reset on the counting clock edge immediately following the period event. The PSMCxTMR counter resumes counting from zero on the counting clock edge after the period event Reset.

During a period, the rising event and falling event are each permitted to occur only once. Subsequent rising or falling events that may occur within the period are suppressed, thereby preventing output chatter from spurious inputs.

26.1.2 RISING EDGE EVENT

The rising edge event determines the start of the active drive period. The rising edge event is also referred to as the phase because two synchronized PSMC peripherals may have different rising edge events relative to the period start, thereby creating a phase relationship between the two PSMC peripheral outputs.

Depending on the PSMC mode, one or more of the PSMC outputs will change in immediate response to the rising edge event. Rising edge event sources include any combination of the following:

- Synchronous:
 - PSMCxTMR time base counter match
- Asynchronous:
 - PSMC input pin
 - sync_C1OUT
 - sync_C2OUT
 - sync_C3OUT
 - sync_C4OUT

Rising edge event sources are selected with the PSMC Phase Source (PSMCxPHS) register (Register 26-13).

For configuring the PSMCxTMR time base counter match for synchronous rising edge events, see **Section 26.2.1.3 “16-bit Phase Register”**.

The first rising edge event in a cycle period is the only one permitted to cause action. All subsequent rising edge events in the same period are suppressed to

prevent the PSMC output from chattering in the presence of spurious event inputs. A rising edge event is also suppressed when it occurs after a falling edge event in the same period.

The rising edge event also triggers the start of two other timers when needed: falling edge blanking and dead-band period. For more detail refer to **Section 26.2.8 “Input Blanking”** and **Section 26.4 “Dead-Band Control”**.

When the rising edge event is delayed from the period start, the amount of delay subtracts from the total amount of time available for the drive duty cycle. For example, if the rising edge event is delayed by 10% of the period time, the maximum duty cycle for that period is 90%. A 100% duty cycle is still possible in this example, but duty cycles from 90% to 100% are not possible.

26.1.3 FALLING EDGE EVENT

The falling edge event determines the end of the active drive period. The falling edge event is also referred to as the duty cycle because varying the falling edge event, while keeping the rising edge event and period events fixed, varies the active drive duty cycle.

Depending on the PSMC mode, one or more of the PSMC outputs will change in immediate response to the falling edge event. Falling edge event sources include any combination of the following:

- Synchronous:
 - PSMCxTMR time base counter match
- Asynchronous:
 - PSMC input pin
 - sync_C1OUT
 - sync_C2OUT
 - sync_C3OUT
 - sync_C4OUT

Falling edge event sources are selected with PSMC Duty Cycle Source (PSMCxDCS) register (Register 26-14).

For configuring the PSMCxTMR time base counter match for synchronous falling edge events, see **Section 26.2.1.4 “16-bit Duty Cycle Register”**.

The first falling edge event in a cycle period is the only one permitted to cause action. All subsequent falling edge events in the same period are suppressed to prevent the PSMC output from chattering in the presence of spurious event inputs.

A falling edge event suppresses any subsequent rising edges that may occur in the same period. In other words, if an asynchronous falling event input should come late and occur early in the period, following that for which it was intended, the rising edge in that period will be suppressed. This will have a similar effect as pulse skipping.

The falling edge event also triggers the start of two other timers: rising edge blanking and dead-band period. For more detail refer to **Section 26.2.8 “Input Blanking”** and **Section 26.4 “Dead-Band Control”**.

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REGISTER 26-6: PSMC4SYNC: PSMC3 SYNCHRONIZATION CONTROL REGISTER

R/W-0/0	R/W-0/0	R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
P4POFST	P4PRPOL	P4DCPOL	—	—	P4SYNC<2:0>		
bit 7							bit 0

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

u = Bit is unchanged

x = Bit is unknown

-n/n = Value at POR and BOR/Value at all other Resets

'1' = Bit is set

'0' = Bit is cleared

bit 7 **P4POFST:** PSMC4 Phase Offset Control bit

1 = sync_out source is phase event and latch set source is synchronous period event

0 = sync_out source is period event and latch set source is phase event

bit 6 **P4PRPOL:** PSMC4 Period Polarity Event Control bit

1 = Selected asynchronous period event inputs are inverted

0 = Selected asynchronous period event inputs are not inverted

bit 5 **P4DCPOL:** PSMC4 Duty-cycle Event Polarity Control bit

1 = Selected asynchronous duty-cycle event inputs are inverted

0 = Selected asynchronous duty-cycle event inputs are not inverted

bit 4-3 **Unimplemented:** Read as '0'

bit 2-0 **P4SYNC<2:0>:** PSMC4 Period Synchronization Mode bits

1xx = Reserved - Do not use

100 = PSMC4 is synchronized with the PSMC4 module (sync_in comes from PSMC4 sync_out)

011 = PSMC4 is synchronized with the PSMC3 module (sync_in comes from PSMC3 sync_out)

010 = PSMC4 is synchronized with the PSMC2 module (sync_in comes from PSMC3 sync_out)

001 = PSMC4 is synchronized with the PSMC1 module (sync_in comes from PSMC3 sync_out)

000 = PSMC4 is synchronized with period event

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27.5.3.3 7-bit Transmission with Address Hold Enabled

Setting the AHEN bit of the SSPCON3 register enables additional clock stretching and interrupt generation after the 8th falling edge of a received matching address. Once a matching address has been clocked in, CKP is cleared and the SSP1IF interrupt is set.

Figure 27-18 displays a standard waveform of a 7-bit Address Slave Transmission with AHEN enabled.

1. Bus starts Idle.
2. Master sends Start condition; the S bit of SSPSTAT is set; SSP1IF is set if interrupt on Start detect is enabled.
3. Master sends matching address with $\overline{R/W}$ bit set. After the 8th falling edge of the SCL line the CKP bit is cleared and SSP1IF interrupt is generated.
4. Slave software clears SSP1IF.
5. Slave software reads ACKTIM bit of SSPCON3 register, and $\overline{R/W}$ and $\overline{D/A}$ of the SSPSTAT register to determine the source of the interrupt.
6. Slave reads the address value from the SSPBUF register clearing the BF bit.
7. Slave software decides from this information if it wishes to ACK or not ACK and sets the ACKDT bit of the SSPCON2 register accordingly.
8. Slave sets the CKP bit releasing SCL.
9. Master clocks in the \overline{ACK} value from the slave.
10. Slave hardware automatically clears the CKP bit and sets SSP1IF after the \overline{ACK} if the $\overline{R/W}$ bit is set.
11. Slave software clears SSP1IF.
12. Slave loads value to transmit to the master into SSPBUF setting the BF bit.

Note: SSPBUF cannot be loaded until after the \overline{ACK} .

13. Slave sets the CKP bit releasing the clock.
14. Master clocks out the data from the slave and sends an \overline{ACK} value on the 9th SCL pulse.
15. Slave hardware copies the \overline{ACK} value into the ACKSTAT bit of the SSPCON2 register.
16. Steps 10-15 are repeated for each byte transmitted to the master from the slave.
17. If the master sends a not \overline{ACK} the slave releases the bus allowing the master to send a Stop and end the communication.

Note: Master must send a not \overline{ACK} on the last byte to ensure that the slave releases the SCL line to receive a Stop.

28.6 EUSART Operation During Sleep

The EUSART will remain active during Sleep only in the Synchronous Slave mode. All other modes require the system clock and therefore cannot generate the necessary signals to run the Transmit or Receive Shift registers during Sleep.

Synchronous Slave mode uses an externally generated clock to run the Transmit and Receive Shift registers.

28.6.1 SYNCHRONOUS RECEIVE DURING SLEEP

To receive during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for Synchronous Slave Reception (see **Section 28.5.2.4 “Synchronous Slave Reception Set-up:”**).
- If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
- The RCIF interrupt flag must be cleared by reading RCREG to unload any pending characters in the receive buffer.

Upon entering Sleep mode, the device will be ready to accept data and clocks on the RX/DT and TX/CK pins, respectively. When the data word has been completely clocked in by the external device, the RCIF interrupt flag bit of the PIR1 register will be set. Thereby, waking the processor from Sleep.

Upon waking from Sleep, the instruction following the **SLEEP** instruction will be executed. If the Global Interrupt Enable (GIE) bit of the INTCON register is also set, then the Interrupt Service Routine at address 004h will be called.

28.6.2 SYNCHRONOUS TRANSMIT DURING SLEEP

To transmit during Sleep, all the following conditions must be met before entering Sleep mode:

- RCSTA and TXSTA Control registers must be configured for synchronous slave transmission (see **Section 28.5.2.2 “Synchronous Slave Transmission Set-up:”**).
- The TXIF interrupt flag must be cleared by writing the output data to the TXREG, thereby filling the TSR and transmit buffer.
- If interrupts are desired, set the TXIE bit of the PIE1 register and the PEIE bit of the INTCON register.
- Interrupt enable bits TXIE of the PIE1 register and PEIE of the INTCON register must set.

Upon entering Sleep mode, the device will be ready to accept clocks on TX/CK pin and transmit data on the RX/DT pin. When the data word in the TSR has been completely clocked out by the external device, the pending byte in the TXREG will transfer to the TSR and the TXIF flag will be set. Thereby, waking the processor from Sleep. At this point, the TXREG is available to accept another character for transmission, which will clear the TXIF flag.

Upon waking from Sleep, the instruction following the **SLEEP** instruction will be executed. If the Global Interrupt Enable (GIE) bit is also set then the Interrupt Service Routine at address 0004h will be called.

28.6.3 ALTERNATE PIN LOCATIONS

This module incorporates I/O pins that can be moved to other locations with the use of the alternate pin function register, APFCON. To determine which pins can be moved and what their default locations are upon a Reset, see **Section 13.1 “Alternate Pin Function”** for more information.

RETURN Return from Subroutine

Syntax: [label] RETURN

Operands: None

Operation: TOS → PC

Status Affected: None

Description: Return from subroutine. The stack is POPed and the top of the stack (TOS) is loaded into the program counter. This is a 2-cycle instruction.

RRF Rotate Right f through Carry

Syntax: [label] RRF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the right through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is placed back in register 'f'.



RLF Rotate Left f through Carry

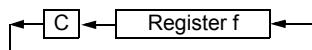
Syntax: [label] RLF f,d

Operands: $0 \leq f \leq 127$
 $d \in [0,1]$

Operation: See description below

Status Affected: C

Description: The contents of register 'f' are rotated one bit to the left through the Carry flag. If 'd' is '0', the result is placed in the W register. If 'd' is '1', the result is stored back in register 'f'.



Words: 1

Cycles: 1

Example: RLF REG1,0

Before Instruction

REG1 = 1110

0110

C = 0

After Instruction

REG1 = 1110

0110

W = 1100

1100

C = 1

SLEEP Enter Sleep mode

Syntax: [label] SLEEP

Operands: None

Operation: 00h → WDT,
0 → WDT prescaler,
1 → $\overline{\text{TO}}$,
0 → $\overline{\text{PD}}$

Status Affected: $\overline{\text{TO}}$, $\overline{\text{PD}}$

Description: The power-down Status bit, $\overline{\text{PD}}$ is cleared. Time-out Status bit, $\overline{\text{TO}}$ is set. Watchdog Timer and its prescaler are cleared. The processor is put into Sleep mode with the oscillator stopped.

SUBLW Subtract W from literal

Syntax: [label] SUBLW k

Operands: $0 \leq k \leq 255$

Operation: $k - (W) \rightarrow (W)$

Status Affected: C, DC, Z

Description: The W register is subtracted (2's complement method) from the 8-bit literal 'k'. The result is placed in the W register.

C = 0	$W > k$
C = 1	$W \leq k$
DC = 0	$W<3:0> > k<3:0>$
DC = 1	$W<3:0> \leq k<3:0>$

32.0 DC AND AC CHARACTERISTICS GRAPHS AND CHARTS

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified VDD range). This is for **information only** and devices are ensured to operate properly only within the specified range.

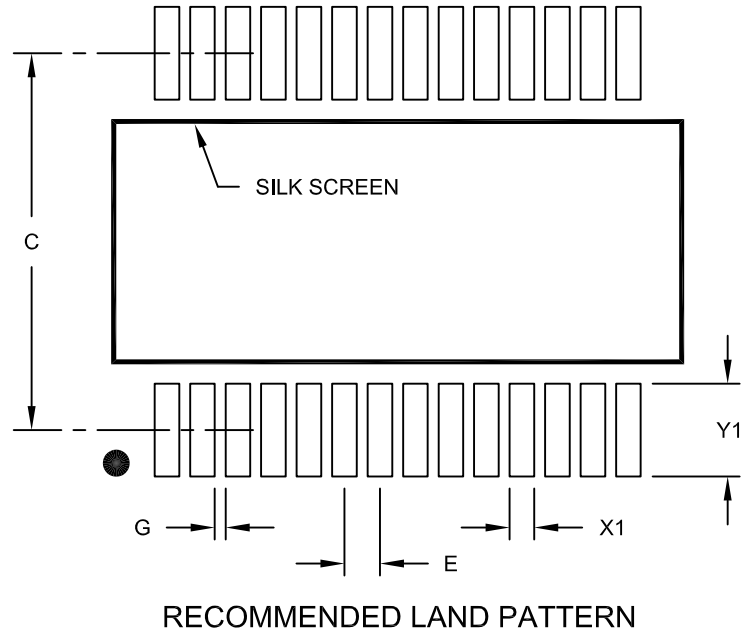
Unless otherwise noted, all graphs apply to both the F and LF devices.

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore, outside the warranted range.

“Typical” represents the mean of the distribution at 25°C. “Maximum”, “Max.”, “Minimum” or “Min.” represents (mean + 3σ) or (mean - 3σ) respectively, where σ is a standard deviation, over each temperature range.

28-Lead Plastic Shrink Small Outline (SS) - 5.30 mm Body [SSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C		7.20	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.75
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2073A