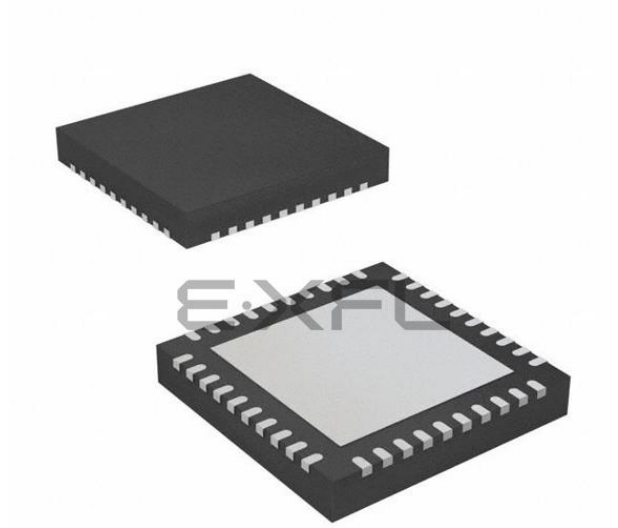

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	8-Bit
Speed	32MHz
Connectivity	I²C, LINbus, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, POR, PSMC, PWM, WDT
Number of I/O	35
Program Memory Size	28KB (16K x 14)
Program Memory Type	FLASH
EEPROM Size	256 x 8
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 3.6V
Data Converters	A/D 14x12b; D/A 1x8b, 3x5b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	40-UFQFN Exposed Pad
Supplier Device Package	40-UQFN (5x5)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic16lf1789t-i-mv

2.0 ENHANCED MID-RANGE CPU

This family of devices contain an enhanced mid-range 8-bit CPU core. The CPU has 49 instructions. Interrupt capability includes automatic context saving. The hardware stack is 16 levels deep and has Overflow and Underflow Reset capability. Direct, Indirect, and Relative addressing modes are available. Two File Select Registers (FSRs) provide the ability to read program and data memory.

- Automatic Interrupt Context Saving
- 16-level Stack with Overflow and Underflow
- File Select Registers
- Instruction Set

FIGURE 2-1: CORE BLOCK DIAGRAM

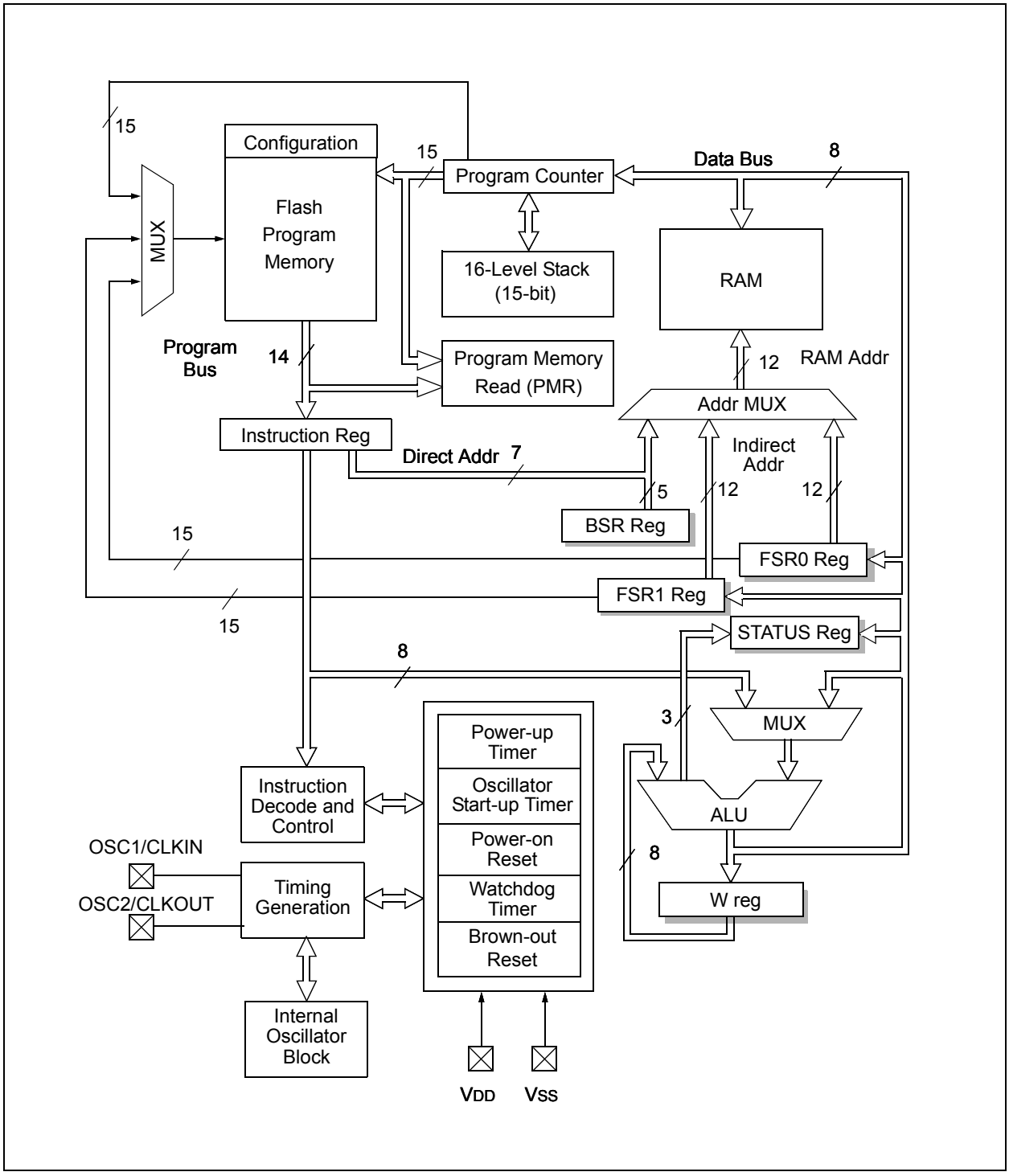


TABLE 3-6: PIC16(L)F1788/9 MEMORY MAP (BANK 10 DETAILS)

	BANK 10
50Ch	Unimplemented Read as '0'
510h	
511h	OPA1CON
512h	—
513h	OPA2CON
514h	—
515h	OPA3CON(1)
516h	—
517h	—
518h	—
519h	
51Ah	CLKRCON
51Bh	Unimplemented Read as '0'
51Fh	

Legend: = Unimplemented data memory locations, read as '0

Note 1: PIC16(L)F1789 only.

TABLE 3-7: PIC16(L)F1788/9 MEMORY MAP (BANK 11 DETAILS)

	BANK 11
58Ch	Unimplemented Read as '0'
590h	
591h	DAC2CON0
592h	DAC2CON1
593h	DAC3CON0
594h	DAC3CON1
595h	DAC4CON0
596h	DAC4CON1
597h	Unimplemented Read as '0'
59Fh	

Legend: = Unimplemented data memory locations, read as '0'.

TABLE 3-8: PIC16(L)F1788/9 MEMORY MAP (BANK 31 DETAILS)

	BANK 31
F8Ch	Unimplemented Read as '0'
FE3h	
FE4h	STATUS_SHAD
FE5h	WREG_SHAD
FE6h	BSR_SHAD
FE7h	PCLATH_SHAD
FE8h	FSR0L_SHAD
FE9h	FSR0H_SHAD
FEAh	FSR1L_SHAD
FEBh	FSR1H_SHAD
FECh	—
FEDh	STKPTR
FEEh	TOSL
FEFh	TOSH

Legend: = Unimplemented data memory locations, read as '0'.

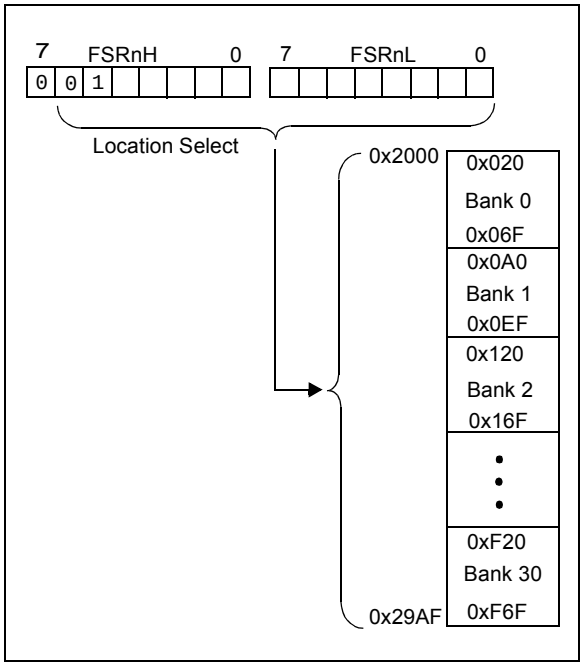
3.6.2 LINEAR DATA MEMORY

The linear data memory is the region from FSR address 0x2000 to FSR address 0x29AF. This region is a virtual region that points back to the 80-byte blocks of GPR memory in all the banks.

Unimplemented memory reads as 0x00. Use of the linear data memory region allows buffers to be larger than 80 bytes because incrementing the FSR beyond one bank will go directly to the GPR memory of the next bank.

The 16 bytes of common memory are not included in the linear data memory region.

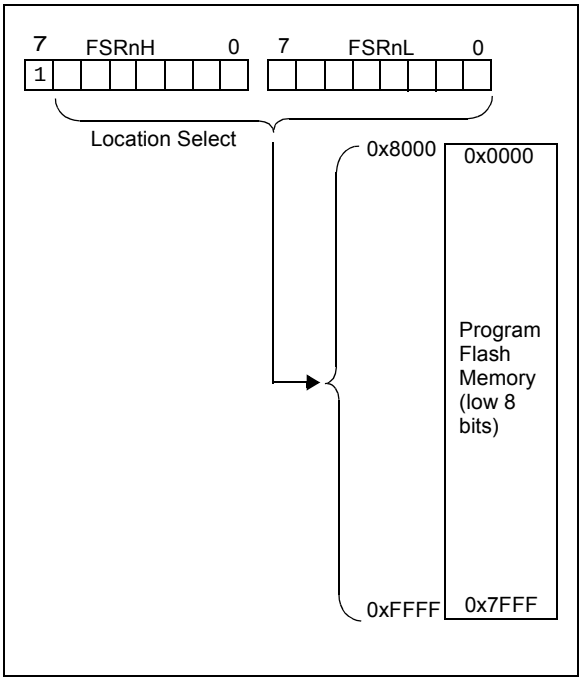
FIGURE 3-10: LINEAR DATA MEMORY MAP



3.6.3 PROGRAM FLASH MEMORY

To make constant data access easier, the entire program Flash memory is mapped to the upper half of the FSR address space. When the MSB of FSRnH is set, the lower 15 bits are the address in program memory which will be accessed through INDF. Only the lower eight bits of each memory location is accessible via INDF. Writing to the program Flash memory cannot be accomplished via the FSR/INDF interface. All instructions that access program Flash memory via the FSR/INDF interface will require one additional instruction cycle to complete.

FIGURE 3-11: PROGRAM FLASH MEMORY MAP

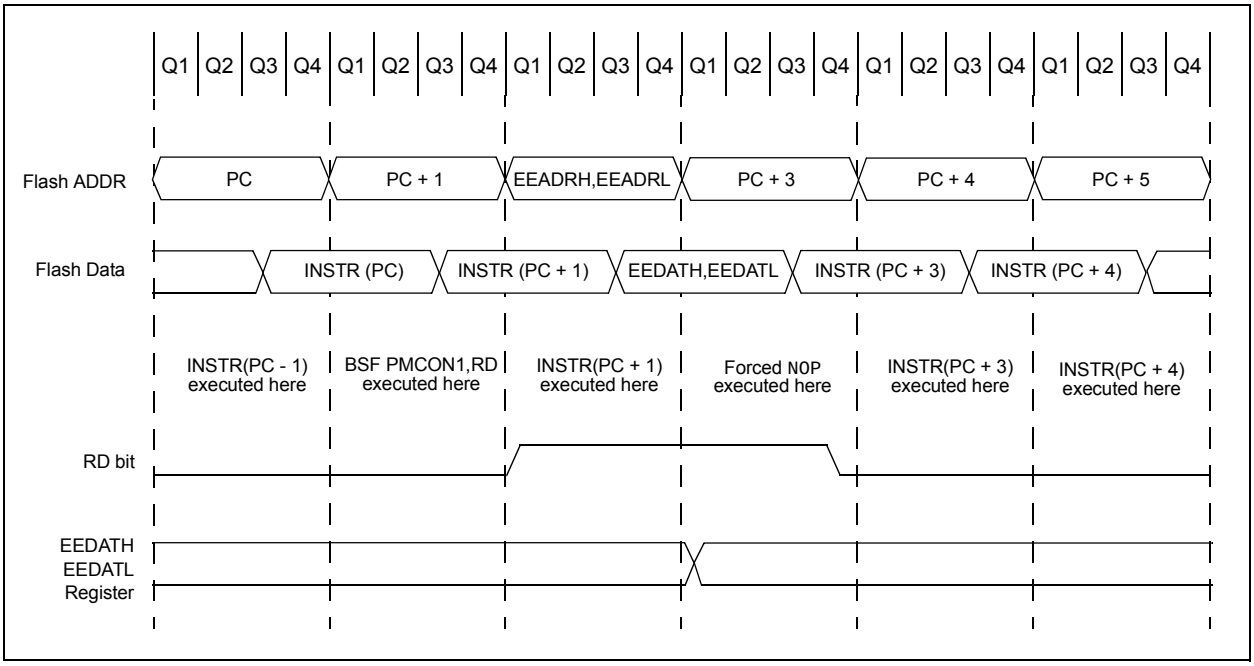


EXAMPLE 12-2: DATA EEPROM WRITE

```
        BANKSEL  EEADRL          ;
        MOVLW    DATA_EE_ADDR    ;
        MOVWF    EEADRL          ;Data Memory Address to write
        MOVLW    DATA_EE_DATA    ;
        MOVWF    EEDATL          ;Data Memory Value to write
        BCF      EECON1, CFGS    ;Deselect Configuration space
        BCF      EECON1, EEPGD   ;Point to DATA memory
        BSF      EECON1, WREN    ;Enable writes

        BCF      INTCON, GIE     ;Disable INTs.
Required
Sequence
        MOVLW    55h             ;
        MOVWF    EECON2          ;Write 55h
        MOVLW    0AAh            ;
        MOVWF    EECON2          ;Write AAh
        BSF      EECON1, WR      ;Set WR bit to begin write
        BSF      INTCON, GIE     ;Enable Interrupts
        BCF      EECON1, WREN    ;Disable writes
        BTFSC    EECON1, WR      ;Wait for write to complete
        GOTO     $-2             ;Done
```

FIGURE 12-1: FLASH PROGRAM MEMORY READ CYCLE EXECUTION



13.0 I/O PORTS

Each port has three standard registers for its operation. These registers are:

- TRISx registers (data direction)
- PORTx registers (reads the levels on the pins of the device)
- LATx registers (output latch)

Some ports may have one or more of the following additional registers. These registers are:

- ANSELx (analog select)
- WPUx (weak pull-up)

In general, when a peripheral is enabled on a port pin, that pin cannot be used as a general purpose output. However, the pin can still be read.

TABLE 13-1: PORT AVAILABILITY PER DEVICE

Device	PORTA	PORTB	PORTC	PORTD	PORTE
PIC16(L)F1788	•	•	•		•
PIC16(L)F1789	•	•	•	•	•

The Data Latch (LATx registers) is useful for read-modify-write operations on the value that the I/O pins are driving.

A write operation to the LATx register has the same effect as a write to the corresponding PORTx register. A read of the LATx register reads of the values held in the I/O PORT latches, while a read of the PORTx register reads the actual I/O pin value.

Ports that support analog inputs have an associated ANSELx register. When an ANSEL bit is set, the digital input buffer associated with that bit is disabled. Disabling the input buffer prevents analog signal levels on the pin between a logic high and low from causing excessive current in the logic input circuitry. A simplified model of a generic I/O port, without the interfaces to other peripherals, is shown in Figure 13-1.

FIGURE 13-1: GENERIC I/O PORT OPERATION

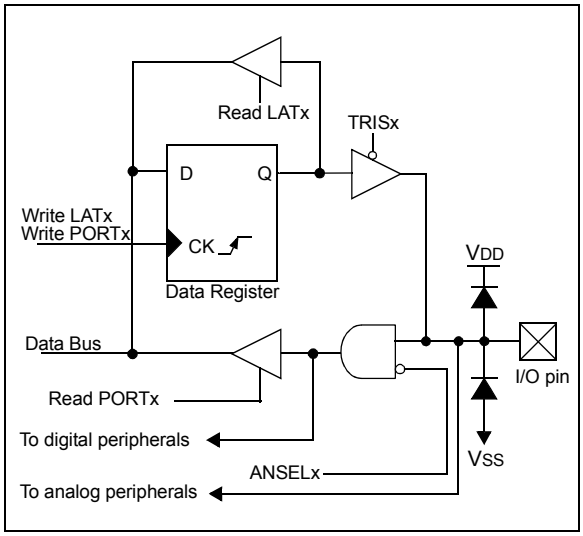
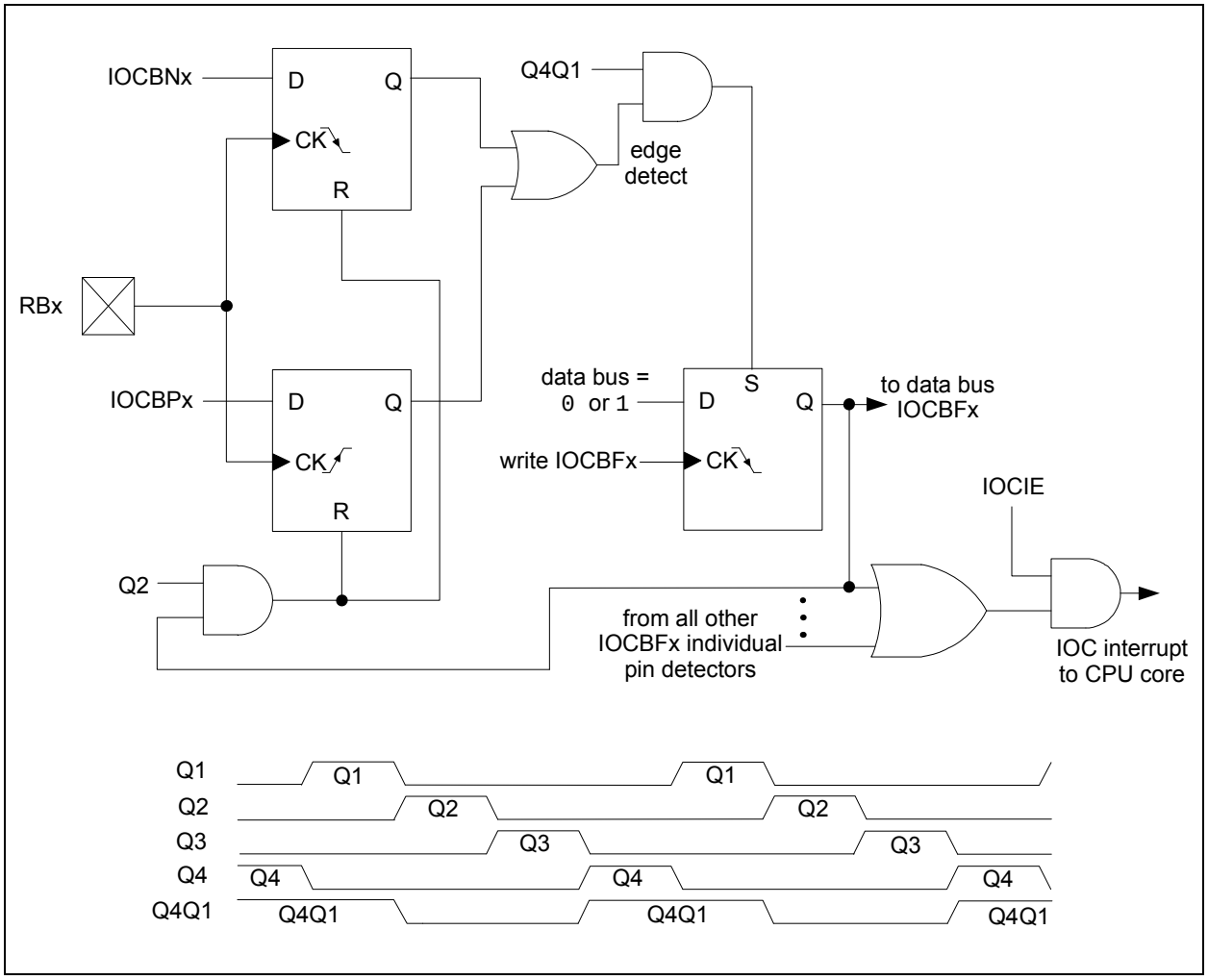


FIGURE 14-1: INTERRUPT-ON-CHANGE BLOCK DIAGRAM



REGISTER 17-2: ADCON1: ADC CONTROL REGISTER 1

R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0	R/W-0/0	R/W-0/0	R/W-0/0
ADFM	ADCS<2:0>			—	ADNREF	ADPREF<1:0>	
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as ‘0’
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
‘1’ = Bit is set	‘0’ = Bit is cleared	

bit 7 **ADFM:** ADC Result Format Select bit (see Figure 17-3)
1 = 2’s complement format.
0 = Sign-magnitude result format.

bit 6-4 **ADCS<2:0>:** ADC Conversion Clock Select bits
111 = FRC (clock supplied from a dedicated FRC oscillator)
110 = FOSC/64
101 = FOSC/16
100 = FOSC/4
011 = FRC (clock supplied from a dedicated FRC oscillator)
010 = FOSC/32
001 = FOSC/8
000 = FOSC/2

bit 3 **Unimplemented:** Read as ‘0’

bit 2 **ADNREF:** ADC Negative Voltage Reference Configuration bit
1 = VREF- is connected to external VREF- pin(1)
0 = VREF- is connected to VSS

bit 1-0 **ADPREF<1:0>:** ADC Positive Voltage Reference Configuration bits
11 = VREF+ is connected internally to FVR Buffer 1
10 = Reserved
01 = VREF+ is connected to VREF+ pin
00 = VREF+ is connected to VDD

Note 1: When selecting the FVR or VREF+ pin as the source of the positive reference, be aware that a minimum voltage specification exists. See **Section 31.0 “Electrical Specifications”** for details.

19.0 8-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) MODULE

The Digital-to-Analog Converter supplies a variable voltage reference, ratiometric with the input source, with 256 selectable output levels.

The input of the DAC can be connected to:

- External VREF pins
- VDD supply voltage
- FVR (Fixed Voltage Reference)

The output of the DAC can be configured to supply a reference voltage to the following:

- Comparator positive input
- Op amp positive input
- ADC input channel
- DAC1OUT1 pin
- DAC1OUT2 pin

The Digital-to-Analog Converter (DAC) is enabled by setting the DAC1EN bit of the DAC1CON0 register.

19.1 Output Voltage Selection

The DAC has 256 voltage level ranges. The 256 levels are set with the DAC1R<7:0> bits of the DAC1CON1 register.

The DAC output voltage is determined by Equation 19-1:

EQUATION 19-1: DAC OUTPUT VOLTAGE

IF DACxEN = 1

$$V_{OUT} = \left((V_{SOURCE+} - V_{SOURCE-}) \times \frac{DACxR[7:0]}{2^8} \right) + V_{SOURCE-}$$

VSOURCE+ = VDD, VREF, or FVR BUFFER 2

VSOURCE- = VSS

19.2 Ratiometric Output Level

The DAC output value is derived using a resistor ladder with each end of the ladder tied to a positive and negative voltage reference input source. If the voltage of either input source fluctuates, a similar fluctuation will result in the DAC output value.

The value of the individual resistors within the ladder can be found in **Section 31.0 "Electrical Specifications"**.

19.3 DAC Voltage Reference Output

The DAC voltage can be output to the DAC1OUT1 and DAC1OUT2 pins by setting the respective DAC1OE1 and DAC1OE2 pins of the DAC1CON0 register. Selecting the DAC reference voltage for output on either DAC1OUTx pin automatically overrides the digital output buffer and digital input threshold detector functions of that pin. Reading the DAC1OUTx pin when it has been configured for DAC reference voltage output will always return a '0'.

Due to the limited current drive capability, a buffer must be used on the DAC voltage reference output for external connections to either DAC1OUTx pin. Figure 19-2 shows an example buffering technique.

21.7 Comparator Negative Input Selection

The CxNCH<2:0> bits of the CMxCON0 register direct an analog input pin or analog ground to the inverting input of the comparator:

- CxIN- pin
- Analog Ground

Some inverting input selections share a pin with the operational amplifier output function. Enabling both functions at the same time will direct the operational amplifier output to the comparator inverting input.

Note:	To use CxINy+ and CxINy- pins as analog input, the appropriate bits must be set in the ANSEL register and the corresponding TRIS bits must also be set to disable the output drivers.

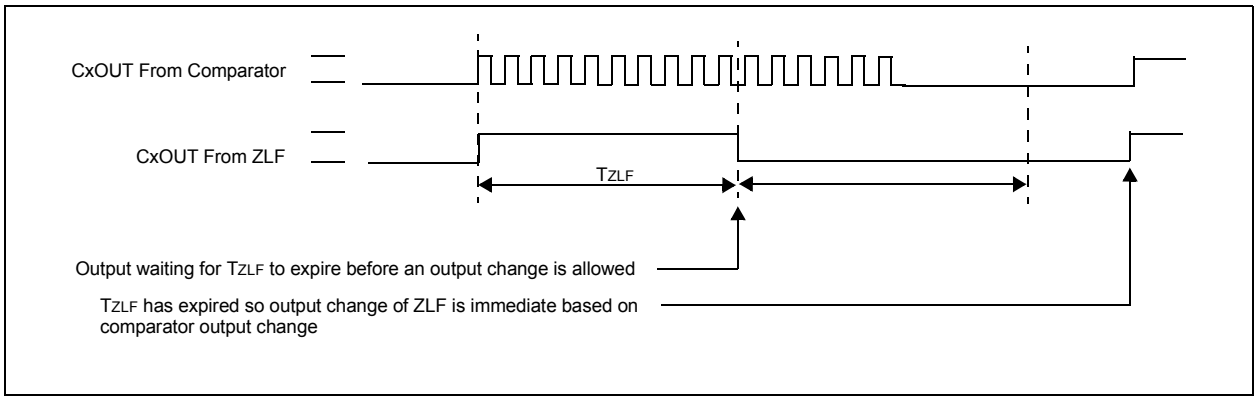
21.8 Comparator Response Time

The comparator output is indeterminate for a period of time after the change of an input source or the selection of a new reference voltage. This period is referred to as the response time. The response time of the comparator differs from the settling time of the voltage reference. Therefore, both of these times must be considered when determining the total response time to a comparator input change. See the Comparator and Voltage Reference Specifications in **Section 31.0 "Electrical Specifications"** for more details.

21.9 Zero Latency Filter

In high-speed operation, and under proper circuit conditions, it is possible for the comparator output to oscillate. This oscillation can have adverse effects on the hardware and software relying on this signal. Therefore, a digital filter has been added to the comparator output to suppress the comparator output oscillation. Once the comparator output changes, the output is prevented from reversing the change for a nominal time of 20 ns. This allows the comparator output to stabilize without affecting other dependent devices. Refer to Figure 21-3.

FIGURE 21-3: COMPARATOR ZERO LATENCY FILTER OPERATION



25.4 Register Definitions: CCP Control

REGISTER 25-1: CCPxCON: CCPx CONTROL REGISTER

U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0
—	—	DCxB<1:0>		CCPxM<3:0>			
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Reset
'1' = Bit is set	'0' = Bit is cleared	

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB<1:0>:** PWM Duty Cycle Least Significant bits

Capture mode:
Unused

Compare mode:
Unused

PWM mode:
These bits are the two LSbs of the PWM duty cycle. The eight MSbs are found in CCPRxL.

bit 3-0 **CCPxM<3:0>:** CCPx Mode Select bits

11xx = PWM mode

1011 = Compare mode: Auto-conversion Trigger (sets CCPxIF bit (CCP2), starts ADC conversion if ADC module is enabled)(1)
1010 = Compare mode: generate software interrupt only
1001 = Compare mode: clear output on compare match (set CCPxIF)
1000 = Compare mode: set output on compare match (set CCPxIF)

0111 = Capture mode: every 16th rising edge
0110 = Capture mode: every 4th rising edge
0101 = Capture mode: every rising edge
0100 = Capture mode: every falling edge

0011 = Reserved
0010 = Compare mode: toggle output on match
0001 = Reserved
0000 = Capture/Compare/PWM off (resets CCPx module)

26.2.7 ASYNCHRONOUS INPUTS

The PSMC module supports asynchronous inputs alone or in combination with the synchronous inputs. asynchronous inputs include:

- Analog
  - sync_C1OUT
  - sync_C2OUT
  - sync_C3OUT
  - sync_C4OUT
- Digital
  - PSMCxIN pin

26.2.7.1 Comparator Inputs

The outputs of any combination of the synchronized comparators may be used to trigger any of the three events as well as auto-shutdown.

The event triggers on the rising edge of the comparator output. Except for auto-shutdown, the event input is not level sensitive.

26.2.7.2 PSMCxIN Pin Input

The PSMCxIN pin may be used to trigger PSMC events. Data is passed through straight to the PSMC module without any synchronization to a system clock. This is so that input blanking may be applied to any external circuit using the module.

The event triggers on the rising edge of the PSMCxIN signal.

26.2.7.3 Asynchronous Polarity

Polarity control is available for the period and duty-cycle asynchronous event inputs. Polarity control is necessary when the same signal is used as the source for both events. Inverting the polarity of one event relative to the other enables starting the period on one edge of the signal and terminating the duty-cycle on the opposite edge. Polarity is controlled with the PxPRPOL and PxDCPOL bits of the PSMCxSYNC register. Inverting the asynchronous input with these controls inverts all enabled asynchronous inputs for the corresponding event.

26.2.8 INPUT BLANKING

Input blanking is a function whereby the inputs from any selected asynchronous input may be driven inactive for a short period of time. This is to prevent electrical transients from the turn-on/off of power components from generating a false event.

Blanking is initiated by either or both:

- Rising event
- Falling event

Blanked inputs are suppressed from causing all asynchronous events, including:

- Rising
- Falling
- Period
- Shutdown

Rising edge and falling edge blanking are controlled independently. The following features are available for blanking:

- Blanking enable
- Blanking time counters
- Blanking mode

The following Blanking modes are available:

- Blanking disabled
- Immediate blanking

The Falling Edge Blanking mode is set with the PxFEBM<1:0> bits of the PSMCx Blanking Control (PSMCxBLNK) register (Register 26-10).

The Rising Edge Blanking mode is set with the PxREBM<1:0> bits of the PSMCx Blanking Control (PSMCxBLNK) register (Register 26-10).

26.2.8.1 Blanking Disabled

With blanking disabled, the asynchronous inputs are passed to the PSMC module without any intervention.

26.2.8.2 Immediate Blanking

With Immediate blanking, a counter is used to determine the blanking period. The desired blanking time is measured in psmc_clk periods. A rising edge event will start incrementing the rising edge blanking counter. A falling edge event will start incrementing the falling edge blanking counter.

The rising edge blanking time is set with the PSMC Rising Edge Blanking Time (PSMCxBLKR) register (Register 26-30). The inputs to be blanked are selected with the PSMC Rising Edge Blanked Source (PSMCxREBS) register (Register 26-11). During rising edge blanking, the selected blanked sources are suppressed for falling edge as well as rising edge, auto-shutdown and period events.

The falling edge blanking time is set with the PSMC Falling Edge Blanking Time (PSMCxBLKF) register (Register 26-31). The inputs to be blanked are selected with the PSMC Falling Edge Blanked Source (PSMCxFEBS) register (Register 26-12). During falling edge blanking, the selected blanked sources are suppressed for rising edge, as well as falling edge, auto-shutdown, and period events.

The blanking counters are incremented on the rising edge of psmc_clk. Blanked sources are suppressed until the counter value equals the blanking time register causing the blanking to terminate.

As the rising and falling edge events are from asynchronous inputs, there may be some uncertainty in the actual blanking time implemented in each cycle. The maximum uncertainty is equal to one psmc_clk period.

26.3.3 PUSH-PULL PWM

The push-pull PWM is used to drive transistor bridge circuits. It uses at least two outputs and generates PWM signals that alternate between the two outputs in even and odd cycles.

Variations of the push-pull waveform include four outputs with two outputs being complementary or two sets of two identical outputs. Refer to Sections 26.3.4 through 26.3.6 for the other Push-Pull modes.

26.3.3.1 Mode Features

- No dead-band control available
- No steering control available
- Output is on the following two pins only:
  - PSMCxA
  - PSMCxB

Note: This is a subset of the 6-pin output of the push-pull PWM output, which is why pin functions are fixed in these positions, so they are compatible with that mode. See **Section 26.3.6 "Push-Pull PWM with Four Full-Bridge and Complementary Outputs"**

26.3.3.2 Waveform Generation

Odd numbered period rising edge event:

- PSMCxA is set active

Odd numbered period falling edge event:

- PSMCxA is set inactive

Even numbered period rising edge event:

- PSMCxB is set active

Even numbered period falling edge event:

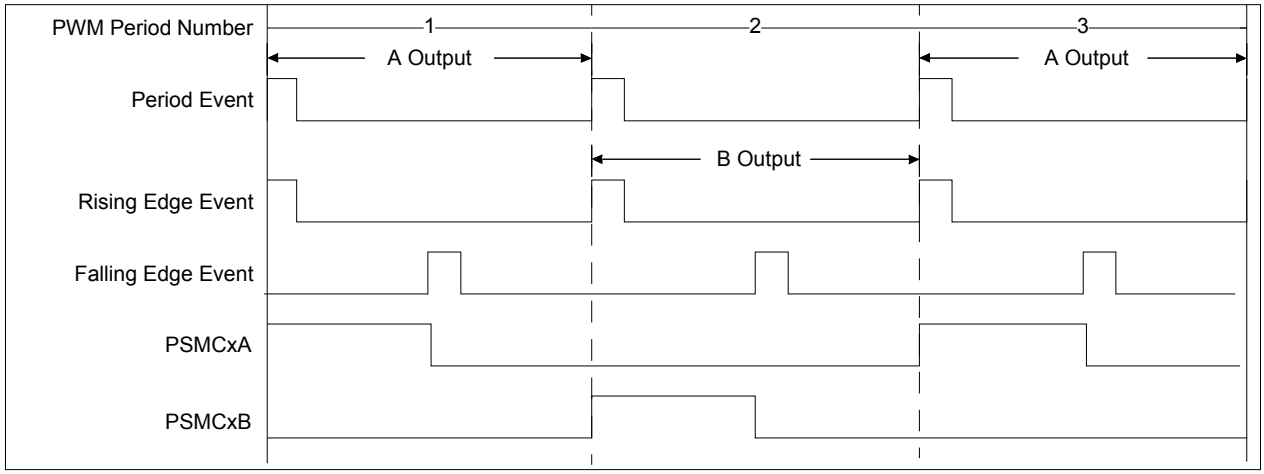
- PSMCxB is set inactive

Code for setting up the PSMC generate the complementary single-phase waveform shown in Figure 26-6, and given in Example 26-3.

EXAMPLE 26-3: PUSH-PULL SETUP

```
; Push-Pull PWM PSMC setup
; Fully synchronous operation
; Period = 10 us
; Duty cycle = 50% (25% each phase)
   BANKSEL  PSMC1CON
   MOVLW    0x02        ; set period
   MOVWF    PSMC1PRH
   MOVLW    0x7F
   MOVWF    PSMC1PRL
   MOVLW    0x01        ; set duty cycle
   MOVWF    PSMC1DCH
   MOVLW    0x3F
   MOVWF    PSMC1DCL
   CLRF     PSMC1PHH    ; no phase offset
   CLRF     PSMC1PHL
   MOVLW    0x01        ; PSMC clock=64 MHz
   MOVWF    PSMC1CLK
; output on A and B, normal polarity
   MOVLW    B'00000011'
   MOVWF    PSMC1OEN
   CLRF     PSMC1POL
; set time base as source for all events
   BSF      PSMC1PRS, P1PRST
   BSF      PSMC1PHS, P1PHST
   BSF      PSMC1DCS, P1DCST
; enable PSMC in Push-Pull Mode
; this also loads steering and time buffers
   MOVLW    B'11000010'
   MOVWF    PSMC1CON
   BANKSEL  TRISC
   BCF      TRISC, 0    ; enable pin drivers
   BCF      TRISC, 1
```

FIGURE 26-6: PUSH-PULL PWM WAVEFORM



REGISTER 26-11: PSMCxREBS: PSMC RISING EDGE BLANKED SOURCE REGISTER

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxREBSIN	—	—	PxREBSC4	PxREBSC3	PxREBSC2	PxREBSC1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxREBSIN:** PSMCx Rising Edge Event Blanked from PSMCxIN pin
1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = PSMCxIN pin is not blanked

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxREBSC4:** PSMCx Rising Edge Event Blanked from sync_C4OUT
1 = sync_C4OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C4OUT is not blanked

bit 3 **PxREBSC3:** PSMCx Rising Edge Event Blanked from sync_C3OUT
1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C3OUT is not blanked

bit 2 **PxREBSC2:** PSMCx Rising Edge Event Blanked from sync_C2OUT
1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C2OUT is not blanked

bit 1 **PxREBSC1:** PSMCx Rising Edge Event Blanked from sync_C1OUT
1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C1OUT is not blanked

bit 0 **Unimplemented:** Read as '0'

REGISTER 26-12: PSMCxFEBS: PSMC FALLING EDGE BLANKED SOURCE REGISTER

R/W-0/0	U-0	U-0	R/W-0/0	R/W-0/0	R/W-0/0	R/W-0/0	U-0
PxFEBSIN	—	—	PxFEBSC4	PxFEBSC3	PxFEBSC2	PxFEBSC1	—
bit 7							bit 0

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
u = Bit is unchanged	x = Bit is unknown	-n/n = Value at POR and BOR/Value at all other Resets
'1' = Bit is set	'0' = Bit is cleared	

bit 7 **PxFEBSIN:** PSMCx Falling Edge Event Blanked from PSMCxIN pin
1 = PSMCxIN pin cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = PSMCxIN pin is not blanked

bit 6-5 **Unimplemented:** Read as '0'

bit 4 **PxFEBSC4:** PSMCx Falling Edge Event Blanked from sync_C4OUT
1 = sync_C4OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C4OUT is not blanked

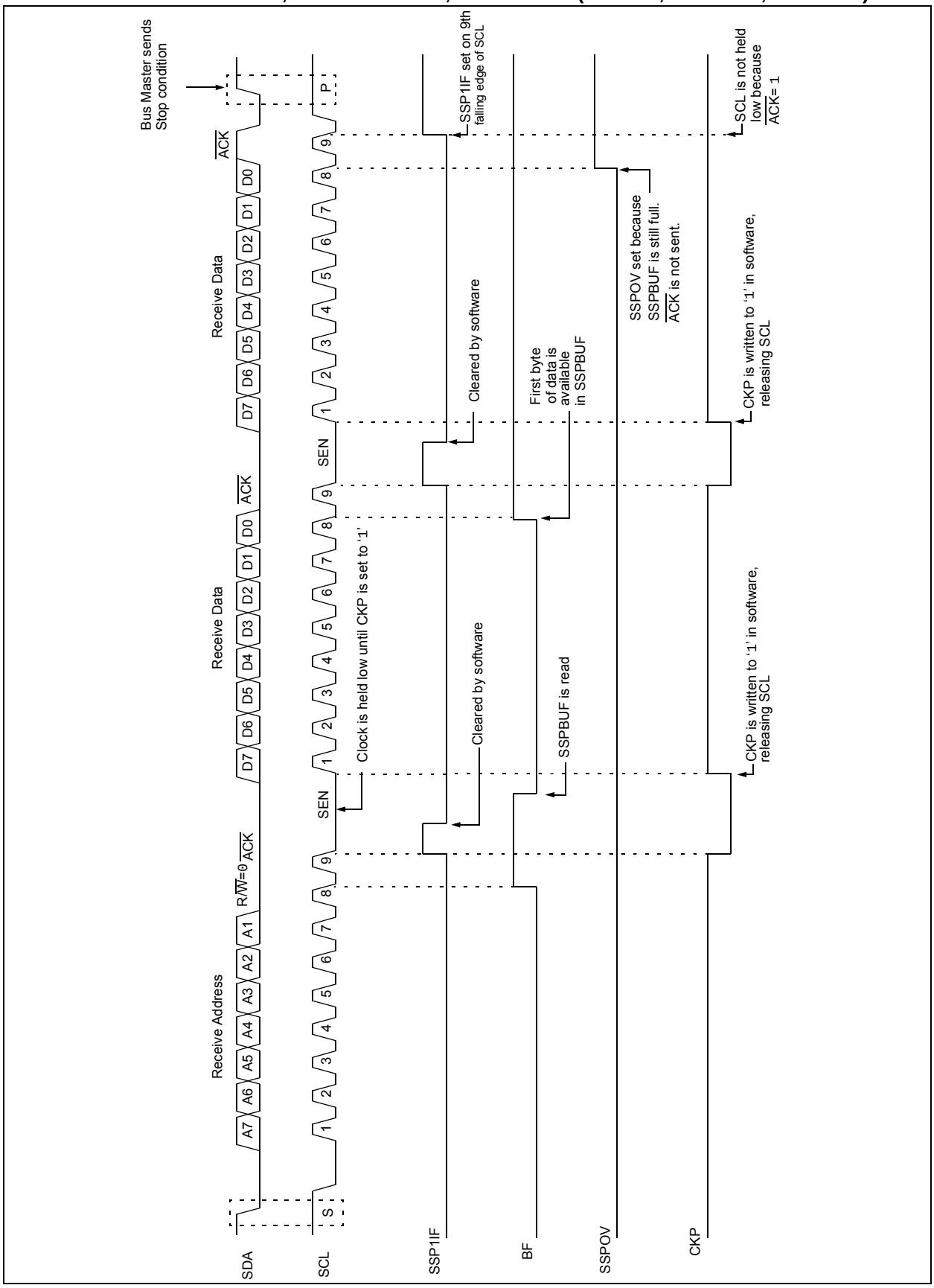
bit 3 **PxFEBSC3:** PSMCx Falling Edge Event Blanked from sync_C3OUT
1 = sync_C3OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C3OUT is not blanked

bit 2 **PxFEBSC2:** PSMCx Falling Edge Event Blanked from sync_C2OUT
1 = sync_C2OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C2OUT is not blanked

bit 1 **PxFEBSC1:** PSMCx Falling Edge Event Blanked from sync_C1OUT
1 = sync_C1OUT cannot cause a rising or falling event for the duration indicated by the PSMCxBLNK register
0 = sync_C1OUT is not blanked

bit 0 **Unimplemented:** Read as '0'

FIGURE 27-15: I²C SLAVE, 7-BIT ADDRESS, RECEPTION (SEN = 1, AHEN = 0, DHEN = 0)



27.5.8 GENERAL CALL ADDRESS SUPPORT

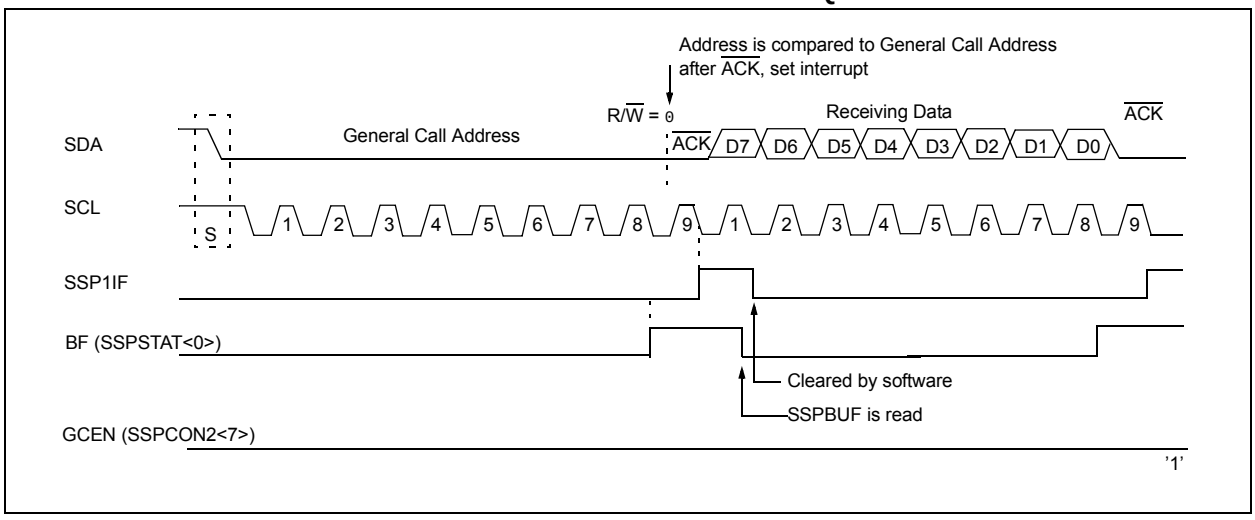
The addressing procedure for the I^2C bus is such that the first byte after the Start condition usually determines which device will be the slave addressed by the master device. The exception is the general call address which can address all devices. When this address is used, all devices should, in theory, respond with an acknowledge.

The general call address is a reserved address in the I^2C protocol, defined as address 0x00. When the GCEN bit of the SSPCON2 register is set, the slave module will automatically $\overline{ACK}$ the reception of this address regardless of the value stored in SSPADD. After the slave clocks in an address of all zeros with the R/$\overline{W}$ bit clear, an interrupt is generated and slave software can read SSPBUF and respond. Figure 27-23 shows a general call reception sequence.

In 10-bit Address mode, the UA bit will not be set on the reception of the general call address. The slave will prepare to receive the second byte as data, just as it would in 7-bit mode.

If the AHEN bit of the SSPCON3 register is set, just as with any other address reception, the slave hardware will stretch the clock after the 8th falling edge of SCL. The slave must then set its ACKDT value and release the clock with communication progressing as it would normally.

FIGURE 27-24: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE



27.5.9 SSP MASK REGISTER

An SSP Mask (SSPMSK) register (Register 27-5) is available in I^2C Slave mode as a mask for the value held in the SSPSR register during an address comparison operation. A zero ('0') bit in the SSPMSK register has the effect of making the corresponding bit of the received address a "don't care".

This register is reset to all '1's upon any Reset condition and, therefore, has no effect on standard SSP operation until written with a mask value.

The SSP Mask register is active during:

- 7-bit Address mode: address compare of A<7:1>.
- 10-bit Address mode: address compare of A<7:0> only. The SSP mask has no effect during the reception of the first (high) byte of the address.

28.5.1.5 Synchronous Master Reception

Data is received at the RX/DT pin. The RX/DT pin output driver is automatically disabled when the EUSART is configured for synchronous master receive operation.

In Synchronous mode, reception is enabled by setting either the Single Receive Enable bit (SREN of the RCSTA register) or the Continuous Receive Enable bit (CREN of the RCSTA register).

When SREN is set and CREN is clear, only as many clock cycles are generated as there are data bits in a single character. The SREN bit is automatically cleared at the completion of one character. When CREN is set, clocks are continuously generated until CREN is cleared. If CREN is cleared in the middle of a character the CK clock stops immediately and the partial character is discarded. If SREN and CREN are both set, then SREN is cleared at the completion of the first character and CREN takes precedence.

To initiate reception, set either SREN or CREN. Data is sampled at the RX/DT pin on the trailing edge of the TX/CK clock pin and is shifted into the Receive Shift Register (RSR). When a complete character is received into the RSR, the RCIF bit is set and the character is automatically transferred to the two character receive FIFO. The Least Significant eight bits of the top character in the receive FIFO are available in RCREG. The RCIF bit remains set as long as there are unread characters in the receive FIFO.

Note:	If the RX/DT function is on an analog pin, the corresponding ANSEL bit must be cleared for the receiver to function.

28.5.1.6 Slave Clock

Synchronous data transfers use a separate clock line, which is synchronous with the data. A device configured as a slave receives the clock on the TX/CK line. The TX/CK pin output driver is automatically disabled when the device is configured for synchronous slave transmit or receive operation. Serial data bits change on the leading edge to ensure they are valid at the trailing edge of each clock. One data bit is transferred for each clock cycle. Only as many clock cycles should be received as there are data bits.

Note:	If the device is configured as a slave and the TX/CK function is on an analog pin, the corresponding ANSEL bit must be cleared.

28.5.1.7 Receive Overrun Error

The receive FIFO buffer can hold two characters. An overrun error will be generated if a third character, in its entirety, is received before RCREG is read to access the FIFO. When this happens the OERR bit of the RCSTA register is set. Previous data in the FIFO will not be overwritten. The two characters in the FIFO buffer can be read, however, no additional characters will be received until the error is cleared. The OERR bit can only be cleared by clearing the overrun condition. If the overrun error occurred when the SREN bit is set and CREN is clear then the error is cleared by reading RCREG. If the overrun occurred when the CREN bit is set then the error condition is cleared by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

28.5.1.8 Receiving 9-bit Characters

The EUSART supports 9-bit character reception. When the RX9 bit of the RCSTA register is set, the EUSART will shift nine bits into the RSR for each character received. The RX9D bit of the RCSTA register is the ninth, and Most Significant, data bit of the top unread character in the receive FIFO. When reading 9-bit data from the receive FIFO buffer, the RX9D data bit must be read before reading the eight Least Significant bits from the RCREG.

28.5.1.9 Synchronous Master Reception Set-up:

1. Initialize the SPBRGH, SPBRGL register pair for the appropriate baud rate. Set or clear the BRGH and BRG16 bits, as required, to achieve the desired baud rate.
2. Clear the ANSEL bit for the RX pin (if applicable).
3. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
4. Ensure bits CREN and SREN are clear.
5. If interrupts are desired, set the RCIE bit of the PIE1 register and the GIE and PEIE bits of the INTCON register.
6. If 9-bit reception is desired, set bit RX9.
7. Start reception by setting the SREN bit or for continuous reception, set the CREN bit.
8. Interrupt flag bit RCIF will be set when reception of a character is complete. An interrupt will be generated if the enable bit RCIE was set.
9. Read the RCSTA register to get the ninth bit (if enabled) and determine if any error occurred during reception.
10. Read the 8-bit received data by reading the RCREG register.
11. If an overrun error occurs, clear the error by either clearing the CREN bit of the RCSTA register or by clearing the SPEN bit which resets the EUSART.

TABLE 31-8: PLL CLOCK TIMING SPECIFICATIONS

Standard Operating Conditions (unless otherwise stated)							
Param No.	**Sym.**	**Characteristic**	**Min.**	**Typ†**	**Max.**	**Units**	**Conditions**
F10	FOSC	Oscillator Frequency Range	4	—	8	MHz	
F11	FSYS	On-Chip VCO System Frequency	16	—	32	MHz	
F12	TRC	PLL Start-up Time (Lock Time)	—	—	2	ms	
F13*	ΔCLK	CLKOUT Stability (Jitter)	-0.25%	—	+0.25%	%	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 31-7: CLKOUT AND I/O TIMING

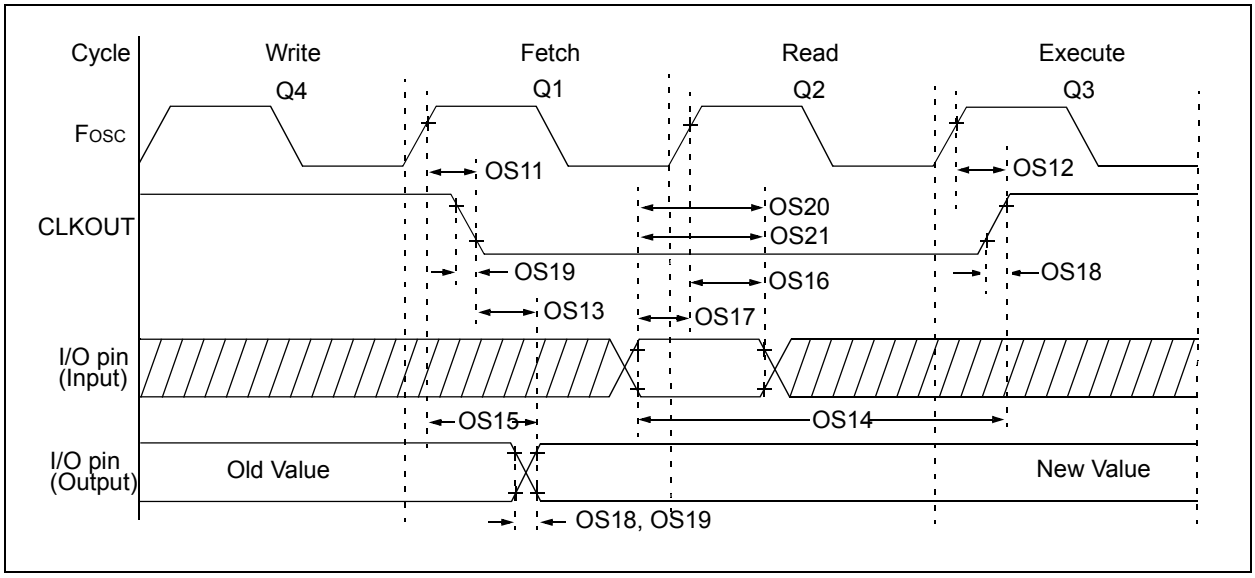


TABLE 31-17: 5-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: V_{DD} = 3V, Temperature = 25°C (unless otherwise stated).							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DAC01*	C_{LSB}5	Step Size	—	V_{DD}/32	—	V	
DAC02*	C_{ACC}5	Absolute Accuracy	—	—	± 1/2	LSb	
DAC03*	C_R5	Unit Resistor Value (R)	—	5K	—	Ω	
DAC04*	C_{ST}5	Settling Time(2)	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: See **Section 32.0 "DC and AC Characteristics Graphs and Charts"** for operating characterization.

2: Settling time measured while DACR<7:0> transitions from '00000' to '01111'.

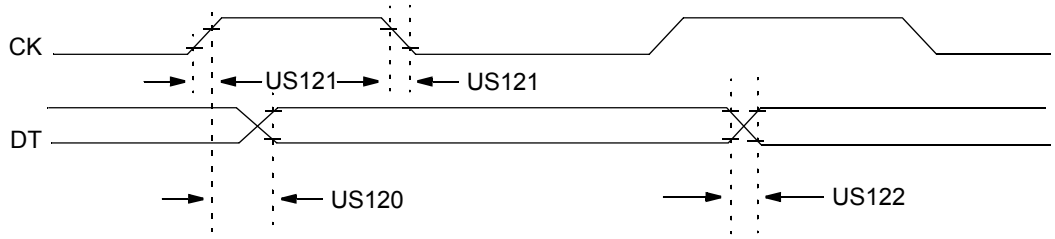
TABLE 31-18: 8-BIT DIGITAL-TO-ANALOG CONVERTER (DAC) SPECIFICATIONS

Operating Conditions: V_{DD} = 3V, Temperature = 25°C (unless otherwise stated).							
Param No.	**Sym.**	**Characteristics**	**Min.**	**Typ.**	**Max.**	**Units**	**Comments**
DAC05*	C_{LSB}8	Step Size	—	V_{DD}/256	—	V	
DAC06*	C_{ACC}8	Absolute Accuracy	—	—	± 1.5	LSb	
DAC07*	C_R8	Unit Resistor Value (R)	—	600	—	Ω	
DAC08*	C_{ST}8	Settling Time(1)	—	—	10	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while DACR<7:0> transitions from '0x00' to '0xFF'.

FIGURE 31-14: EUSART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING



Note: Refer to Figure 31-4 for load conditions.

TABLE 31-19: EUSART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Standard Operating Conditions (unless otherwise stated)							
Param. No.	**Symbol**	**Characteristic**		**Min.**	**Max.**	**Units**	**Conditions**
US120	$T_{CK}H2_{DT}V$	SYNC XMIT (Master and Slave) Clock high to data-out valid	3.0-5.5V	—	80	ns	
			1.8-5.5V	—	100	ns	
US121	T_{CKRF}	Clock out rise time and fall time (Master mode)	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	
US122	T_{DTRF}	Data-out rise time and fall time	3.0-5.5V	—	45	ns	
			1.8-5.5V	—	50	ns	

Note: Unless otherwise noted, V_{IN} = 5V, F_{OSC} = 300 kHz, C_{IN} = 0.1 µF, T_A = 25°C.

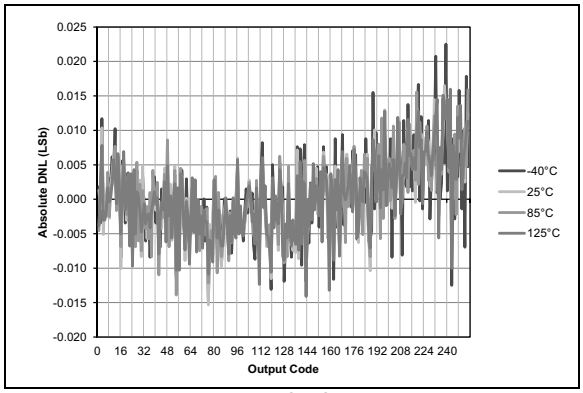


FIGURE 32-126: *Typical DAC DNL Error, V_{DD} = 3.0V, V_{REF} = External 3V.*

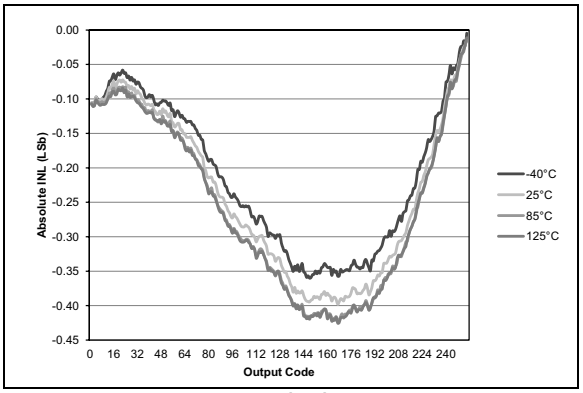


FIGURE 32-127: *Typical DAC INL Error, V_{DD} = 3.0V, V_{REF} = External 3V.*

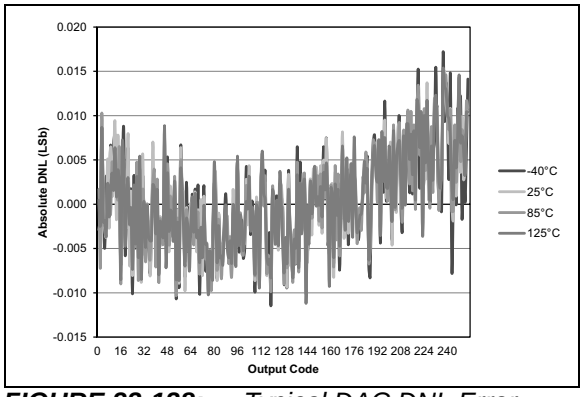


FIGURE 32-128: *Typical DAC DNL Error, V_{DD} = 5.0V, V_{REF} = External 5V, PIC16F1788/9 Only.*

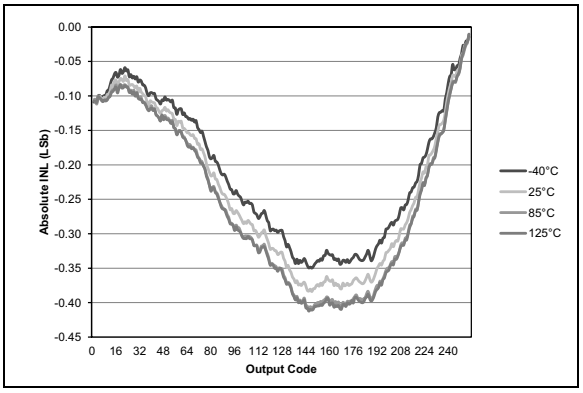


FIGURE 32-129: *Typical DAC INL Error, V_{DD} = 5.0V, V_{REF} = External 5V, PIC16F1788/9 Only.*

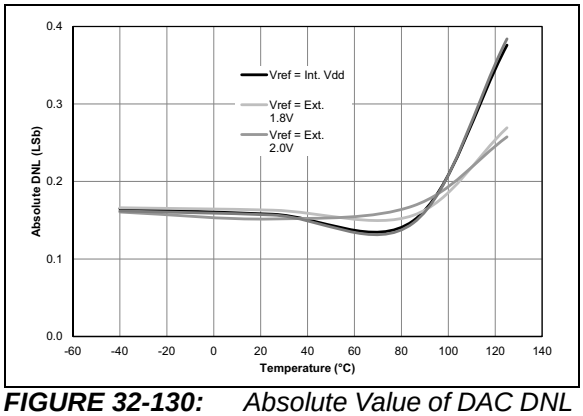


FIGURE 32-130: *Absolute Value of DAC DNL Error, V_{DD} = 3.0V, V_{REF} = V_{DD}.*

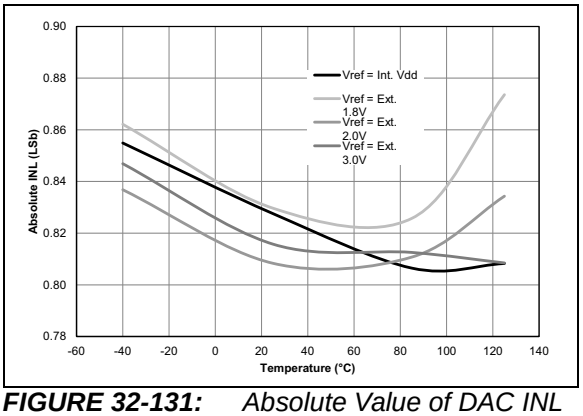
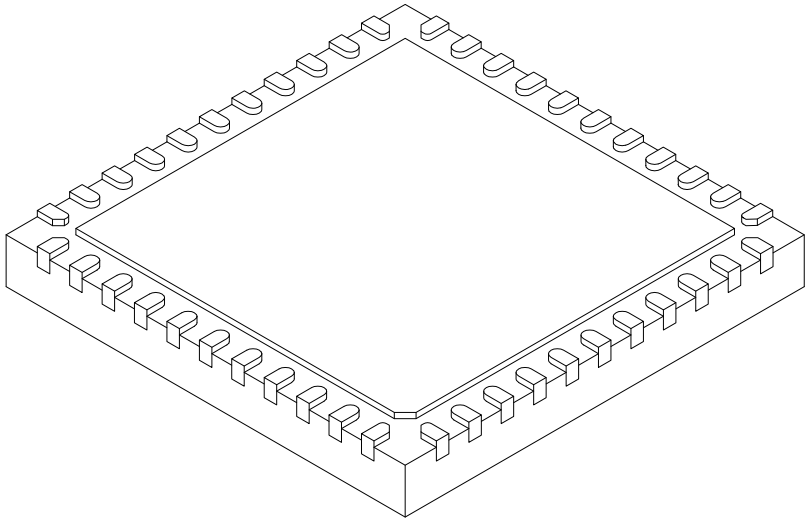


FIGURE 32-131: *Absolute Value of DAC INL Error, V_{DD} = 3.0V.*

44-Lead Plastic Quad Flat, No Lead Package (ML) - 8x8 mm Body [QFN]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		44	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Terminal Thickness	A3		0.20 REF	
Overall Width	E		8.00 BSC	
Exposed Pad Width	E2	6.25	6.45	6.60
Overall Length	D		8.00 BSC	
Exposed Pad Length	D2	6.25	6.45	6.60
Terminal Width	b	0.20	0.30	0.35
Terminal Length	L	0.30	0.40	0.50
Terminal-to-Exposed-Pad	K	0.20	-	-

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Package is saw singulated
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-103C Sheet 2 of 2