Infineon Technologies - MB96F6B6RBPMC-GSE2 Datasheet

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What is "Embedded - Microcontrollers"?

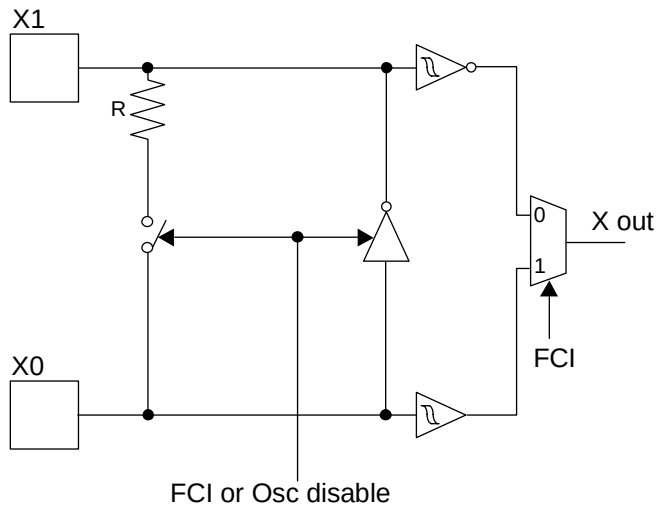
"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

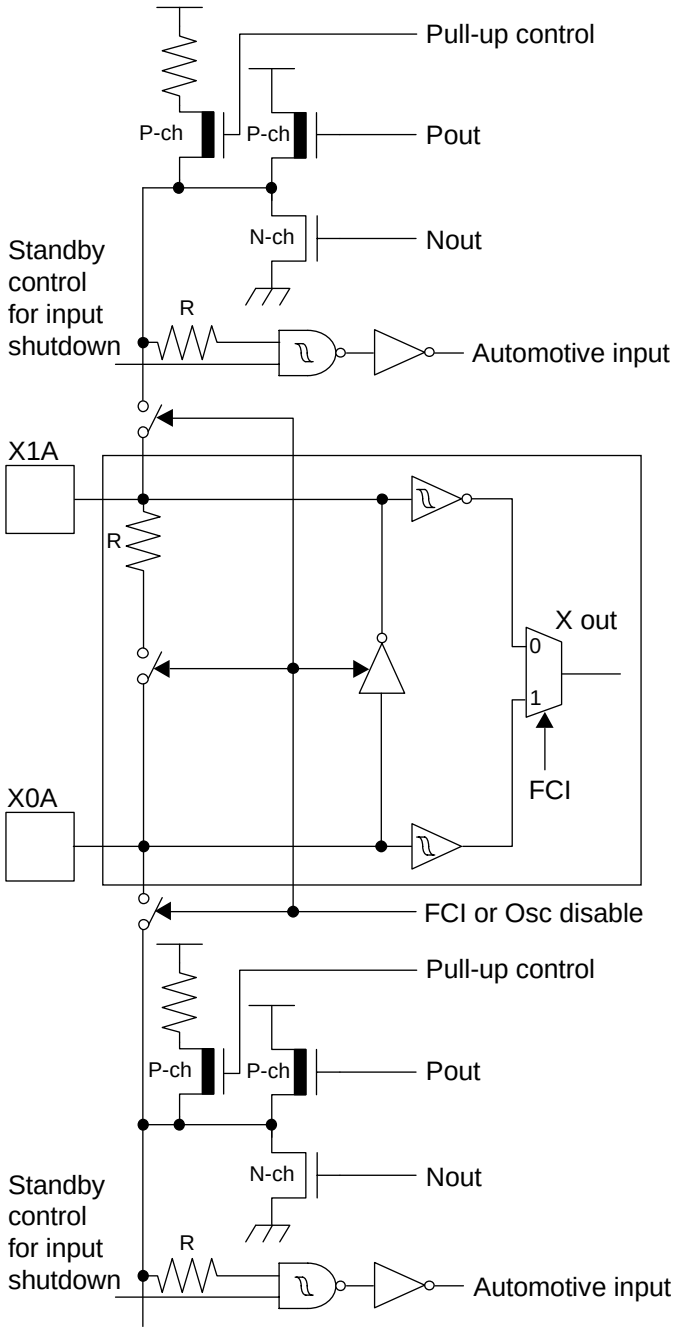
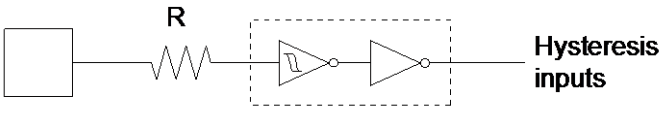
Applications of "Embedded - Microcontrollers"

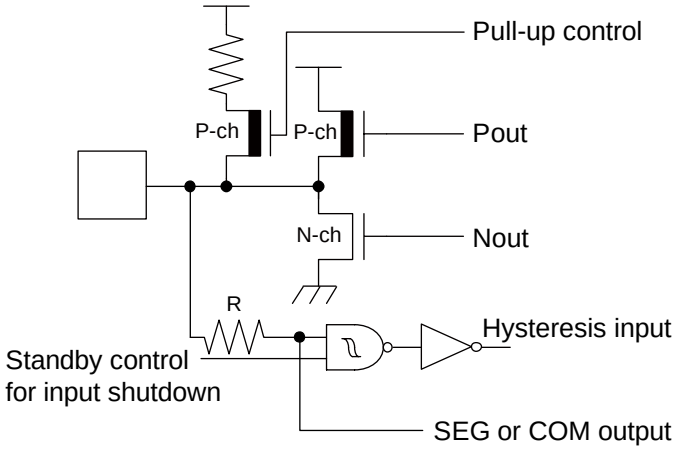
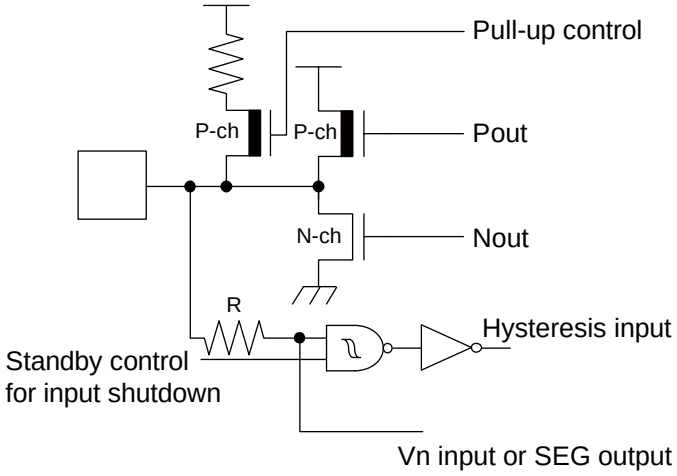
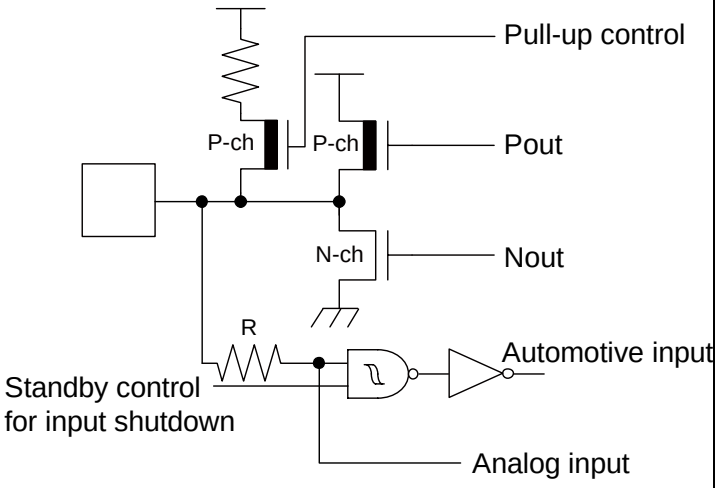
Details	
Product Status	Active
Core Processor	F²MC-16FX
Core Size	16-Bit
Speed	32MHz
Connectivity	CANbus, I²C, LINbus, SCI, UART/USART
Peripherals	DMA, LCD, LVD, POR, PWM, WDT
Number of I/O	79
Program Memory Size	288KB (288K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	16K x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 5.5V
Data Converters	A/D 27x8/10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	100-LQFP
Supplier Device Package	100-LQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/mb96f6b6rbpmc-gse2

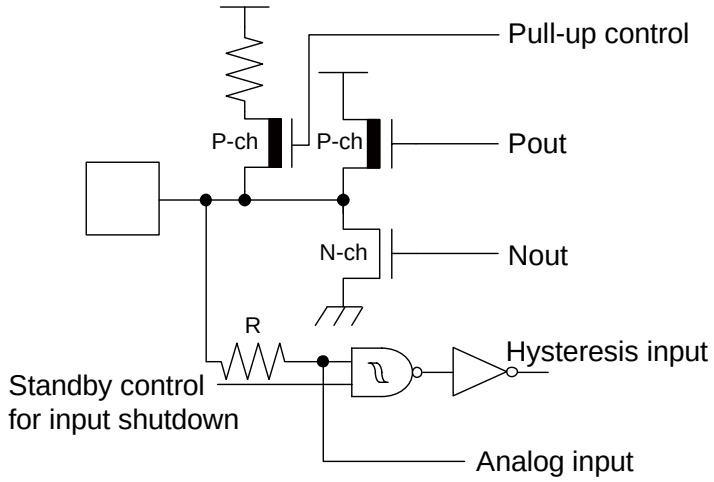
- Flash Memory
  - Dual operation flash allowing reading of one Flash bank while programming or erasing the other bank
  - Command sequencer for automatic execution of programming algorithm and for supporting DMA for programming of the Flash Memory
  - Supports automatic programming, Embedded Algorithm
  - Write/Erase/Erase-Suspend/Resume commands
  - A flag indicating completion of the automatic algorithm
  - Erase can be performed on each sector individually
  - Sector protection
  - Flash Security feature to protect the content of the Flash
  - Low voltage detection during Flash erases or writes

6. I/O Circuit Type

Type	Circuit	Remarks
A		High-speed oscillation circuit: • Programmable between oscillation mode (external crystal or resonator connected to X0/X1 pins) and Fast external Clock Input (FCI) mode (external clock connected to X0 pin) • Feedback resistor = approx. 1.0MΩ • The amplitude: 1.8V±0.15V to operate by the internal supply voltage

Type	Circuit	Remarks
B		Low-speed oscillation circuit shared with GPIO functionality: • Feedback resistor = approx. 5.0MΩ • GPIO functionality selectable (CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA), Automotive input with input shutdown function and programmable pull-up resistor)
C		CMOS hysteresis input pin

Type	Circuit	Remarks
P		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis inputs with input shutdown function • Programmable pull-up resistor • SEG or COM output
Q		• CMOS level output (I_{OL} = 4mA, I_{OH} = -4mA) • CMOS hysteresis inputs with input shutdown function • Programmable pull-up resistor • Vn input or SEG output
V		• CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 20mA, I_{OH} = -20mA) • Automotive input with input shutdown function • Programmable pull-up resistor • Analog input

Type	Circuit	Remarks
W		• CMOS level output (programmable I_{OL} = 4mA, I_{OH} = -4mA and I_{OL} = 20mA, I_{OH} = -20mA) • CMOS hysteresis input with input shutdown function • Programmable pull-up resistor • Analog input

Vector number	Offset in vector table	Vector name	Cleared by DMA	Index in ICR to program	Description
121	218_H	SG1	No	121	Sound Generator 1
122	214_H	-	-	122	Reserved
123	210_H	-	-	123	Reserved
124	$20C_H$	-	-	124	Reserved
125	208_H	-	-	125	Reserved
126	204_H	-	-	126	Reserved
127	200_H	-	-	127	Reserved
128	$1FC_H$	-	-	128	Reserved
129	$1F8_H$	-	-	129	Reserved
130	$1F4_H$	-	-	130	Reserved
131	$1F0_H$	-	-	131	Reserved
132	$1EC_H$	-	-	132	Reserved
133	$1E8_H$	FLASHA	Yes	133	Flash memory A interrupt
134	$1E4_H$	-	-	134	Reserved
135	$1E0_H$	-	-	135	Reserved
136	$1DC_H$	-	-	136	Reserved
137	$1D8_H$	QPRC0	Yes	137	Quadrature Position/Revolution counter 0
138	$1D4_H$	QPRC1	Yes	138	Quadrature Position/Revolution counter 1
139	$1D0_H$	ADCRC0	No	139	A/D Converter 0 - Range Comparator
140	$1CC_H$	ADCPD0	No	140	A/D Converter 0 - Pulse detection
141	$1C8_H$	-	-	141	Reserved
142	$1C4_H$	-	-	142	Reserved
143	$1C0_H$	-	-	143	Reserved

12. Handling Precautions

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your Cypress semiconductor devices.

12.1 Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

■Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of certain established limits, called absolute maximum ratings. Do not exceed these ratings.

■Recommended Operating Conditions

Recommended operating conditions are normal operating ranges for the semiconductor device. All the device's electrical characteristics are warranted when operated within these ranges.

Always use semiconductor devices within the recommended operating conditions. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their sales representative beforehand.

■Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.

1. Preventing Over-Voltage and Over-Current Conditions

   Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
2. Protection of Output Pins

   Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
   Therefore, avoid this type of connection.
3. Handling of Unused Input Pins

   Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

■Latch-up

Semiconductor devices are constructed by the formation of P-type and N-type areas on a substrate. When subjected to abnormally high voltages, internal parasitic PNPN junctions (called thyristor structures) may be formed, causing large current levels in excess of several hundred mA to flow continuously at the power supply pin. This condition is called latch-up.

CAUTION: The occurrence of latch-up not only causes loss of reliability in the semiconductor device, but can cause injury or damage from high heat, smoke or flame. To prevent this from happening, do the following:

1. Be sure that voltages applied to pins do not exceed the absolute maximum ratings. This should include attention to abnormal noise, surge levels, etc.
2. Be sure that abnormal current flows do not occur during the power-on sequence.

■Observance of Safety Regulations and Standards

Most countries in the world have established standards and regulations regarding safety, protection from electromagnetic interference, etc. Customers are requested to observe applicable regulations and standards in the design of products.

■Fail-Safe Design

Any semiconductor devices have inherently a certain rate of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

13.8 Pin handling when not using the A/D converter

If the A/D converter is not used, the power supply pins for A/D converter should be connected such as $AV_{CC} = V_{CC}$, AV_{SS} = AVRH = AVRL = V_{SS}.

13.9 Notes on Power-on

To prevent malfunction of the internal voltage regulator, supply voltage profile while turning the power supply on should be slower than 50µs from 0.2V to 2.7V.

13.10 Stabilization of power supply voltage

If the power supply voltage varies acutely even within the operation safety range of the V_{CC} power supply voltage, a malfunction may occur. The V_{CC} power supply voltage must therefore be stabilized. As stabilization guidelines, the power supply voltage must be stabilized in such a way that V_{CC} ripple fluctuations (peak to peak value) in the commercial frequencies (50Hz to 60Hz) fall within 10% of the standard V_{CC} power supply voltage and the transient fluctuation rate becomes 0.1V/µs or less in instantaneous fluctuation for power supply switching.

13.11 Serial communication

There is a possibility to receive wrong data due to noise or other causes on the serial communication.

Therefore, design a printed circuit board so as to avoid noise.

Consider receiving of wrong data when designing the system. For example apply a checksum and retransmit the data if an error occurs.

13.12 Mode Pin (MD)

Connect the mode pin directly to Vcc or Vss pin. To prevent the device unintentionally entering test mode due to noise, lay out the printed circuit board so as to minimize the distance from the mode pin to Vcc or Vss pin and provide a low-impedance connection.

14. Electrical Characteristics

14.1 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit	Remarks
			Min	Max		
Power supply voltage*1	V_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	
Analog power supply voltage*1	AV_{CC}	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_{CC} = AV_{CC}$*2
Analog reference voltage*1	AVRH, AVRL	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$AV_{CC} \geq$ AVRH, $AV_{CC} \geq$ AVRL, AVRH > AVRL, AVRL ≥ AV_{SS}
LCD power supply voltage*1	V0 to V3	-	V_{SS} - 0.3	V_{SS} + 6.0	V	V0 to V3 must not exceed V_{CC}
Input voltage*1	V_I	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_I \leq V_{CC}$ + 0.3V*3
Output voltage*1	V_O	-	V_{SS} - 0.3	V_{SS} + 6.0	V	$V_O \leq V_{CC}$ + 0.3V*3
Maximum Clamp Current	I_{CLAMP}	-	-4.0	+4.0	mA	Applicable to general purpose I/O pins *4
Total Maximum Clamp Current	$\Sigma\|I_{CLAMP}\|$	-	-	26	mA	Applicable to general purpose I/O pins *4
"L" level maximum output current	I_{OL}	-	-	15	mA	Normal port
	I_{OLHCO}	-	-	20	mA	High current port
"L" level average output current	I_{OLAV}	-	-	4	mA	Normal port
	$I_{OLAVHCO}$	-	-	15	mA	High current port
"L" level maximum overall output current	ΣI_{OL}	-	-	64	mA	Normal port
	ΣI_{OLHCO}	-	-	150	mA	High current port
"L" level average overall output current	ΣI_{OLAV}	-	-	32	mA	Normal port
	$\Sigma I_{OLAVHCO}$	-	-	100	mA	High current port
"H" level maximum output current	I_{OH}	-	-	-15	mA	Normal port
	I_{OHHCO}	-	-	-20	mA	High current port
"H" level average output current	I_{OHAV}	-	-	-4	mA	Normal port
	$I_{OHAVHCO}$	-	-	-15	mA	High current port
"H" level maximum overall output current	ΣI_{OH}	-	-	-64	mA	Normal port
	ΣI_{OHHCO}	-	-	-150	mA	High current port
"H" level average overall output current	ΣI_{OHAV}	-	-	-32	mA	Normal port
	$\Sigma I_{OHAVHCO}$	-	-	-100	mA	High current port
Power consumption*5	P_D	T_A= +125°C	-	416*6	mW	
Operating ambient temperature	T_A	-	-40	+125*7	°C	
Storage temperature	T_{STG}	-	-55	+150	°C	

*1: This parameter is based on $V_{SS} = AV_{SS}$ = 0V.

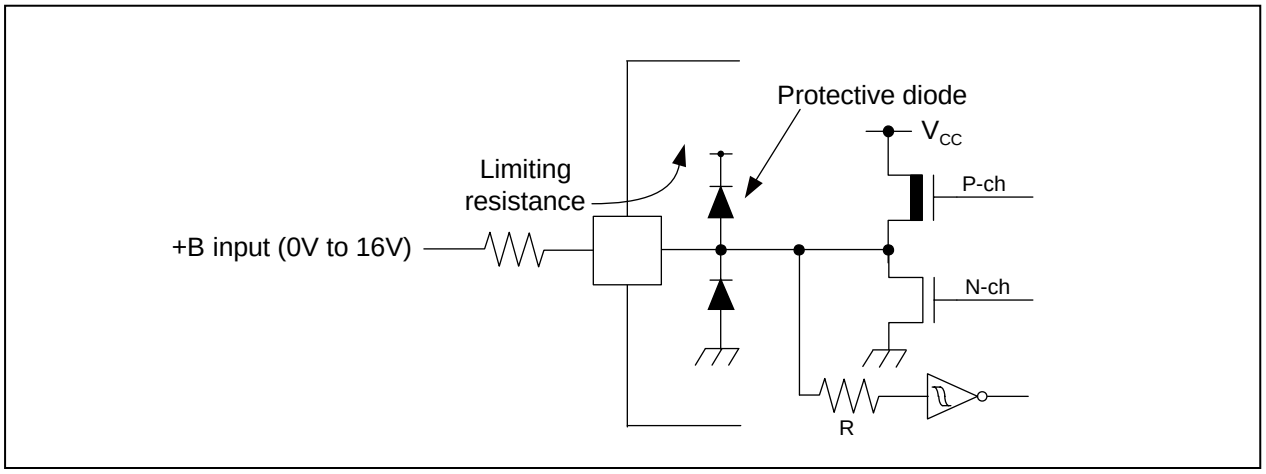
*2: AV_{CC} and V_{CC} must be set to the same voltage. It is required that AV_{CC} does not exceed V_{CC} and that the voltage at the analog inputs does not exceed AV_{CC} when the power is switched on.

*3: V_I and V_O should not exceed V_{CC} + 0.3V. V_I should also not exceed the specified ratings. However if the maximum current to/from an input is limited by some means with external components, the I_{CLAMP} rating supersedes the V_I rating. Input/Output voltages of general I/O ports depend on V_{CC}.

*4: Applicable to all general purpose I/O pins (Pnn_m).

- Use within recommended operating conditions.
- Use at DC voltage (current).
- The +B signal should always be applied a limiting resistance placed between the +B signal and the microcontroller.
- The value of the limiting resistance should be set so that when the +B signal is applied the input current to the microcontroller pin does not exceed rated values, either instantaneously or for prolonged periods.
- Note that when the microcontroller drive current is low, such as in the power saving modes, the +B input potential may pass through the protective diode and increase the potential at the VCC pin, and this may affect other devices.
- Note that if a +B signal is input when the microcontroller power supply is off (not fixed at 0V), the power supply is provided from the pins, so that incomplete operation may result.
- Note that if the +B input is applied during power-on, the power supply is provided from the pins and the resulting supply voltage may not be sufficient to operate the Power reset.
- The DEBUG I/F pin has only a protective diode against VSS. Hence it is only permitted to input a negative clamping current (4mA). For protection against positive input voltages, use an external clamping diode which limits the input voltage to maximum 6.0V.

- Sample recommended circuits:



*5: The maximum permitted power dissipation depends on the ambient temperature, the air flow velocity and the thermal conductance of the package on the PCB.
The actual power dissipation depends on the customer application and can be calculated as follows:
$P_D = P_{IO} + P_{INT}$
$P_{IO} = \Sigma (V_{OL} \times I_{OL} + V_{OH} \times I_{OH})$ (I/O load power dissipation, sum is performed on all I/O ports)
$P_{INT} = V_{CC} \times (I_{CC} + I_A)$ (internal power dissipation)
I_{CC} is the total core current consumption into V_{CC} as described in the “DC characteristics” and depends on the selected operation mode and clock frequency and the usage of functions like Flash programming.
I_A is the analog current consumption into AV_{CC}.

*6: Worst case value for a package mounted on single layer PCB at specified T_A without air flow.

*7: Write/erase to a large sector in flash memory is warranted with $T_A \leq +105°C$.

WARNING

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current in Timer modes*2	I_{CCTPLL}	Vcc	PLL Timer mode with CLKPLL = 32MHz (CLKRC and CLKSC stopped)	-	1800	2250	µA	T_A = +25°C
				-	-	3220	µA	T_A = +105°C
				-	-	4200	µA	T_A = +125°C
	$I_{CCTMAIN}$		Main Timer mode with CLKMC = 4MHz, SMCR:LPMSS = 0 (CLKPLL, CLKRC and CLKSC stopped)	-	285	330	µA	T_A = +25°C
				-	-	1200	µA	T_A = +105°C
				-	-	2155	µA	T_A = +125°C
	I_{CCTRCH}		RC Timer mode with CLKRC = 2MHz, SMCR:LPMSS = 0 (CLKPLL, CLKMC and CLKSC stopped)	-	160	215	µA	T_A = +25°C
				-	-	1110	µA	T_A = +105°C
				-	-	2065	µA	T_A = +125°C
	I_{CCTRCL}		RC Timer mode with CLKRC = 100kHz, (CLKPLL, CLKMC and CLKSC stopped)	-	35	75	µA	T_A = +25°C
				-	-	910	µA	T_A = +105°C
				-	-	1870	µA	T_A = +125°C
	I_{CCTSUB}		Sub Timer mode with CLKSC = 32kHz (CLKMC, CLKPLL and CLKRC stopped)	-	25	65	µA	T_A = +25°C
				-	-	885	µA	T_A = +105°C
				-	-	1845	µA	T_A = +125°C

Parameter	Symbol	Pin name	Conditions	Value			Unit	Remarks
				Min	Typ	Max		
Input leak current	I_{IL}	Pnn_m	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 1	-	+ 1	µA	Single port pin except high current output I/O
		P08_m, P09_m, P10_m	$V_{SS} < V_I < V_{CC}$ AV_{SS}, AVRL < V_I < AV_{CC}, AVRH	- 3	-	+ 3	µA	
Total LCD leak current	$\Sigma\|I_{ILCD}\|$	All SEG/ COM pin	V_{CC} = 5.0V	-	0.5	10	µA	Maximum leakage current of all LCD pins
Internal LCD divide resistance	R_{LCD}	Between V3 and V2, V2 and V1, V1 and V0	V_{CC} = 5.0V	6.25	12.5	25	kΩ	
Pull-up resistance value	R_{PU}	Pnn_m	V_{CC} = 5.0V ±10%	25	50	100	kΩ	
Input capacitance	C_{IN}	Other than C, Vcc, Vss, AVcc, AVss, AVRH, AVRL, P08_m, P09_m, P10_m	-	-	5	15	pF	
		P08_m, P09_m, P10_m	-	-	15	30	pF	

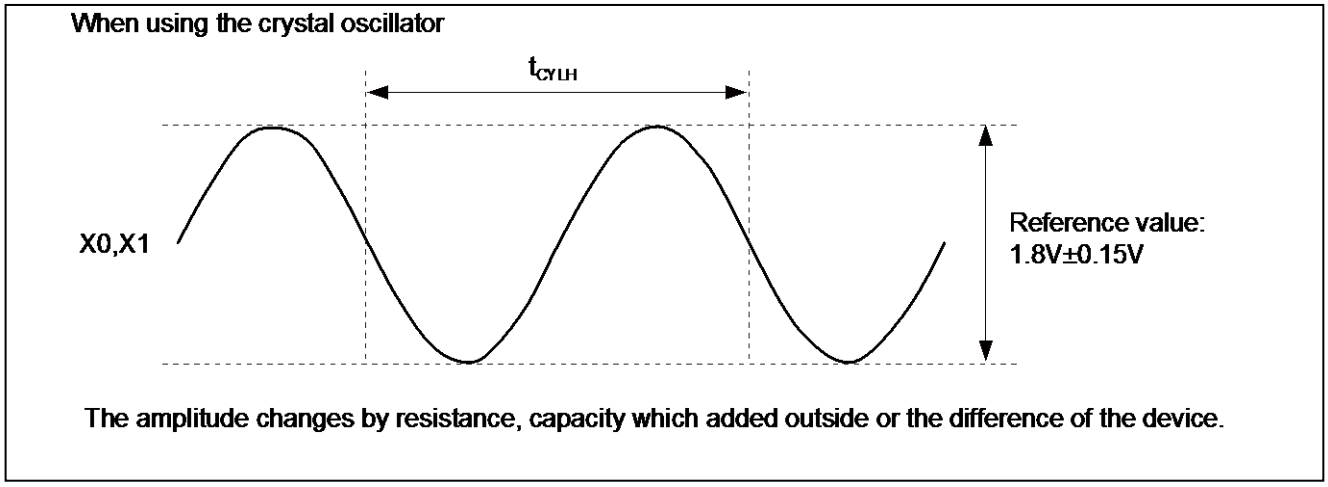
*: In the case of high current outputs, set "1" to the bit in the Port High Drive Register.

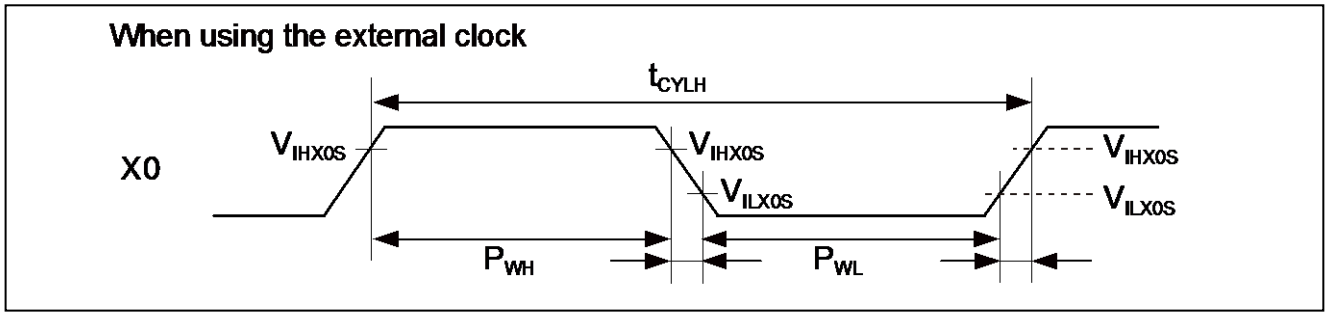
14.4 AC Characteristics

14.4.1 Main Clock Input Characteristics

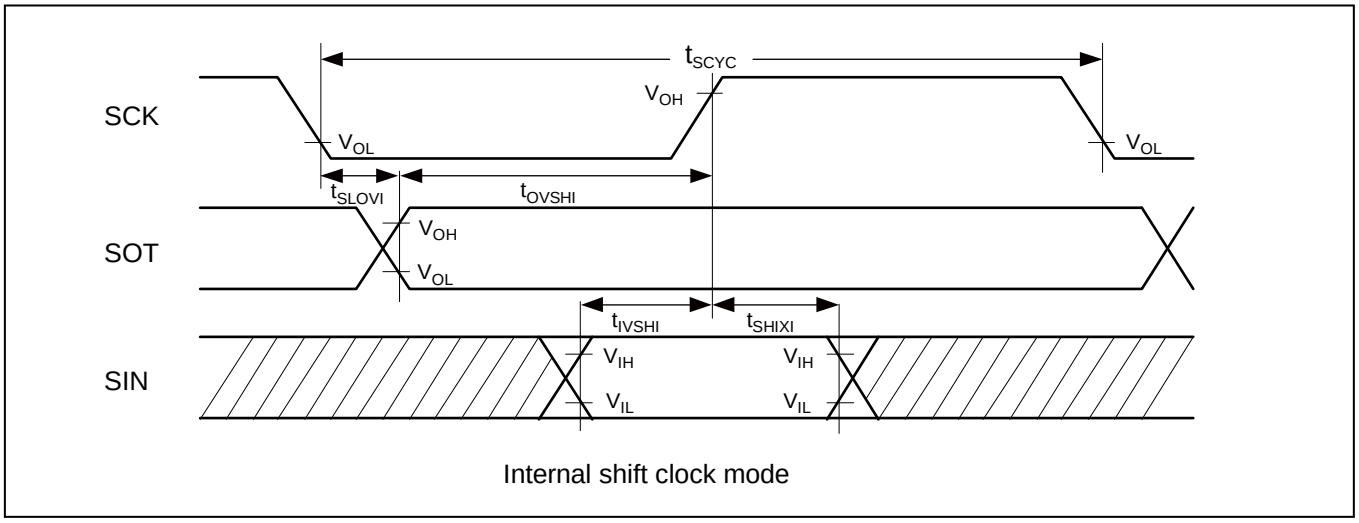
(V_{CC} = AV_{CC} = 2.7V to 5.5V, VD=1.8V±0.15V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Input frequency	f_C	X0, X1	4	-	8	MHz	When using a crystal oscillator, PLL off
			-	-	8	MHz	When using an opposite phase external clock, PLL off
			4	-	8	MHz	When using a crystal oscillator or opposite phase external clock, PLL on
Input frequency	f_{FCI}	X0	-	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL off
			4	-	8	MHz	When using a single phase external clock in “Fast Clock Input mode”, PLL on
Input clock cycle	t_{CYLH}	-	125	-	-	ns	
Input clock pulse width	P_{WH}, P_{WL}	-	55	-	-	ns	

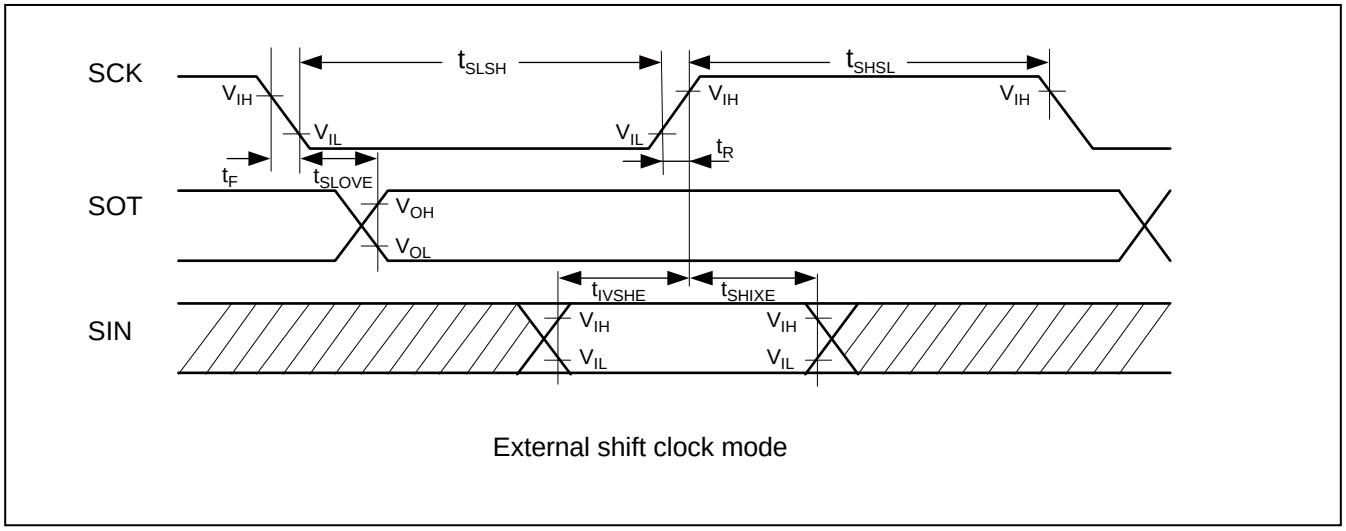




t_{SCYC}	N
$4 \times t_{CLKP1}$	2
$5 \times t_{CLKP1}$, $6 \times t_{CLKP1}$	3
$7 \times t_{CLKP1}$, $8 \times t_{CLKP1}$	4
...	...



Internal shift clock mode



External shift clock mode

14.4.10 I^2C Timing

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter	Symbol	Conditions	Typical mode		High-speed mode*4		Unit
			Min	Max	Min	Max	
SCL clock frequency	f_{SCL}	C_L = 50pF, R = (V_p/I_{OL})*1	0	100	0	400	kHz
(Repeated) START condition hold time SDA ↓ → SCL ↓	t_{HDSTA}		4.0	-	0.6	-	µs
SCL clock "L" width	t_{LOW}		4.7	-	1.3	-	µs
SCL clock "H" width	t_{HIGH}		4.0	-	0.6	-	µs
(Repeated) START condition setup time SCL ↑ →SDA ↓	t_{SUSTA}		4.7	-	0.6	-	µs
Data hold time SCL ↓ → SDA ↓ ↑	t_{HDDAT}		0	3.45*2	0	0.9*3	µs
Data setup time SDA ↓ ↑ → SCL ↑	t_{SUDAT}		250	-	100	-	ns
STOP condition setup time SCL ↑ → SDA ↑	t_{SUSTO}		4.0	-	0.6	-	µs
Bus free time between "STOP condition" and "START condition"	t_{BUS}		4.7	-	1.3	-	µs
Pulse width of spikes which will be suppressed by input noise filter	t_{SP}	-	0	(1-1.5) × t_{CLKP1}*5	0	(1-1.5) × t_{CLKP1}*5	ns

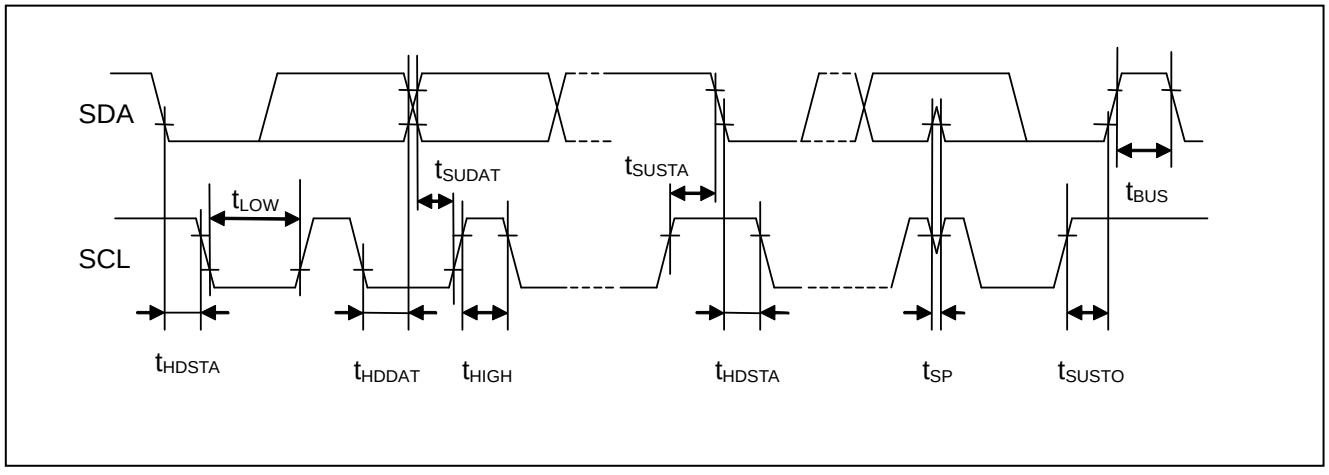
*1: R and C_L represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and I_{OL} indicates V_{OL} guaranteed current.

*2: The maximum t_{HDDAT} only has to be met if the device does not extend the "L" width (t_{LOW}) of the SCL signal.

*3: A high-speed mode I^2C bus device can be used on a standard mode I^2C bus system as long as the device satisfies the requirement of "t_{SUDAT} ≥ 250ns".

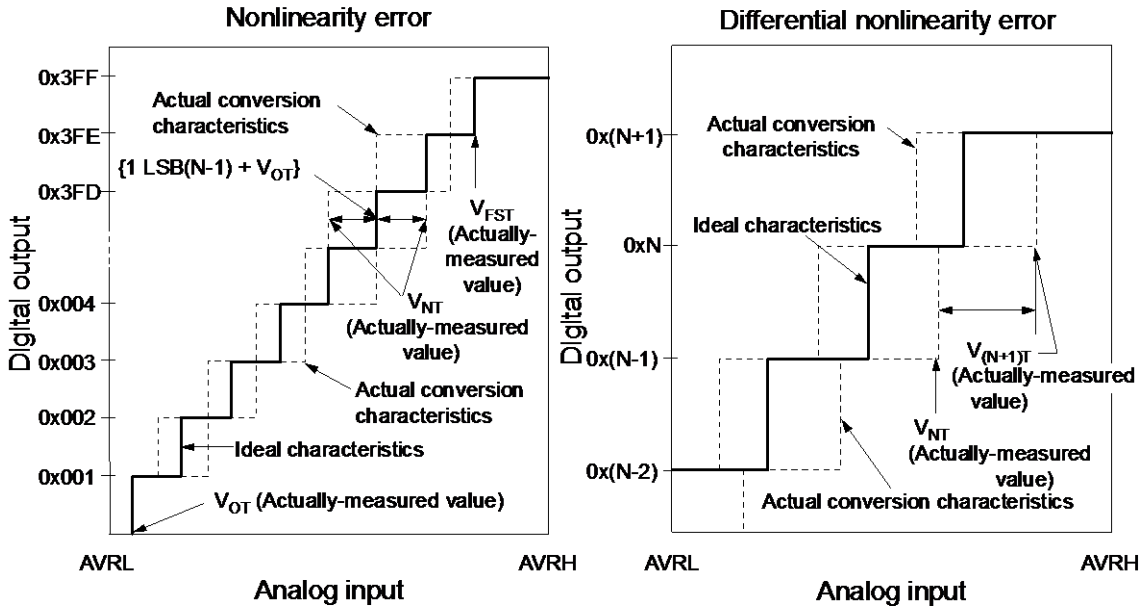
*4: For use at over 100 kHz, set the peripheral clock1 (CLKP1) to at least 6MHz.

*5: t_{CLKP1} indicates the peripheral clock1 (CLKP1) cycle time.



14.5.3 Definition of A/D Converter Terms

- Resolution : Analog variation that is recognized by an A/D converter.
- Nonlinearity error : Deviation of the actual conversion characteristics from a straight line that connects the zero transition point (0b0000000000 ⟷ 0b0000000001) to the full-scale transition point (0b1111111110 ⟷ 0b1111111111).
- Differential nonlinearity error : Deviation from the ideal value of the input voltage that is required to change the output code by 1LSB.
- Total error : Difference between the actual value and the theoretical value. The total error includes zero transition error, full-scale transition error and nonlinearity error.
- Zero transition voltage : Input voltage which results in the minimum conversion value.
- Full scale transition voltage: Input voltage which results in the maximum conversion value.

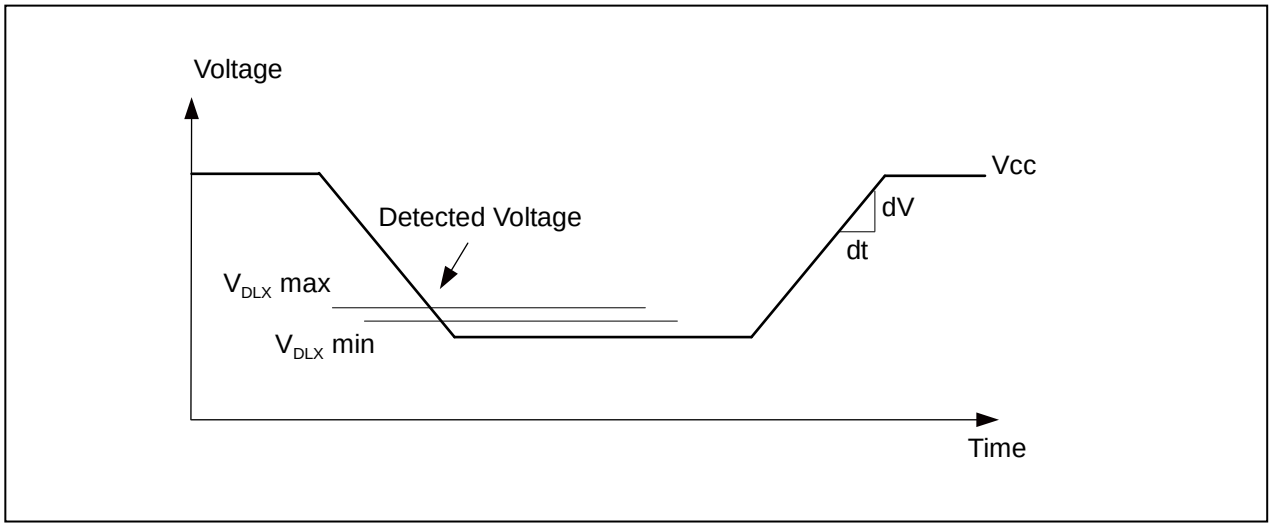


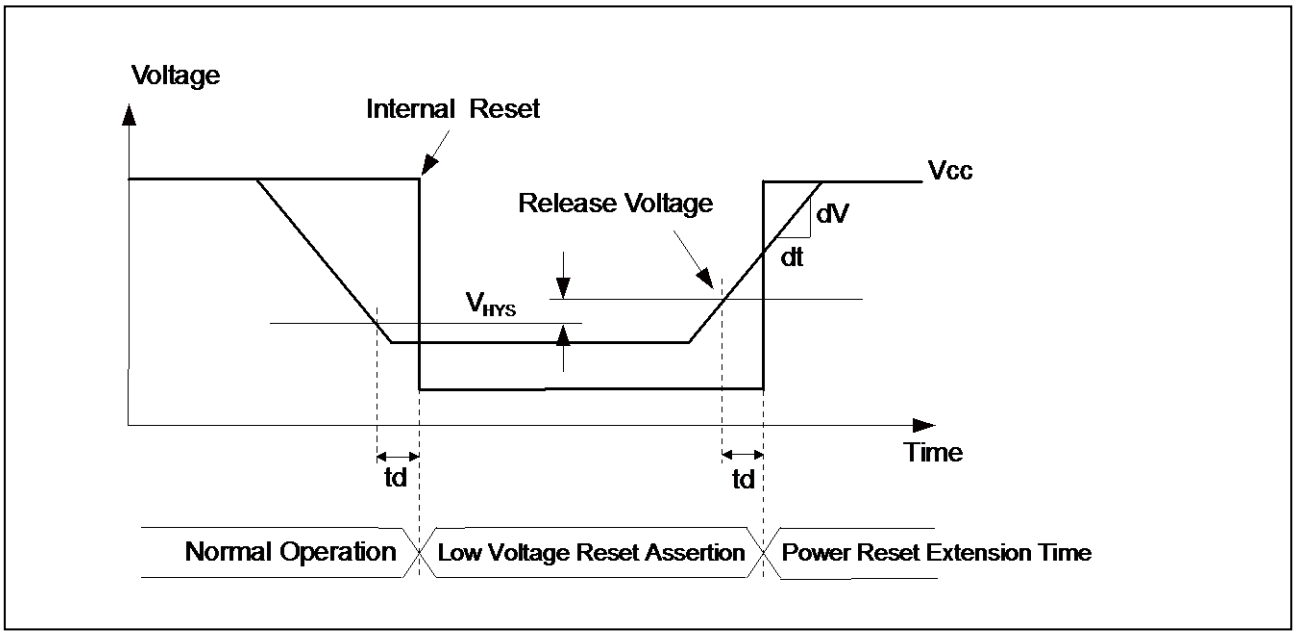
$$\text{Nonlinearity error of digital output N} = \frac{V_{NT} - \{1LSB \times (N - 1) + V_{OT}\}}{1LSB} \text{ [LSB]}$$

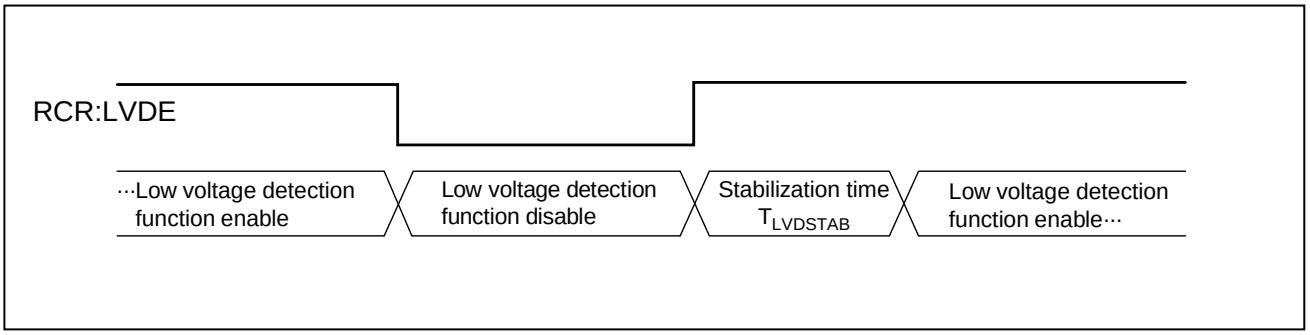
$$\text{Differential nonlinearity error of digital output N} = \frac{V_{(N+1)T} - V_{NT}}{1LSB} - 1 \text{ [LSB]}$$

$$1LSB = \frac{V_{FST} - V_{OT}}{1022}$$

N : A/D converter digital output value.
V_{OT} : Voltage at which the digital output changes from 0x000 to 0x001.
V_{FST} : Voltage at which the digital output changes from 0x3FE to 0x3FF.
V_{NT} : Voltage at which the digital output changes from 0x(N − 1) to 0xN.


Voltage
Vcc
Detected Voltage
dV
dt
V_{DLX} max
V_{DLX} min
Time


Voltage
Internal Reset
Vcc
Release Voltage
dV
dt
V_{HYS}
Time
td
td
Normal Operation
Low Voltage Reset Assertion
Power Reset Extension Time


RCR:LVDE
···Low voltage detection function enable
Low voltage detection function disable
Stabilization time $T_{LVDSTAB}$
Low voltage detection function enable···

14.8 Flash Memory Write/Erase Characteristics

(V_{CC} = AV_{CC} = 2.7V to 5.5V, V_{SS} = AV_{SS} = 0V, T_A = - 40°C to + 125°C)

Parameter		Conditions	Value			Unit	Remarks
			Min	Typ	Max		
Sector erase time	Large Sector	T_A ≤ + 105°C	-	1.6	7.5	s	Includes write time prior to internal erase.
	Small Sector	-	-	0.4	2.1	s	
	Security Sector	-	-	0.31	1.65	s	
Word (16-bit) write time	Large Sector	T_A ≤ + 105°C	-	25	400	µs	Not including system-level overhead time.
	Small Sector	-	-	25	400	µs	
Chip erase time		T_A ≤ + 105°C	-	8.31	40.05	s	Includes write time prior to internal erase.

Note:

While the Flash memory is written or erased, shutdown of the external power (V_{CC}) is prohibited. In the application system where the external power (V_{CC}) might be shut down while writing or erasing, be sure to turn the power off by using a low voltage detection function.

To put it concrete, change the external power in the range of change ration of power supply voltage (-0.004V/µs to +0.004V/µs) after the external power falls below the detection voltage (V_{DLX})[*1].

Write/Erase cycles and data hold time

Write/Erase cycles (cycle)	Data hold time (year)
1,000	20 [*2]
10,000	10 [*2]
100,000	5 [*2]

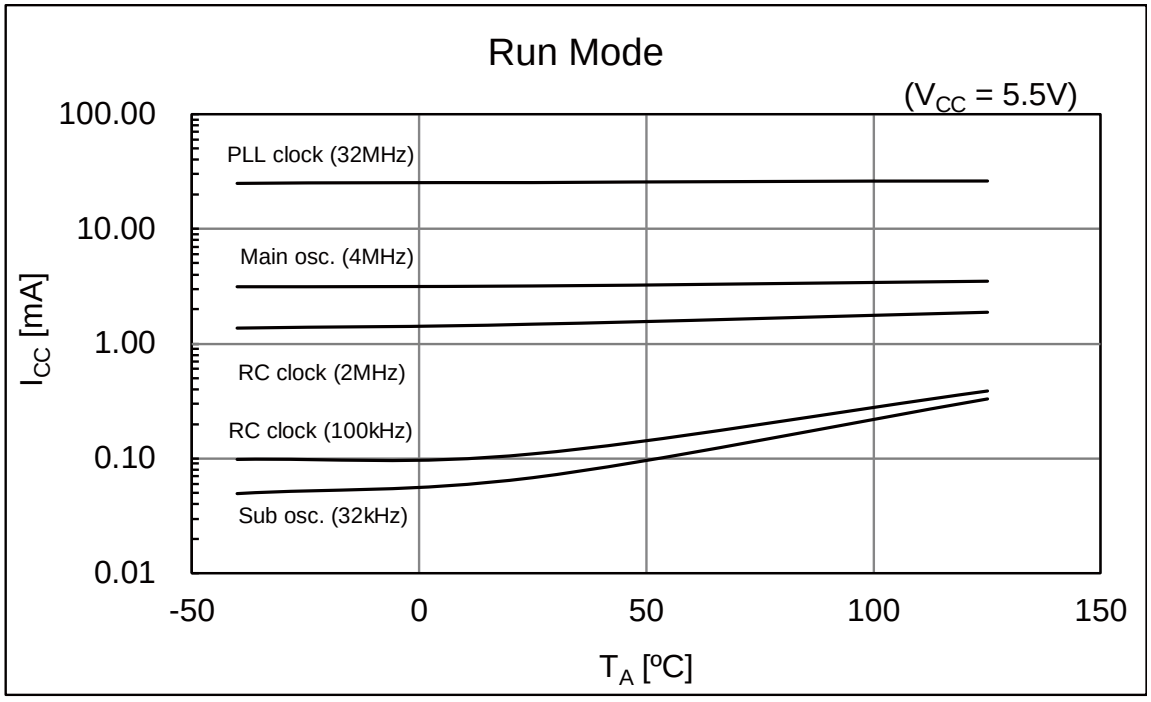
*1: See "14.7 Low Voltage Detection Function Characteristics".

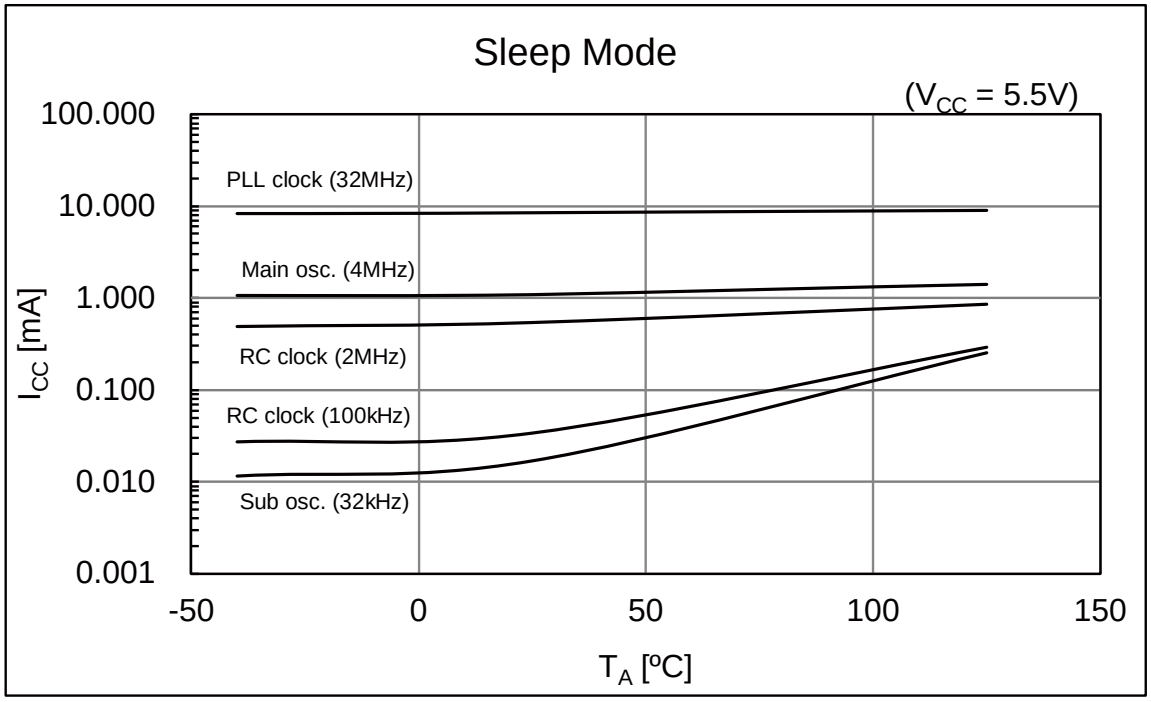
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at + 85°C).

15. Example Characteristics

This characteristic is an actual value of the arbitrary sample. It is not the guaranteed value.

■MB96F6B6





■Used setting

Mode	Selected Source Clock	Clock/Regulator and FLASH Settings
Run mode	PLL	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32MHz
	Main osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 4MHz
	RC clock fast	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 2MHz
	RC clock slow	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 100kHz
	Sub osc.	CLKS1 = CLKS2 = CLKB = CLKP1 = CLKP2 = 32kHz
Sleep mode	PLL	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	Main osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 4MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock fast	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 2MHz Regulator in High Power Mode, (CLKB is stopped in this mode)
	RC clock slow	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 100kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
	Sub osc.	CLKS1 = CLKS2 = CLKP1 = CLKP2 = 32kHz Regulator in Low Power Mode, (CLKB is stopped in this mode)
Timer mode	PLL	CLKMC = 4MHz, CLKPLL = 32MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	Main osc.	CLKMC = 4MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock fast	CLKMC = 2MHz (System clocks are stopped in this mode) Regulator in High Power Mode, FLASH in Power-down / reset mode
	RC clock slow	CLKMC = 100kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
	Sub osc.	CLKMC = 32 kHz (System clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode
Stop mode	stopped	(All clocks are stopped in this mode) Regulator in Low Power Mode, FLASH in Power-down / reset mode