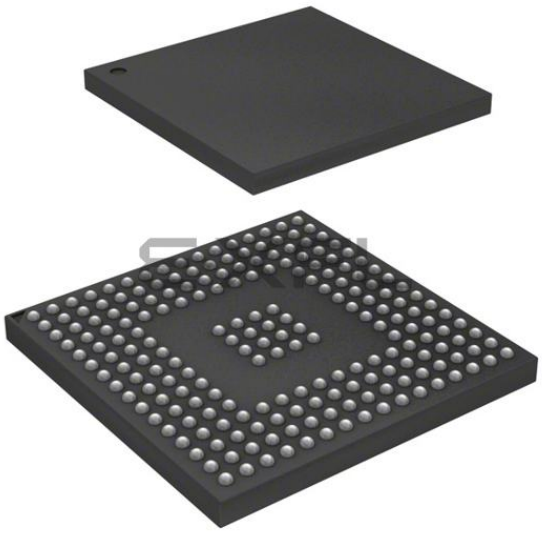

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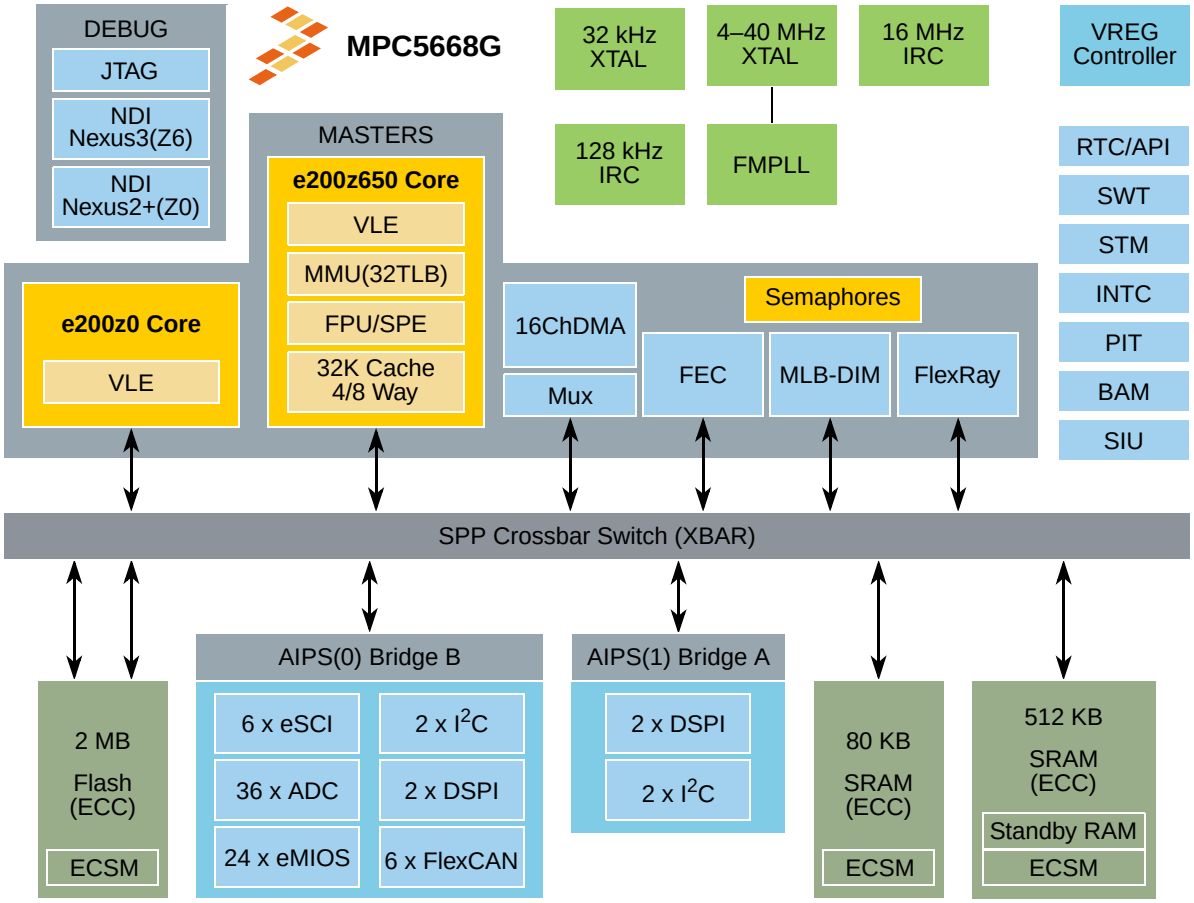
Details	
Product Status	Active
Core Processor	e200z650
Core Size	32-Bit Single-Core
Speed	116MHz
Connectivity	CANbus, Ethernet, I²C, LINbus, SCI, SPI
Peripherals	DMA, POR, PWM, WDT
Number of I/O	155
Program Memory Size	2MB (2M x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	592K x 8
Voltage - Supply (Vcc/Vdd)	3V ~ 5.5V
Data Converters	A/D 36x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	208-BGA
Supplier Device Package	208-BGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/spc5668gf1ammgr

2 MPC5668x Block Diagrams

Figure 1 shows a top-level block diagram of the MPC5668G device.



LEGEND

ADC	– Analog to Digital Converter	**I²C**	– Inter IC Controller
BAM	– Boot Assist Module	**INTC**	– Interrupt Controller
DSPI	– Serial Peripherals Interface	**JTAG**	– Joint Test Action Group interface
ECC	– Error Correction Code	**MLB-DIM**	– Media Local Bus Device Interface Module
ECSM	– Error Correction Status Module	**NDI**	– Nexus Debug Interface
eMIOS	– Timed Input Output	**PIT**	– Periodic Interrupt Timer
eDMA	– Enhanced Direct Memory Access controller	**RTC**	– Real Time Clock
eSCI	– Serial Communications Interface	**SIU**	– System Integration
FEC	– Fast Ethernet Controller	**STM**	– System Timer Module
FlexCAN	– Controller Area Network controller	**SWT**	– Software Watchdog Timer
FlexRay™	– FlexRay Bus Controller	**VREG**	– Voltage Regulator
FMPLL	– Frequency Modulated Phase Locked Loop		

Figure 1. MPC5668G Block Diagram

3 Pin Assignments

3.1 208-ball MAPBGA Pin Assignments

Figure 3 shows the 208-ball MAPBGA pin assignments.

Figure 3. MPC5668x 208-ball MAPBGA (full diagram)

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PA6	PA[6] AN[6]	6	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	H16	H16
PA7	PA[7] AN[7]	7	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	G14	G14
PA8	PA[8] AN[8]	8	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F14	F14
PA9	PA[9] AN[9]	9	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E14	E14
PA10	PA[10] AN[10]	10	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D13	D13
PA11	PA[11] AN[11]	11	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	E13	E13
PA12	PA[12] AN[12]	12	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	D14	D14
PA13	PA[13] AN[13]	13	00 01 10 11	Port A GPI ADC Analog Input — —	I I — —	V_{DDA}	IHA	—	—	F13	F13
PA14	PA[14] AN[14] EXTAL32	14	00 01 10 11	Port A GPI ADC Analog Input External 32 kHz Crystal In —	I I I —	V_{DDA}	IHA	—	—	D16	D16
PA15	PA[15] AN[15] XTAL32	15	00 01 10 11	Port A GPI ADC Analog Input External 32 kHz Crystal Out —	I I O —	V_{DDA}	IHA	—	—	E16	E16

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PE14	PE[14] SCL_A PCS_D[2]	78	00 01 10 11	Port E GPIO I^2C_A Serial Clock DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N7	N7
PE15	PE[15] SDA_A PCS_D[5]	79	00 01 10 11	Port E GPIO I^2C_A Serial Data DSPI_D Peripheral Chip Select —	I/O I/O O —	V_{DDE2}	SH	—	—	N6	N6
Port F (16)											
PF0	PF[0] SCK_A	80	00 01 10 11	Port F GPIO DSPI_A Serial Clock — —	I/O I/O — —	V_{DDE2}	MH	—	—	H2	H2
PF1	PF[1] SOUT_A	81	00 01 10 11	Port F GPIO DSPI_A Serial Data Out — —	I/O O — —	V_{DDE2}	MH	—	—	J1	J1
PF2	PF[2] SIN_A	82	00 01 10 11	Port F GPIO DSPI_A Serial Data In — —	I/O I — —	V_{DDE2}	SH	—	—	J2	J2
PF3	PF[3] PCS_A[0] PCS_B[5] PCS_C[4]	83	00 01 10 11	Port F GPIO DSPI_A Peripheral Chip Select DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	N2	N2
PF4	PF[4] SCK_B PCS_A[1] PCS_C[2]	84	00 01 10 11	Port F GPIO DSPI_B Serial Clock DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I/O O O	V_{DDE2}	MH	—	—	M1	M1
PF5	PF[5] SOUT_B PCS_A[2] PCS_C[3]	85	00 01 10 11	Port F GPIO DSPI_B Serial Data Out DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	P2	P2
PF6	PF[6] SIN_B PCS_A[3] PCS_C[5]	86	00 01 10 11	Port F GPIO DSPI_B Serial Data In DSPI_A Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	N1	N1
PF7	PF[7] PCS_B[0] PCS_C[5] PCS_D[4]	87	00 01 10 11	Port F GPIO DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select DSPI_D Peripheral Chip Select	I/O I/O O O	V_{DDE2}	SH	—	—	R2	R2

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PG13	PG[13] eMIOS[2] FEC_TXD[1] AN[61]	109	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	L16	L16
PG14	PG[14] eMIOS[1] FEC_TXD[2] AN[62]	110	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	M16	M16
PG15	PG[15] eMIOS[0] FEC_TXD[3] AN[63]	111	00 01 10 11	Port G GPIO eMIOS Channel Ethernet Transmit Data ADC Analog Input	I/O I/O O I	V_{DDE3}	MHA	—	—	N16	N16
Port H (16)											
PH0	PH[0] eMIOS[31] FEC_COL	112	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Collision —	I/O I/O I —	V_{DDE3}	SH	—	—	T14	T14
PH1	PH[1] eMIOS[30] FEC_RX_DV	113	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data Valid —	I/O I/O I —	V_{DDE3}	SH	—	—	P16	P16
PH2	PH[2] eMIOS[29] FEC_TX_EN	114	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Transmit Enable —	I/O I/O O —	V_{DDE3}	MH	—	—	R16	R16
PH3	PH[3] eMIOS[28] FEC_RX_ER	115	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Error —	I/O I/O I —	V_{DDE3}	SH	—	—	N15	N15
PH4	PH[4] eMIOS[27] FEC_RXD[0]	116	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	P15	P15
PH5	PH[5] eMIOS[26] FEC_RXD[1]	117	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R14	R14
PH6	PH[6] eMIOS[25] FEC_RXD[2]	118	00 01 10 11	Port H GPIO eMIOS Channel Ethernet Receive Data —	I/O I/O I —	V_{DDE3}	SH	—	—	R15	R15

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
PK6	PK[6] FR_B_RX PCS_B[1] PCS_C[4]	150	00 01 10 11	Port K GPIO FlexRay B Receive Data DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O I O O	V_{DDE2}	SH	—	—	R5	R5
PK7	PK[7] FR_B_TX PCS_B[2] PCS_C[5]	151	00 01 10 11	Port K GPIO FlexRay B Transmit Data DSPI_B Peripheral Chip Select DSPI_C Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	T5	T5
PK8	PK[8] FR_B_TX_EN PCS_B[3] PCS_A[1]	152	00 01 10 11	Port K GPIO FlexRay B Transmit Enable DSPI_B Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O O O O	V_{DDE2}	MH	—	—	R6	R6
PK9	PK[9] CLKOUT PCS_D[1] PCS_A[2] BOOTCFG	153	00 01 10 11	Port K GPIO CLKOUT (User mode) DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select Boot Configuration	I/O O O O I	V_{DDE2}	MH	BOOT CFG (Pull-down)	GPIO	T6	T6
PK10	PK[10] PCS_B[5] PCS_D[2] PCS_A[3]	154	00 01 10 11	Port K GPIO DSPI_B Peripheral Chip Select DSPI_D Peripheral Chip Select DSPI_A Peripheral Chip Select	I/O O O O	V_{DDE2}	SH	—	—	P6	P6
Nexus Pins (17)											
$\overline{\text{EVTI}}$	$\overline{\text{EVTI}}$	—	—	Nexus Event In	I	V_{DDENEX}	F	—	—	—	M11
$\overline{\text{EVTO}}$	$\overline{\text{EVTO}}$	—	—	Nexus Event Out	O	V_{DDENEX}	F	—	—	—	M12
$\overline{\text{MSEO0}}$	$\overline{\text{MSEO[0]}}$	—	—	Nexus Message Start/End Out	O	V_{DDENEX}	F	—	—	—	M9
$\overline{\text{MSEO1}}$	$\overline{\text{MSEO[1]}}$	—	—	Nexus Message Start/End Out	O	V_{DDENEX}	F	—	—	—	M8
MCKO	MCKO	—	—	Nexus Message Clock Out	O	V_{DDENEX}	F	—	—	—	M10
MDO0	MDO[0]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	E5
MDO1	MDO[1]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	F5
MDO2	MDO[2]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	G5
MDO3	MDO[3]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	H5
MDO4	MDO[4]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	H6
MDO5	MDO[5]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	J6
MDO6	MDO[6]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	J5
MDO7	MDO[7]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	K5
MDO8	MDO[8]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	L5
MDO9	MDO[9]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M5
MDO10	MDO[10]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M6

Table 2. MPC5668x Signal Properties (continued)

Pin Name[1]	Supported Functions[2]	GPIO (PCR) Num[3]	PA[4]	Description	I/O Type	Volt-age	Pad Type[5]	Status		Package Pin Locations	
								During Reset[6]	After Reset[7]	208 BGA	256 BGA
MDO11	MDO[11]	—	—	Nexus Message Data Out	O	V_{DDENEX}	F	—	—	—	M7
Miscellaneous Pins (9)											
EXTAL	EXTAL EXTCLK	—	—	Main Crystal Oscillator Input External Clock Input	I I	V_{DDSYN}	A	EXTAL		A14	A14
XTAL	XTAL	—	—	Main Crystal Oscillator Output	O	V_{DDSYN}	A	XTAL		A13	A13
TDI	TDI	—	—	JTAG Test Data Input	I	V_{DDE2}	SH	TDI (Pull Up)		J3	J3
TDO	TDO	—	—	JTAG Test Data Output	O	V_{DDE2}	MH	TDO (Pull Up[8])		M3	M3
TMS	TMS	—	—	JTAG Test Mode Select Input	I	V_{DDE2}	MH	TMS (Pull Up)		L3	L3
TCK	TCK	—	—	JTAG Test Clock Input	I	V_{DDE2}	SH	TCK (Pull Down)		P3	P3
JCOMP	JCOMP	—	—	JTAG Compliancy	I	V_{DDE2}	SH	JCOMP (Pull Down)		K3	K3
TEST	TEST	—	—	Test Mode Select	I	V_{DDE3}	IH	TEST[9]		M13	M13
$\overline{\text{RESET}}$	$\overline{\text{RESET}}$	—	—	External Reset	I/O	V_{DDE1}	MH	$\overline{\text{RESET}}$ (Pull Up)		A11	A11

1 The primary signal name is used as the pin label on the BGA map for identification purposes.

2 Each line in the Signal Name column corresponds to a separate signal function on the pin. For all device I/O pins, the primary, alternate, or GPIO signal functions are designated in the PA field of the System Integration Unit (SIU) PCR registers except where explicitly noted.

3 The GPIO number is the same as the corresponding pad configuration register (SIU_PCR*n*) number.

4 The PA bitfield in the SIU_PCR*n* register selects the signal function for the pin. A dash in the Description field of this table indicates that this value for PC is reserved on this pin, and should not be used.

5 The pad type is indicated by one or more of the following abbreviations: A–analog, F—fast speed, H–high voltage, I—input-only, M–medium speed, S–slow speed. For example, pad type SH designates a slow high-voltage pad.

6 The Status During Reset pin is sampled after the internal POR is negated. Prior to exiting POR, the signal has a high impedance. The terminology used in this column is: O – output, I – input, Up – weak pull up enabled, Down – weak pulldown enabled, Low – output driven low, High – output driven high. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin. The signal name to the left or right of the slash indicates the pin is enabled.

7 The Function After Reset of a GPI function is general purpose input. A dash on the left side of the slash denotes that both the input and output buffers for the pin are off. A dash on the right side of the slash denotes that there is no weak pull up/down enabled on the pin.

8 Pullup is enabled only when JCOMP is negated.

9 Tie to V_{SS} for normal operation.

3.3.1 Power and Ground Supply Summary

Table 3. MPC5668x Power/Ground

Pin Name	Function Description	Voltage[1]	Package Pin Locations	
			208	256
V_{DD}	Internal Logic Power	1.2 V	D4, D10, H4, G13, K13, N5	D4, D10, H4, G13, K13, N5
V_{DDE1}	External I/O Power	3.3–5.0 V	D6	D6
V_{DDE2}			L4	L4
V_{DDE3}			J13	J13
V_{DDE4}			N10	N10
V_{DDA}	Analog Power	3.3–5.0 V	B15	B15
V_{DD33}	3.3 V I/O Power	3.3 V	L13	L13
V_{DDEMLB}	Media Local Bus Power	2.5 or 3.3 V	K4	K4
V_{DDENEX}[2]	Nexus Power	3.3 V	—	E6, K11, L7
V_{RCSEL}	Voltage Regulator Select	V_{SSA} / V_{DDA}	H13	H13
V_{RC}	Voltage Regulator Control Voltage	3.3–5.0 V	B10	B10
V_{RCCTL}	Voltage Regulator Control Output	—[3]	B11	B11
V_{DDSYN}	Clock Synthesizer Power	3.3 V	A12	A12
V_{RH}	Analog High Voltage Reference	3.3–5.0 V	B16	B16
V_{RL}	Analog Low Voltage Reference	0 V	C16	C16
V_{SS}	Ground	0 V	A1, A16, D7, G4, G[7:10], H[7:10], J[7:10], K[7:10], N13, T1, T16	A1, A16, D7, E[7:12], F[7:12], G4, G[6:12], H[7:12], J[7:12], K[6:10], K12, L[8:10], L12, N13, T1, T16
V_{SSA}	Analog Ground	0 V	C15	C15
V_{SSSYN}	Clock Synthesizer Ground	0 V	A15	A15

1 Nominal voltages.

2 Dedicated Nexus power pin on 256-pin package only. On the 208-pin package, VDDENEX is tied to VSS internal to the package substrate and is not available externally.

3 Base current to external NPN power transistor. Voltage may vary.

4.3 ESD Characteristics

Table 6. ESD Ratings[1, 2]

Characteristic	Symbol	Value	Unit
ESD for Human Body Model (HBM)		2000	V
HBM Circuit Description	R1	1500	Ohm
	C	100	pF
ESD for Field Induced Charge Model (FDCM)		750 (corner pins)	V
		250 (all other pins)	
Number of Pulses per pin: Positive Pulses (HBM) Negative Pulses (HBM)	 — —	 1 1	 — —
Interval of Pulses	—	1	second

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

2 A device will be defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing shall be performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

4.4 VRC Electrical Specifications

Table 7. VRC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Units
1	Current which can be sourced by V_{RCCTL}	I_V_{RCCTL}	6.25 µA	20 mA	—
2	Minimum Required Gain from external circuit: I_{DD} / I_V_{RCCTL} (@V_{DD} = 1.32 V)[1] –40°C 25°C 150°C	BETA	 50 50 50	 500	

1 Assumes “typical usage” currents which will vary with application.

4.5 DC Electrical Specifications

Table 8. DC Electrical Specifications

Spec	Characteristic	Symbol	Min	Max	Unit
1	Maximum Operating Temperature Range — Die Junction Temperature	T_J	–40.0	150.0	°C
2	3.3 V Clock Synthesizer Voltage[1]	V_{DDSYN}	3.0	3.6	V
3	3.3 V I/O Buffer Voltage[1]	V_{DD33}	3.0	3.6	V
4	3.3–5.0 V Voltage Regulator Reference Voltage[1] V_{RCSEL} = V_{SSA} V_{RCSEL} = V_{DDA}	V_{VRC}	 3.0 4.5	 3.6 5.5	V
5	3.3–5.0 V Analog Supply Voltage	V_{DDA}	maximum of 3.0 V or V_{VRC} – 0.1	5.5	V

Table 17. 5V Low Frequency (128 kHz) Internal RC Oscillator

Spec	Characteristic	Symbol	Range	Min	Typ	Max	Unit
1	Frequency before trim[1]	F_{ut128}	35%	83.2	128	172.8	kHz
2	Frequency after loading factory trim[2]	F_{t128}	7%	119.0	128	137.0	kHz
3	Application trim resolution[3]	T_{s128}	—	—	—	±2	%
4	Application frequency trim step[3]	F_{s128}	—	—	4	—	kHz
5	Startup Time	S_{t128}	—	—	—	100	µs

1 Across process, voltage, and temperature.
2 Across voltage and temperature.
3 Fixed voltage and temperature.

4.10 FMPLL Electrical Characteristics

Table 18. FMPLL Electrical Specifications[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	System Frequency[2]	f_{SYS}	—	116	MHz
2	PLL Reference Frequency Range	f_{REF}	4	40	MHz
3	PLL Frequency	f_{PLL}	$\frac{f_{vco(min)}}{(ERFD+1)}$		MHz
4	Loss of Reference Frequency [3]	f_{LOR}	100	2000	kHz
5	Self Clocked Mode Frequency	f_{SCM}	16	64	MHz
6	PLL Lock Time[4]	t_{LPLL}	—	400	µs
7	Duty Cycle of Reference	t_{DC}	40	60	%
8	Frequency un-LOCK Range	f_{UL}	–4.0	4.0	% f_{SYS}
9	Frequency LOCK Range	f_{LCK}	–2.0	2.0	% f_{SYS}
10	CLKOUT Period Jitter,[5] Measured at f_{SYS} Max Cycle-to-cycle Jitter	C_{Jitter}	–5	5	%f_{SYS}
11	CLKOUT Jitter at ≥ 50 µs period	C_{Jitter}	–250	250	ns
12	Peak-to-Peak Frequency Modulation Range Limit [6,7] (f_{SYS}Max must not be exceeded)	C_{mod}	0	4	%f_{SYS}
13	FM Depth Tolerance[8]	C_{mod_err}	–0.50	0.50	%f_{SYS}
14	VCO Frequency[9]	f_{VCO}	192	600	MHz
15	Modulation Rate Limits[10]	f_{MOD}	0.400	1	MHz

1 V_{DDSYN} = 3.0 V to 3.6 V, V_{SS} = V_{SSSYN} = 0 V, T_A = T_L to T_H.

2 The maximum frequency value is with frequency modulation disabled. If frequency modulation is enabled, the maximum frequency value should be de-rated by the percentage of modulation enabled so that the maximum frequency is not exceeded.

3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.

4 This specification applies to the period required for the PLL to re-lock after changing the MFD frequency control bits in the synthesizer control register (SYNCR). From power up with crystal oscillator reference, lock time will be additive with crystal startup time.

5 Values are with frequency modulation disabled. If frequency modulation is enabled, jitter is the sum of C_{jitter} + C_{mod}.

6 Modulation depth selected must not result in f_{PLL} value greater than the f_{PLL} maximum specified value.

7 Maximum and minimum variations from programmed modulation depth are 2%, 3%, and 4% peak-to-peak. Use only these settings.

8 Depth tolerance is the programmed modulation depth ±0.25% of f_{SYS}.

9 See the Block Guide for VCO frequency synthesis equations.

10 Modulation rates less than 400 kHz will result in exceedingly long FM calibration durations. Modulation rates greater than 1 MHz will result in reduced calibration accuracy.

4.11 ADC Electrical Characteristics

Table 19. ADC Conversion Specifications (Operating)

Spec	Characteristic	Symbol	Min	Max	Unit
1	Analog High Reference Voltage	V_{RH}	V_{DDA} – 0.5	V_{DDA}	V
2	Analog Low Reference Voltage	V_{RL}	0	0.5	V
3	Analog Input Voltage	AV_{IN}	V_{RL}	V_{RH}	V
4	Sampling Frequency	F_S	—	1.53	MHz
5	Maximum ADC Clock Frequency	F_{MAX}	—	60	MHz
6	Sampling Time V_{DDA} = 3.0 V – 3.6 V V_{DDA} > 3.6 V – 5.5 V	t_S	 250 125	—	ns
7	Differential Non Linearity	DNL	–1.0	1.0	LSB
8	Integral Non Linearity	INL	–1.5	1.5	LSB
9	Offset Error	OFS	–1.0	1.0	LSB
10	Gain Error	GNE	–2.0	2.0	LSB
11	Total Unadjusted Error [1]	TUE	–2.0	2.0	LSB

1 TUE assumes no pin activity on pins adjacent to analog channel or output driver activity on corresponding V_{DDE} segment.

4.12 Flash Memory Electrical Characteristics

Table 20. Flash Program and Erase Specifications[1]

Spec	Characteristic	Symbol	Min	Initial Max[2]	Max[3]	Unit
1	Double Word (64 bits) Program Time[4]	$t_{dwprogram}$	—	—	500	µs
2	Page (128 bits and 256 bits) Program Time[4]	$t_{pprogram}$	—	160	500	µs
3	16 KB Block Pre-program and Erase Time	$t_{16kpperase}$	—	1000	5000	ms
4	64 KB Block Pre-program and Erase Time	$t_{64kpperase}$	—	1800	5000	ms
5	128 KB Block Pre-program and Erase Time	$t_{128kpperase}$	—	2600	7500	ms

4.14 AC Timing

4.14.1 Reset and Boot Configuration Pins

Table 24. Reset and Boot Configuration Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	$\overline{\text{RESET}}$ Pulse Width	t_{RPW}	150	—	ns
2	BOOTCFG Setup Time after $\overline{\text{RESET}}$ Valid	t_{RCSU}	—	100	µs
3	BOOTCFG Hold Time from $\overline{\text{RESET}}$ Valid	t_{RCH}	0	—	µs

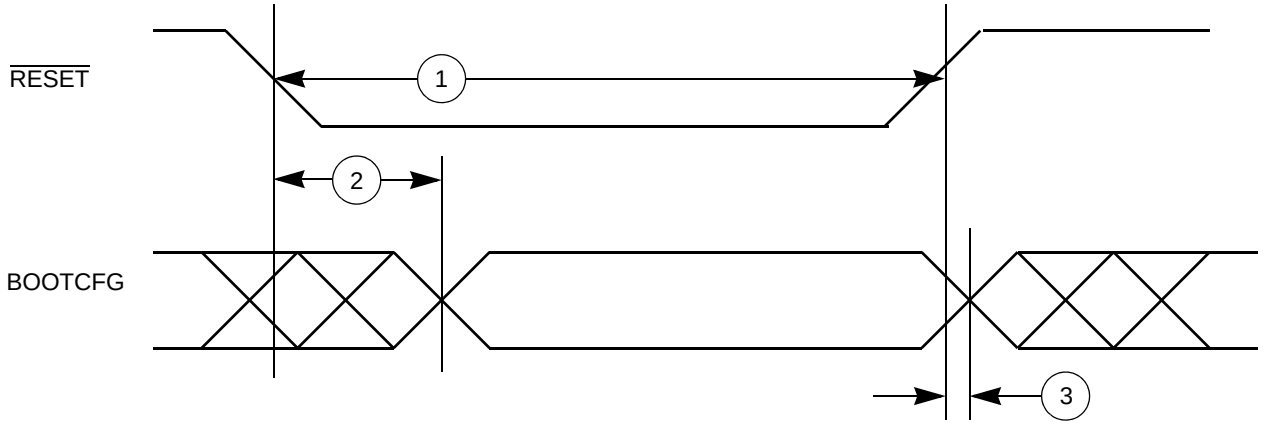


Figure 7. Reset and Boot Configuration Timing

4.14.2 External Interrupt (IRQ) and Non-Maskable Interrupt (NMI) Pins

Table 25. IRQ/NMI Timing

Spec	Characteristic	Symbol	Min	Max	Unit
1	IRQ/NMI Pulse Width Low	t_{IPWL}	3	—	t_{SYS}
2	IRQ/NMI Pulse Width High	T_{IPWH}	3	—	t_{SYS}
3	IRQ/NMI Edge to Edge Time[1]	t_{ICYC}	6	—	t_{SYS}

[1] Applies when IRQ/NMI pins are configured for rising edge or falling edge events, but not both.

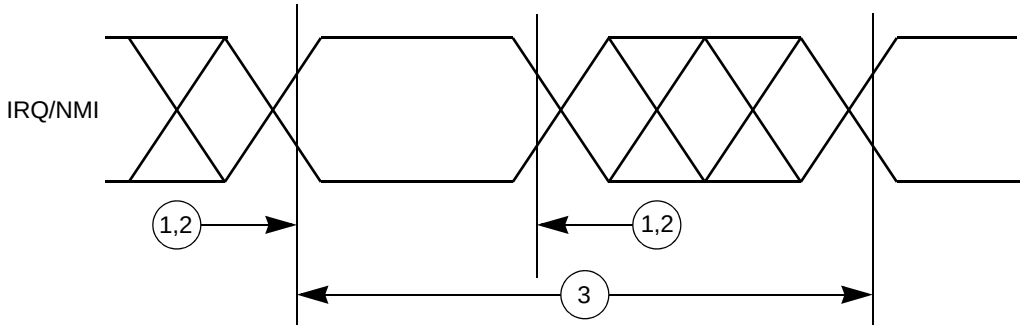


Figure 8. IRQ and NMI Timing

4.14.3 JTAG (IEEE 1149.1) Interface

Table 26. JTAG Interface Timing[1]

Spec	Characteristic	Symbol	Min	Max	Unit
1	TCK Cycle Time	t_{JCYC}	100	—	ns
2	TCK Clock Pulse Width (Measured at $V_{DDE}/2$)	t_{JDC}	40	60	ns
3	TCK Rise and Fall Times (40% – 70%)	$t_{TCKRISE}$	—	3	ns
4	TMS, TDI Data Setup Time	t_{TMSS}, t_{TDIS}	5	—	ns
5	TMS, TDI Data Hold Time	t_{TMSH}, t_{TDIH}	25	—	ns
6	TCK Low to TDO Data Valid	t_{TDOV}	—	25	ns
7	TCK Low to TDO Data Invalid	t_{TDOI}	0	—	ns
8	TCK Low to TDO High Impedance	t_{TDOHZ}	—	20	ns
9	JCOMP Assertion Time	t_{JCMPPW}	100	—	ns
10	JCOMP Setup Time to TCK Low	t_{JCMPS}	40	—	ns
11	TCK Falling Edge to Output Valid	t_{BSDV}	—	50	ns
12	TCK Falling Edge to Output Valid out of High Impedance	t_{BSDVZ}	—	50	ns
13	TCK Falling Edge to Output High Impedance	t_{BSDHZ}	—	50	ns
14	Boundary Scan Input Valid to TCK Rising Edge	t_{BSDST}	50	—	ns
15	TCK Rising Edge to Boundary Scan Input Invalid	t_{BSDHT}	50	—	ns

1 These specifications apply to JTAG boundary scan only. JTAG timing specified at V_{DDE} = 3.0 – 5.5 V, $T_A = T_L$ to T_H, and C_L = 30 pF with SRC = 0b11.

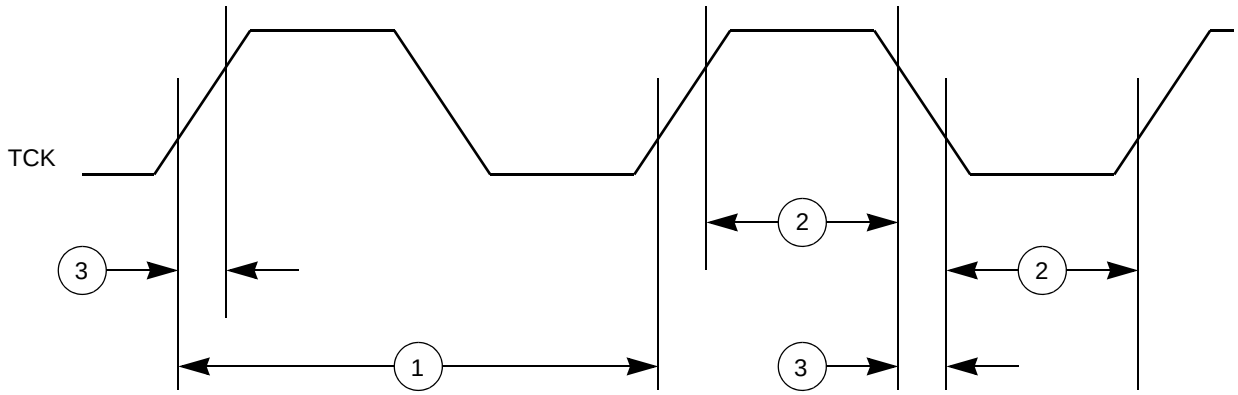


Figure 9. JTAG Test Clock Input Timing

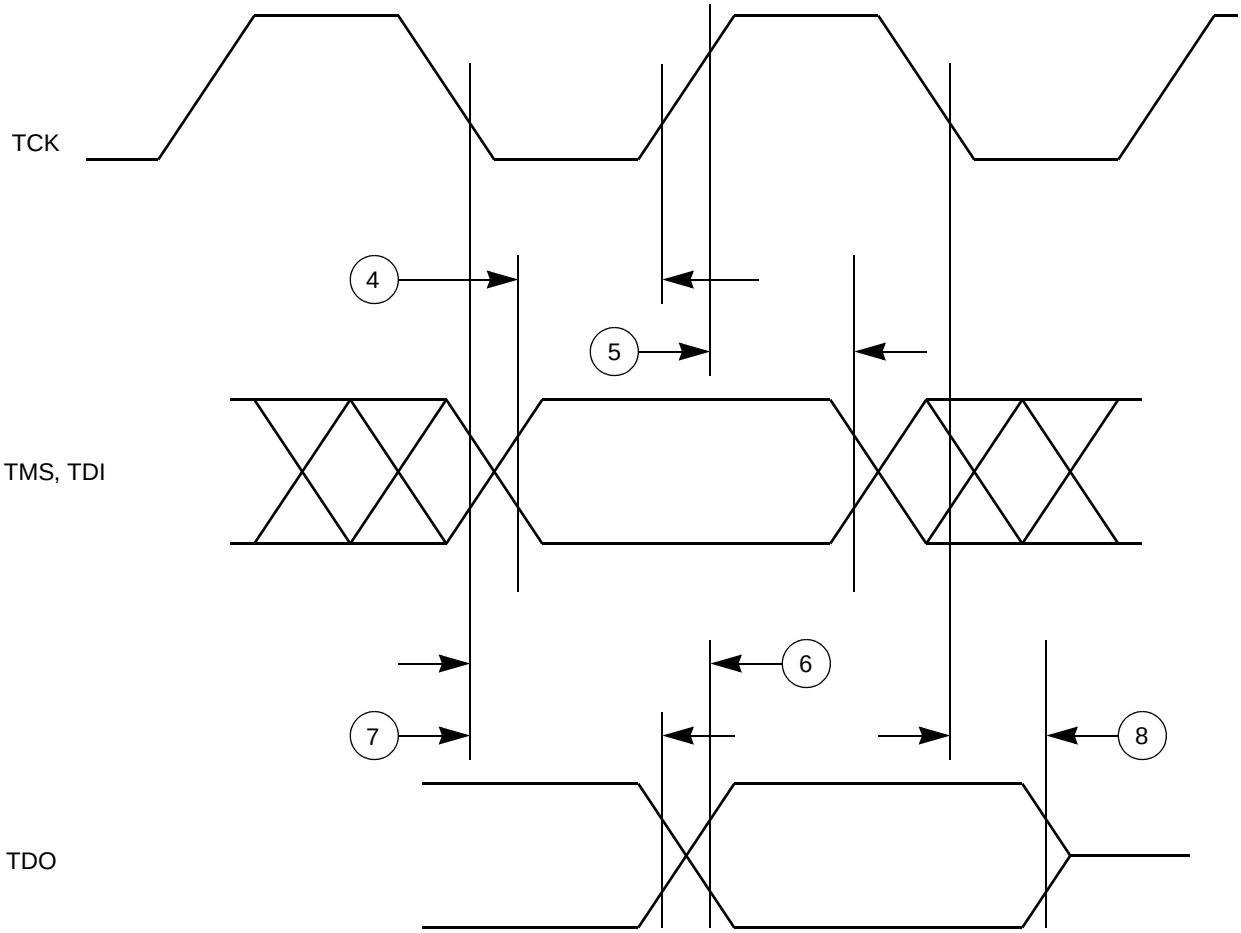


Figure 10. JTAG Test Access Port Timing

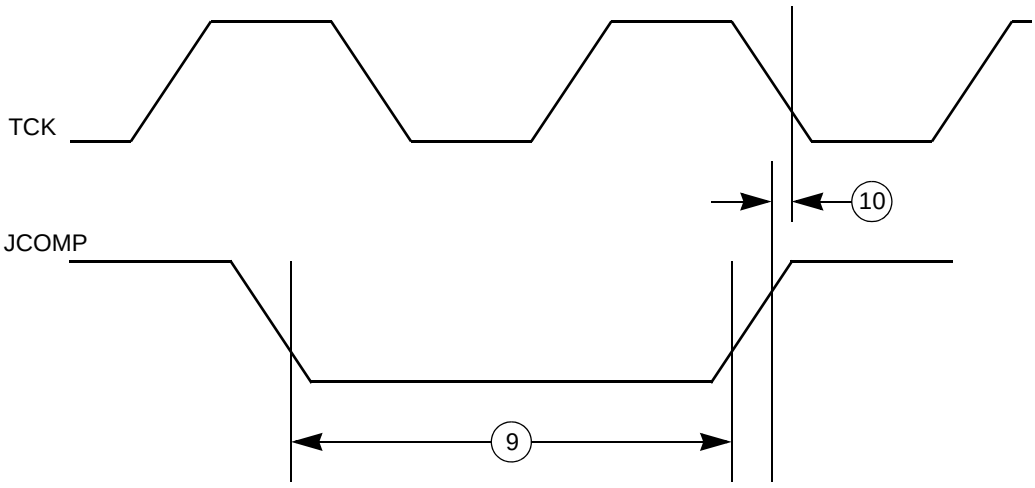


Figure 11. JTAG JCOMP Timing

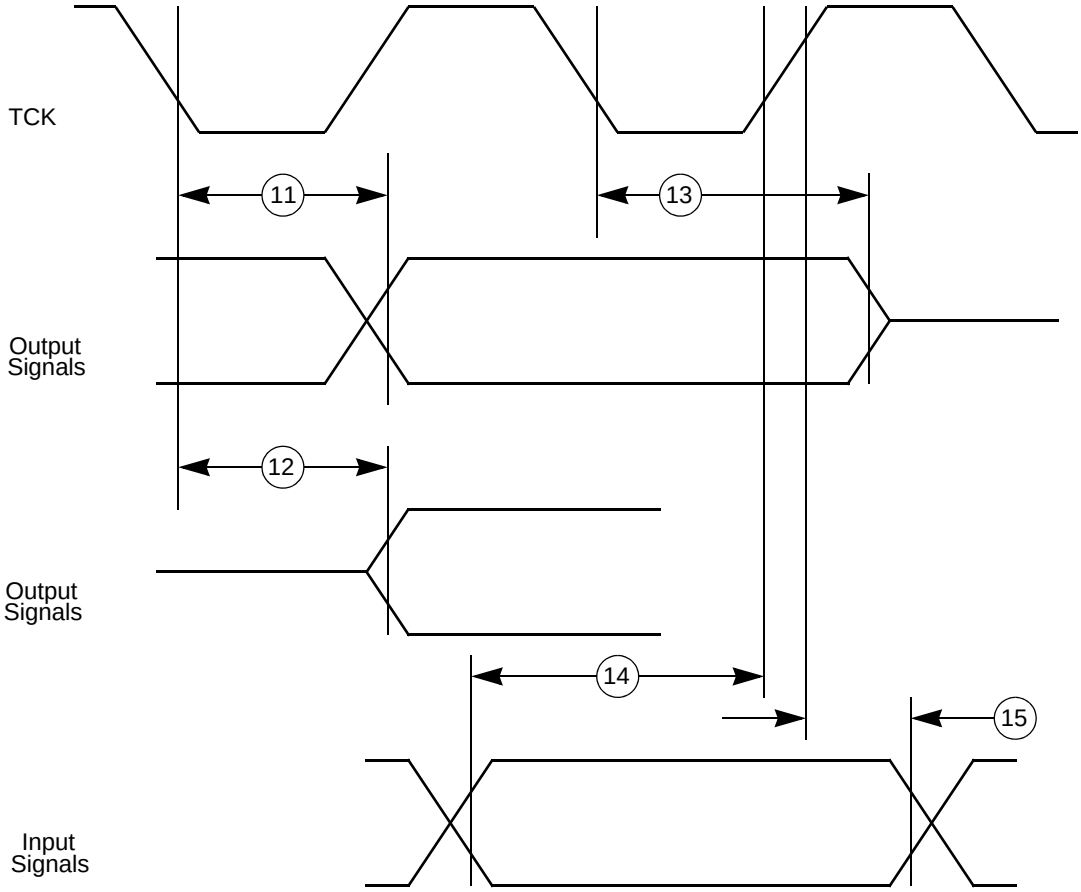


Figure 12. JTAG Boundary Scan Timing

4.14.6 Deserial Serial Peripheral Interface (DSPI)

Table 29. DSPI Timing

Spec	Characteristic	Symbol	116 MHz[1]		Unit
			Min. Value	Max. Value	
1	DSPI Cycle Time Master (MTFE = 0) Slave (MTFE = 0) Master (MTFE = 1) Slave (MTFE = 1)	t_{SCK}	 100 100 50 50	 — — — —	 ns ns ns ns
2	PCS to SCK Delay[2]	t_{CSC}	7	—	ns
3	After SCK Delay[3]	t_{ASC}	14	—	ns
4	SCK Duty Cycle	t_{SDC}	$0.4 \times t_{SCK}$	$0.6 \times t_{SCK}$	ns
5	Slave Access Time ($\overline{SS}$ active to SOUT valid)	t_A	—	25	ns
6	Slave SOUT Disable Time ($\overline{SS}$ inactive to SOUT High-Z or invalid)	t_{DIS}	—	25	ns
7	PCSx to $\overline{PCSS}$ time	t_{PCSC}	0	—	ns
8	$\overline{PCSS}$ to PCSx time	t_{PASC}	0	—	ns
9	Data Setup Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[4] Master (MTFE = 1, CPHA = 1)	t_{SUI}	 25 5 10 25	 — — — —	 ns ns ns ns
10	Data Hold Time for Inputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0)[4] Master (MTFE = 1, CPHA = 1)	t_{HI}	 –4 7 12 –4	 — — — —	 ns ns ns ns
11	Data Valid (after SCK edge) Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{SUO}	 — — — —	 8 28 15 8	 ns ns ns ns
12	Data Hold Time for Outputs Master (MTFE = 0) Slave Master (MTFE = 1, CPHA = 0) Master (MTFE = 1, CPHA = 1)	t_{HO}	 –7 2 1 –7	 — — — —	 ns ns ns ns

1 116 MHz timing specified at CL = 50 pF with SRC = 0b11.

2 The maximum value is programmable in DSPI_CTAR*n*[PSSCK] and DSPI_CTAR*n*[CSSCK].

3 The maximum value is programmable in DSPI_CTAR*n*[PASC] and DSPI_CTAR*n*[ASC].

4 This number is calculated assuming the SMPL_PT bit field in DSPI_MCR is set to 0b10.

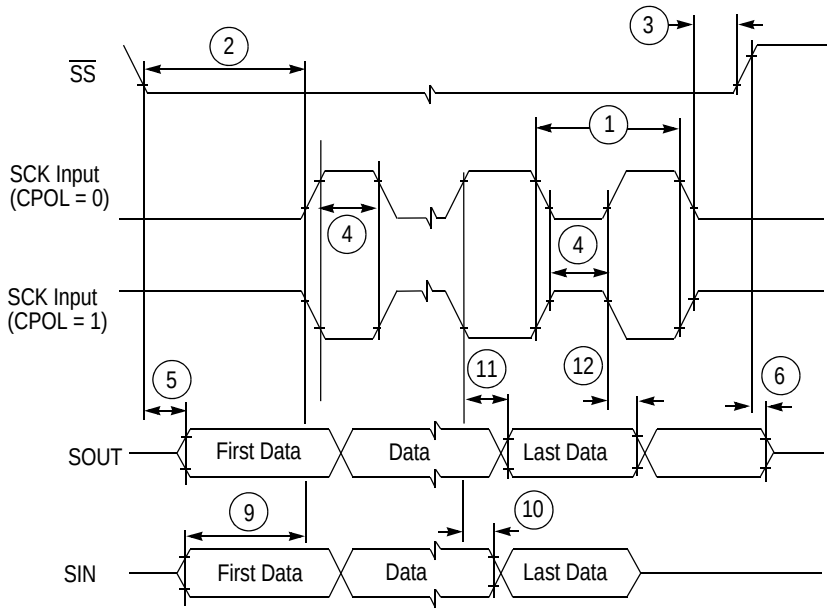


Figure 22. DSPI Modified Transfer Format Timing — Slave, CPHA = 0

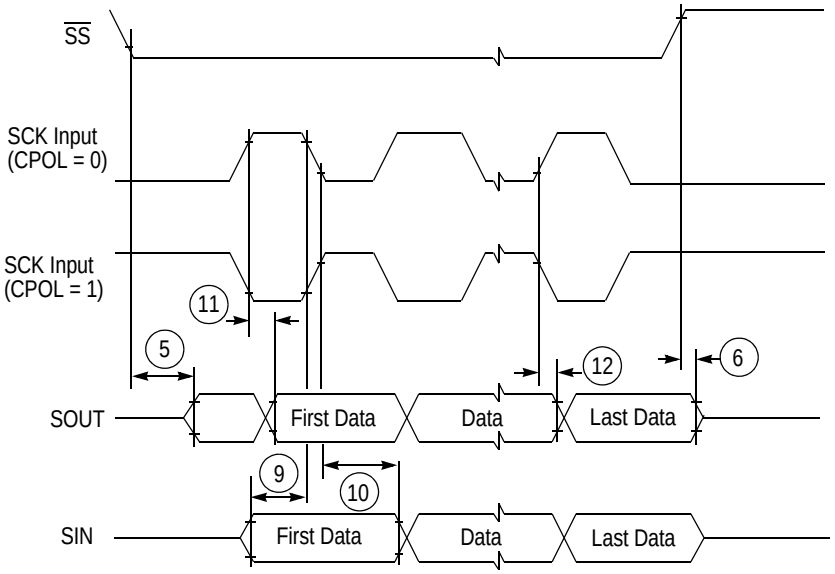


Figure 23. DSPI Modified Transfer Format Timing — Slave, CPHA = 1

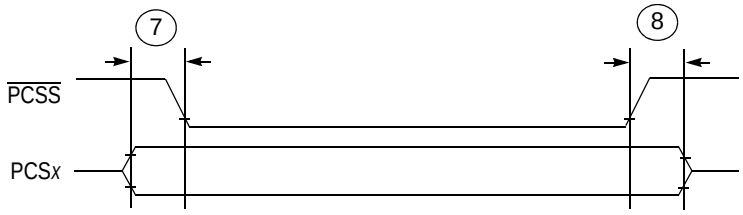


Figure 24. DSPI PCS Strobe (PCSS) Timing

1 The Controller can shut off MLBCLK to place MLB in a low-power state.

2 Pulse width variation is measured at 1.25 V by triggering on one edge of MLBCLK and measuring the spread on the other edge, measured in ns peak-to-peak (ns p-p).

3 The board must be designed to insure that the high-impedance bus does not leave the logic state of the final driven bit for this time period. Therefore, coupling must be minimized while meeting the maximum capacitive load listed.

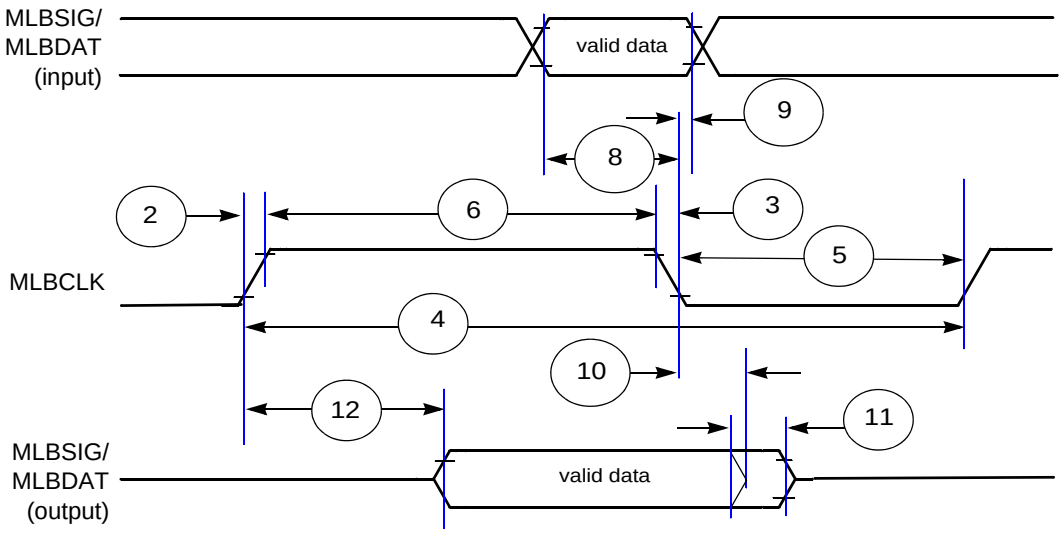


Figure 25. Media Local Bus (MLB) Timing

4.14.8 Fast Ethernet Interface

MII signals use CMOS signal levels compatible with devices operating at either 5.0 V or 3.3 V. Signals are not TTL compatible. They follow the CMOS electrical characteristics.

4.14.8.1 MII Receive Signal Timing (RXD[3:0], RX_DV, RX_ER, and RX_CLK)

The receiver functions correctly up to a RX_CLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the system clock frequency must exceed four times the RX_CLK frequency.

Table 33. MII Receive Signal Timing

Spec	Characteristic	Min	Max	Unit
M1	RXD[3:0], RX_DV, RX_ER to RX_CLK setup	5	—	ns
M2	RX_CLK to RXD[3:0], RX_DV, RX_ER hold	5	—	ns
M3	RX_CLK pulse width high	35%	65%	RX_CLK period
M4	RX_CLK pulse width low	35%	65%	RX_CLK period

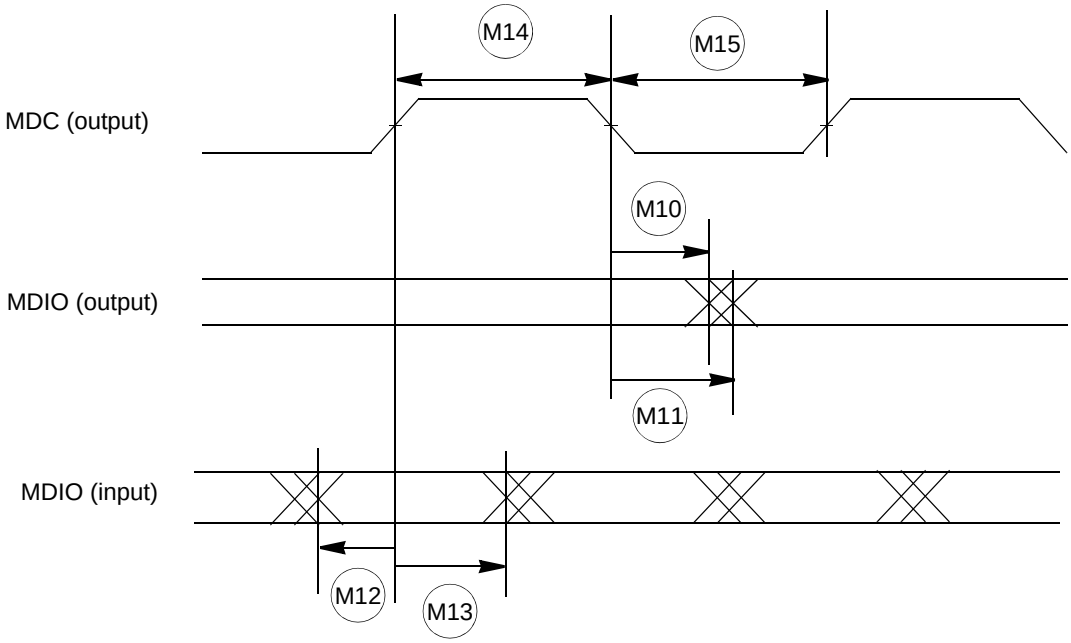


Figure 29. MII Serial Management Channel Timing Diagram

6 Revision History

Table 37 describes the changes made to this document between revisions.

Table 37. Revision History

Revision	Date	Description
0	April 2008	Preliminary release.
1	June 2008	Initial release: Advance Information.
2	Jan 2009	Release: Advance Information.
3	September 2009	Release: Advance Information, interim updates.
4	January 2011	Release: Technical Data, interim updates.
5	January 2011	Release: Technical Data, interim updates.
6	March 2011	Release: Technical Data, interim updates.