Analog Devices Inc./Maxim Integrated - MAXQ305X-0000+ Datasheet

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	-
Core Size	16-Bit
Speed	12MHz
Connectivity	SPI, UART/USART
Peripherals	Brown-out Detect/Reset, Infrared, Power-Fail, POR, WDT
Number of I/O	32
Program Memory Size	80KB (80K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	2K x 8
Voltage - Supply (Vcc/Vdd)	0.9V ~ 3.6V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	Die
Supplier Device Package	Diesale
Purchase URL	https://www.e-xfl.com/product-detail/analog-devices/maxq305x-0000

ABSOLUTE MAXIMUM RATINGS

Voltage Range of V_{DD} with Respect to GND .....-0.3V to +3.6V
Voltage Range on Any Lead
with Respect to GND except V_{DD}..... -0.3V to (V_{DD} + 0.5V)
Continuous Power Dissipation (T_A = +70°C)
TQFN (derate 37mW/°C above +70°C).....2963mW

Operating Temperature Range ..... -20°C to +70°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (TQFN only, reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

PACKAGE THERMAL CHARACTERISTICS (Note 1)

TQFN
Junction-to-Ambient Thermal Resistance (θ_{JA}).....27°C/W
Junction-to-Case Thermal Resistance (θ_{JC}).....1°C/W

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

RECOMMENDED OPERATING CONDITIONS

(V_{DD} = $V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = -20°C to +70°C, typical T_A = +25°C, $V_{DD(TYP)}$, unless otherwise noted. Specifications to T_A = -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	V_{DD}		V_{RST}	1.5	3.6	V
Supply Voltage (High Voltage Mode)	V_{DD_HV}	HVREN = HVRMD = 1	1.2			V
Supply Voltage (Performance Mode)	V_{DD_PFM}	HVREN = HVRMD = PFMSEL = 1, f_{SYSCLK} = f_{HFXIN} = 12MHz	1.2			V
Regulator Output	V_{REGOUT_1}	HVRMD = 0	1.26	1.4	1.54	V
	V_{REGOUT_2}	HVRMD = 1		1.8		
Power-Fail Warning Voltage for Supply (Note 2)	V_{PFW}	Monitors V_{DD}	0.95	1.0	1.05	V
Power-Fail Reset Voltage	V_{RST}	Monitors V_{DD}	0.9	0.925	0.95	V
Power-On Reset Voltage	V_{POR}	Monitors V_{DD}		0.8		V
RAM Data-Retention Voltage	V_{DRV}	(Note 3)	0.7			V
Active Current	I_{DD_1}	Source clock = 12MHz, Sysclk = 4MHz (green mode), HVREN = HVRMD = PFMSEL = 0 (Note 4)		1.36		mA
Active Current	I_{DD_2}	Source clock = 12MHz, Sysclk = 4MHz (green mode), HVREN = HVRMD = PFMSEL = 0 (Note 4)		10		mA
Active Current During Flash Programming	I_{DD_FP}	V_{DD} = V_{RST} to 1.0V, f_{SYSCLK} = 4MHz, HVREN = HVRMD = PFMSEL = 0		10		mA

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = $V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = -20°C to +70°C, typical T_A = +25°C, $V_{DD(TYP)}$, unless otherwise noted. Specifications to T_A = -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Stop Mode Current	I_{STOP1}	Power-fail off, T_A = +25°C		0.4	3.5	µA
		Power-fail off, T_A = 0 to +70°C		0.4	12	
	I_{STOP2}	Power-fail on, T_A = +25°C		22		
		Power-fail on, T_A = 0 to +70°C		22		
Current Consumption During Power-Fail	I_{PFR}	(Note 5)		$((3 \times I_{STOP2}) + ((PCI - 3) \times (I_{STOP1} + I_{NANO})))/PCI$		µA
Power Consumption During Power-On Reset	I_{POR}	(Note 6)		100		nA
Stop-Mode Resume Time (Note 7)	t_{ON}	$V_{DD} \geq 1.5V$		375		µs
		$V_{DD} < 1.5V$		550		
Power-Fail Monitor Startup Time	t_{PFM_ON}			150		µs
Power-Fail Warning Detection Time	t_{PFW}	(Note 8)		10		µs
Input Low Voltage for IRTX, IRRX, HFXIN, $\overline{RESET}$, and All Port Pins	V_{IL}		V_{GND}		0.3 x V_{DD}	V
Input High Voltage for IRTX, IRRX, HFXIN, $\overline{RESET}$, and All Port Pins	V_{IH}		0.7 x V_{DD}		V_{DD}	V
Input Hysteresis (Schmitt)	V_{IHYS}	$V_{DD} \geq 1.5V$		300		mV
		$V_{DD} < 1.5V$		50		
IRRX Input Filter Pulse-Width Reject	t_{IRRX_R}				50	ns
IRRX Input Filter Pulse-Width Accept	t_{IRRX_A}		300			ns
Output Low Voltage for $\overline{RESET}$ and All Port Pins (Note 9)	V_{OL}	V_{DD} = 3.6V, I_{OL} = 11mA		0.4	0.5	V
		V_{DD} = 2.35V, I_{OL} = 8mA		0.4	0.5	V
		V_{DD} = 1.85V, I_{OL} = 4.5mA		0.4	0.5	V
		V_{DD} = 0.9V, I_{OL} = 20µA		0.1	0.15	V
Output High Voltage for $\overline{RESET}$ and All Port Pins (Note 9)	V_{OH}	V_{DD} = 1.62V to 3.6V, I_{OH} = 2mA	V_{DD} - 0.5		V_{DD}	V
		V_{DD} = 0.9V, I_{OH} = 20µA	V_{DD} - 0.15		V_{DD}	
IRTX Reference Current	I_{IRTX}	Constant used to calculate IRTX drive		100		mA
LED Reference Current	I_{LED}	Constant used to calculate LED[1:0] drive		5		mA

RECOMMENDED OPERATING CONDITIONS (continued)

(V_{DD} = $V_{DD(MIN)}$ to $V_{DD(MAX)}$, T_A = -20°C to +70°C, typical T_A = +25°C, $V_{DD(TYP)}$, unless otherwise noted. Specifications to T_A = -20°C are guaranteed by design and are not production tested.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
IR						
Carrier Frequency	f_{IRX}	External crystal			$f_{HFXIN}/2$	Hz
	f_{IRC}	External clock			$f_{XCLK}/2$	
IR Transmission Rate	f_{IR_RATE}	IRIOCN.IRRATE = 0		1		MHz

Note 2: The VPFW level can be programmed to one of a range of trip points as defined by PWCN.PFWARNCN[1:0]. The values listed in the *Recommended Operating Conditions* table are for the default configuration of 1.0V (nominal) ±5%.

Note 3: Guaranteed by design, not production tested.

Note 4: Measured on the V_{DD} pin with the device not in reset. All inputs are tied to GND or V_{DD}. Outputs do not source/sink any current. Part is executing code from flash memory.

Note 5: The power check interval (PCI) can be set to check once every 1024, 2048, or 4096 nano-ring clock cycles. If the PCI is set to check every clock cycle, then this value will be equal to I_{STOP} The power check interval (PCI) can be set to always on, 1024, 2048, or 4096 nano-ring clock cycles.

Note 6: Current consumption during POR when powering up while V_{DD} is less than the POR release voltage.

Note 7: After typical startup time, and before the completion of an 8192 t_{HFXIN} crystal warmup period, the microcontroller runs off of a 1MHz ring oscillator.

Note 8: The minimum amount of time that V_{DD} must be below V_{PFW} before a power-fail event is detected; refer to the user's guide for detailed information.

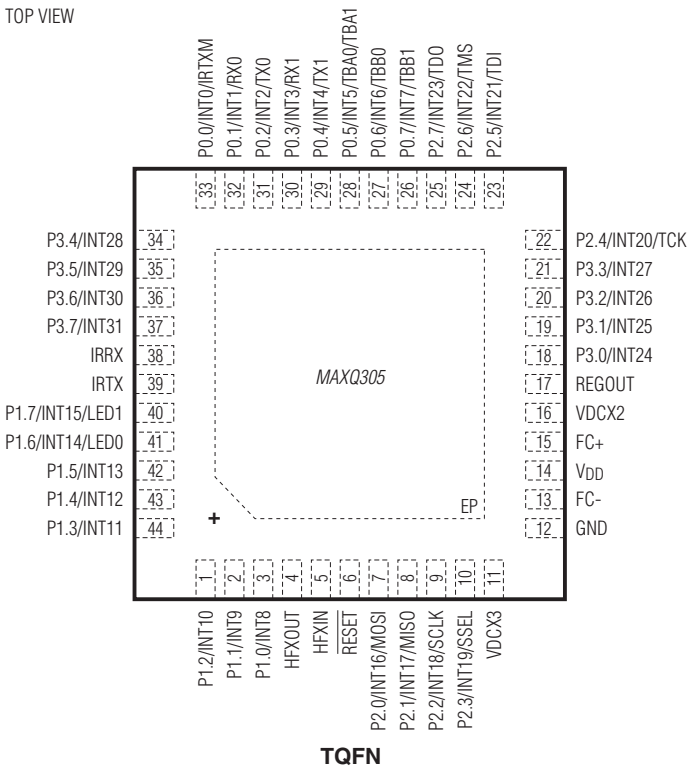
Note 9: The maximum total current, $I_{OH(MAX)}$ and $I_{OL(MAX)}$, for all listed outputs combined, should not exceed 32mA to satisfy the maximum specified voltage drop. This does not include the IRTX or LED outputs.

Note 10: Do not write to flash memory while $V_{DD} < V_{DD\_HV(MIN)}$. The flash memory write functions in the utility ROM attempt to enable the high voltage mode if not already enabled, and return an error code if $V_{DD} < V_{DD\_HV(MIN)}$.

Note 11: Programming time does not include overhead associated with utility ROM interface.

Low-Voltage Microcontroller with Infrared Module

Pin Configuration



TQFN

Pin Description

PIN		NAME	FUNCTION
BARE DIE	TQFN		
POWER PINS			
16	14	V_{DD}	**Supply Voltage.**
14	12	GND	**Ground**. Connect directly to the ground plane.
5, 31	EP	GND	**Ground–Exposed Pad**. The exposed pad is found only on the TQFN packages. It should be connected directly to the ground plane.
19	17	REGOUT	**Internal Regulator Output**. This pin must be connected to ground through a 1.0µF external ceramic chip capacitor. The capacitor must be placed as close to this pin as possible. No devices other than the capacitor should be connected to this pin.
17	15	FC+	**2x Charge-Pump Capacitor Pins**. Connect a 270nF external capacitor between FC+ and FC-.
15	13	FC-	

Pin Description (continued)

PIN		NAME	FUNCTION
BARE DIE	TQFN		
18	16	VDCX2	**2x Charge-Pump Output**. Connect a 4.7µF external capacitor between this pin and ground. No devices other than the capacitor should be connected to this pin, except for functional circuitry related to LED0, LED1, IRTX drive and IRRX input.
13	11	VDCX3	**3x Charge-Pump Output.** Connect a 2nF external capacitor between this pin and ground. No devices other than the capacitor should be connected to this pin.
8	6	$\overline{\text{RESET}}$	**Digital, Active-Low, Reset Input/Output**. The MAXQ305 remains in reset as long as this pin is low and begins executing from the Utility ROM at address 8000h when this pin returns to a high state. This pin includes a pullup current source; if this pin is driven by an external device, it should be driven by an open-drain source capable of sinking in excess of 4mA. This pin may be left unconnected if there is no need to place the MAXQ305 in a reset state using an external signal. This pin is driven low as an output when an internal reset condition occurs.
6	4	HFXOUT	**High-Frequency Crystal Input Pins**. Connect an external crystal or resonator between HFXIN and HFXOUT for use as the high-frequency system clock source. Alternatively, connect HFXOUT to ground when an external, high-frequency clock source is connected to the HFXIN pin.
7	5	HFXIN	
IR FUNCTION PINS			
44	38	IRRX	**IR Receive Input**. IR receiver pin.
45	39	IRTX	**IR Transmit Output**. Active-low IR transmit pin. This pin defaults to a high-impedance input with the weak pullup disabled during all forms of reset. Software must configure this pin after release from reset to remove the high-impedance input condition.

Pin Description (continued)

PIN		NAME	FUNCTION	
BARE DIE	TQFN			
GENERAL-PURPOSE I/O AND SPECIAL FUNCTION PINS				
			Port 0 General-Purpose Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD0, PO0, and PI0 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used.	
			GPIO PORT PIN	**SPECIAL FUNCTIONS**
39	33	P0.0/INT0/IRTXM	P0.0	INT0/IR Modulator Output
38	32	P0.1/INT1/RX0	P0.1	INT1/USART 0 Receive
37	31	P0.2/INT2/TX0	P0.2	INT2/USART 0 Transmit
35	30	P0.3/INT3/RX1	P0.3	INT3/USART 1 Receive
33	29	P0.4/INT4/TX1	P0.4	INT4/USART 1 Transmit
32	28	P0.5/INT5/TBA0/TBA1	P0.5	INT5/Type B Timer 0 Pin A or Type B Timer 1 Pin A
30	27	P0.6/INT6/TBB0	P0.6	INT6/Type B Timer 0 Pin B
29	26	P0.7/INT7/TBB1	P0.7	INT7/Type B Timer 1 Pin B
			Port 1 General-Purpose Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD1, PO1, and PI1 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used (Note that P1.6 and P1.7 do not support the weak pullup mode).	
			GPIO PORT PIN	**SPECIAL FUNCTIONS**
1	44	P1.3/INT11	P1.3	INT11
2	1	P1.2/INT10	P1.2	INT10
3	2	P1.1/INT9	P1.1	INT9
4	3	P1.0/INT8	P1.0	INT8
46	40	P1.7/INT15/LED1	P1.7 (No weak pullup mode)	INT15/LED1 Output
47	41	P1.6/INT14/LED0	P1.6 (No weak pullup mode)	INT14/LED0 Output
48	42	P1.5/INT13	P1.5	INT13
49	43	P1.4 / INT12	P1.4	INT12

Pin Description (continued)

PIN		NAME	FUNCTION	
BARE DIE	TQFN			
			Port 2 General-Purpose Digital I/O Pins. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD2, PO2 and PI2 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All special functions must be enabled from software before they can be used.	
			GPIO PORT PIN	**SPECIAL FUNCTION**
9	7	P2.0/INT16/MOSI	P2.0	INT16/SPI Master Out Slave In
10	8	P2.1/INT17/MISO	P2.1	INT17/SPI Master In Slave Out
11	9	P2.2/INT18/SCLK	P2.2	INT18/SPI Clock
12	10	P2.3/INT19/SSEL	P2.3	INT19/SPI Slave Select
24	22	P2.4/INT20/TCK	P2.4	INT20/JTAG Test Clock
25	23	P2.5/INT21/TDI	P2.5	INT21/JTAG Test Data In
27	24	P2.6/INT22/TMS	P2.6	INT22/JTAG Test Mode Select
28	25	P2.7/INT23/TDO	P2.7	INT23/JTAG Test Data Out
			Port 3 General-Purpose Digital I/O Pins with Interrupt Capability. These port pins function as general-purpose I/O pins with their input and output states controlled by the PD3, PO3 and PI3 registers. All port pins default to high-impedance mode after a reset. Software must configure these pins after release from reset to remove the high-impedance condition. All external interrupts must be enabled from software before they can be used.	
			GPIO PORT PIN	**EXTERNAL INTERRUPT**
20	18	P3.0/INT24	P3.0	INT24
21	19	P3.1/INT25	P3.1	INT25
22	20	P3.2/INT26	P3.2	INT26
23	21	P3.3/INT27	P3.3	INT27
26, 34, 36	—	N.C.	No Connection.	
40	34	P3.4/INT28	P3.4	INT28
41	35	P3.5/INT29	P3.5	INT29
42	36	P3.6/INT30	P3.6	INT30
43	37	P3.7/INT31	P3.7	INT31

the beginning of user application code in program flash memory.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming or in-circuit debugging functions is prohibited until a password has been supplied. Three different password locks are provided, each of which can be used to protect a different area of memory (system memory, user loader and user application). Each password lock is controlled by a 16-word area of flash memory; if the password is set to all FFFFh values or all 0000h values, the password is disabled. Otherwise, the password is active and must be matched by the user of the bootloader or debugger before access is granted to the corresponding area of flash program memory. Refer to the *MAXQ305 User's Guide* for more details.

Watchdog Timer

The internal watchdog timer greatly increases system reliability. The timer resets the device if software execution is disturbed. The watchdog timer is a free-running counter designed to be periodically reset by the application software. If software is operating correctly, the counter is periodically reset and never reaches its maximum count. However, if software operation is interrupted, the timer does not reset, triggering a system reset and optionally a watchdog timer interrupt. This protects the system against electrical noise or electrostatic discharge (ESD) upsets that could cause uncontrolled processor operation. The internal watchdog timer is an upgrade to older designs with external watchdog devices, reducing system cost and simultaneously increasing reliability.

The watchdog timer functions as the source of both the watchdog timer timeout and the watchdog timer reset. The timeout period can be programmed in a range of 2^{15} to 2^{24} system clock cycles. An interrupt is generated when the timeout period expires if the interrupt is enabled. All watchdog timer resets follow the programmed interrupt timeouts by 512 system clock cycles. If the watchdog timer is not restarted for another full interval in this time period, a system reset occurs when the reset timeout expires. See Table 2.

IR Carrier Generation and Modulation Timer

The dedicated IR timer/counter module simplifies low-speed infrared (IR) communication. The IR timer implements two pins (IRTX and IRRX) for supporting IR transmit and receive, respectively. The IRTX pin has no corresponding port pin designation, so the standard PD, PO, and PI port control status bits are not present. However, the IRTX pin output can be manipulated high or low using the PWCN.IRTXOUT and PWCN.IRTXOE bits when the IR timer is not enabled (i.e., IREN = 0).

The IR timer is composed of a carrier generator and a carrier modulator. The carrier generation module uses the 16-bit IR carrier register (IRCA) to define the high and low time of the carrier through the IR carrier high byte (IRCAH) and IR carrier low byte (IRCAL). The carrier modulator uses the IR data bit (IRDATA) and IR modulator time register (IRMT) to determine whether the carrier or the idle condition is present on IRTX.

The IR timer is enabled when the IR enable bit (IREN) is set to 1. The IR Value register (IRV) defines the beginning value for the carrier modulator. During transmission, the IRV register is initially loaded with the IRMT value and begins down counting towards 0000h, whereas in receive mode it counts upward from the initial IRV register value. During the receive operation, the IRV register can be configured to reload with 0000h when capture occurs on detection of selected edges or can be allowed to continue free-running throughout the receive operation. An overflow occurs when the IR timer value rolls over from 0FFFFh to 0000h. The IR overflow flag (IROV) is set to 1 and an interrupt is generated if enabled (IRIE = 1).

Table 2. Watchdog Interrupt Timeout

WD[1:0]	WATCHDOG CLOCK	WATCHDOG INTERRUPT TIMEOUT	WATCHDOG RESET AFTER WATCHDOG INTERRUPT (µs)
00	Sysclk/2^{15}	2.7ms	42.7
01	Sysclk/2^{18}	21.9ms	42.7
10	Sysclk/2^{21}	174.7ms	42.7
11	Sysclk/2^{24}	1.4s	42.7

Carrier Generation Module

The IRCAH byte defines the carrier high time in terms of the number of IR input clocks, whereas the IRCAL byte defines the carrier low time.

- IR Input Clock (f_{IRCLK}) = $f_{SYS}/2^{IRDIV[1:0]}$
- Carrier Frequency (fCARRIER) = fIRCLK/(IRCAH + IRCAL + 2)
- Carrier High Time = IRCAH + 1
- Carrier Low Time = IRCAL + 1
- Carrier Duty Cycle = (IRCAH + 1)/(IRCAH + IRCAL + 2)

During transmission, the IRCA register is latched for each IRV down-count interval, and is sampled along with the IRTXPOL and IRDATA bits at the beginning of each new IRV down-count interval so that duty-cycle variation and frequency shifting is possible from one interval to the next, which is illustrated in Figure 2.

Figure 3 illustrates the basic carrier generation and its path to the IRTX output pin. The IR transmit polarity bit (IRTXPOL) defines the starting/idle state and the carrier polarity of the IRTX pin when the IR timer is enabled.

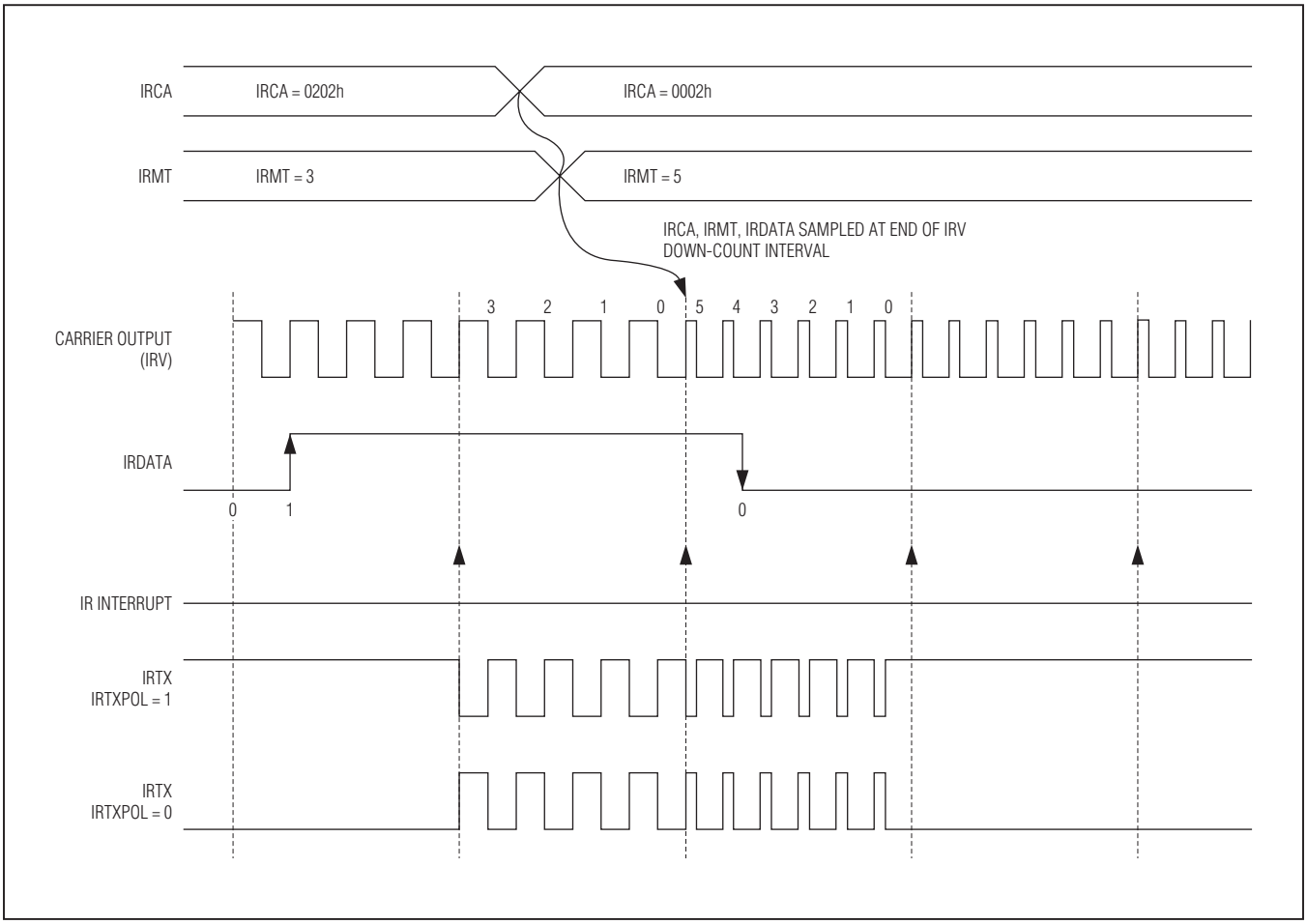


Figure 2. IR Transmit Frequency Shifting Example (IRCFME=0)

IR Transmission

During IR transmission (IRMODE = 1), the carrier generator creates the appropriate carrier waveform, while the carrier modulator performs the modulation. The carrier modulation can be performed as a function of carrier cycles or IRCLK cycles dependent on the setting of the IRCFME bit. When IRCFME = 0, the IRV down counter is clocked by the carrier frequency and thus the modulation is a function of carrier cycles. When IRCFME = 1, the IRV down counter is clocked by IRCLK, allowing carrier modulation timing with IRCLK resolution.

The IRTXPOL bit defines the starting/idle state as well as the carrier polarity for the IRTX pin. If IRTXPOL = 1, the IRTX pin is set to a logic-high when the IR timer module is enabled. If IRTXPOL = 0, the IRTX pin is set to a logic-low when the IR timer is enabled.

A separate register bit, IR data (IRDATA), is used to determine whether the carrier generator output is output to the IRTX pin for the next IRMT carrier cycles. When IRDATA = 1, the carrier waveform (or inversion of this waveform if IRTXPOL = 1) is output on the IRTX pin during the next IRMT cycles. When IRDATA = 0, the idle condition, as defined by IRTXPOL, is output on the IRTX pin during the next IRMT cycles.

The IR timer acts as a down counter in transmit mode. An IR transmission starts when the IREN bit is set to 1 when IRMODE = 1; when the IRMODE bit is set to 1 when IREN = 1; or when IREN and IRMODE are both set to 1 in the same instruction. The IRMT and IRCA registers, along with the IRDATA and IRTXPOL bits, are sampled at the beginning of the transmit process and every time the IR timer value reloads its value. When the IRV reaches 0000h value, on the next carrier clock, it does the following:

1) Reloads IRV with IRMT.
2) Samples IRCA, IRDATA, and IRTXPOL.
3) Generates IRTX accordingly.
4) Sets IRIF to 1.
5) Generates an interrupt to the CPU if enabled (IRIE = 1).

To terminate the current transmission, the user can switch to receive mode (IRMODE = 0) or clear IREN to 0.

Carrier Modulation Time = IRMT + 1 carrier cycles

IR Transmit—Independent External Carrier and Modulator Outputs

The normal transmit mode modulates the carrier based upon the IRDATA bit. However, the user has the option to input the modulator (envelope) on an external pin if desired. If the IRENV[1:0] bits are configured to 01b or 10b, the modulator/envelope is output to the IRTXM pin. The IRDATA bit is output directly to the IRTXM pin (if IRTXPOL = 0) on each IRV down-count interval boundary just as if it were being used to internally modulate the carrier frequency. If IRTXPOL = 1, the inverse of the IRDATA bit is output to the IRTXM pin on the IRV interval down-count boundaries. See Figure 4. When the envelope mode is enabled, it is possible to output either the modulated (IRENV[1:0] = 01b) or unmodulated (INENV[1:0] = 10b) carrier to the IRTX pin.

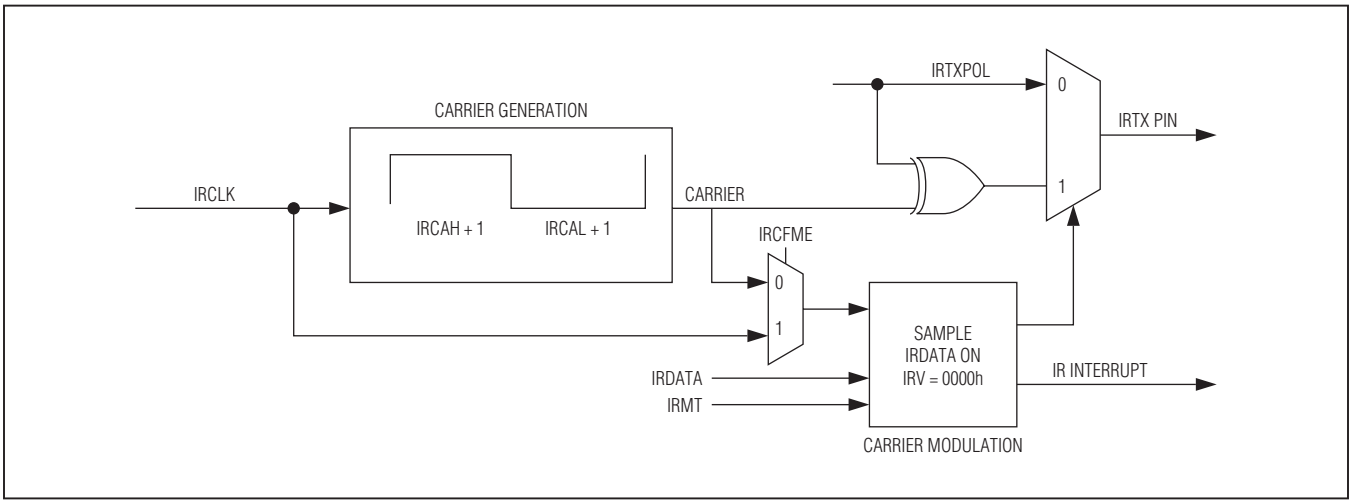


Figure 3. IR Transmit Carrier Generation and Carrier Modulator Control

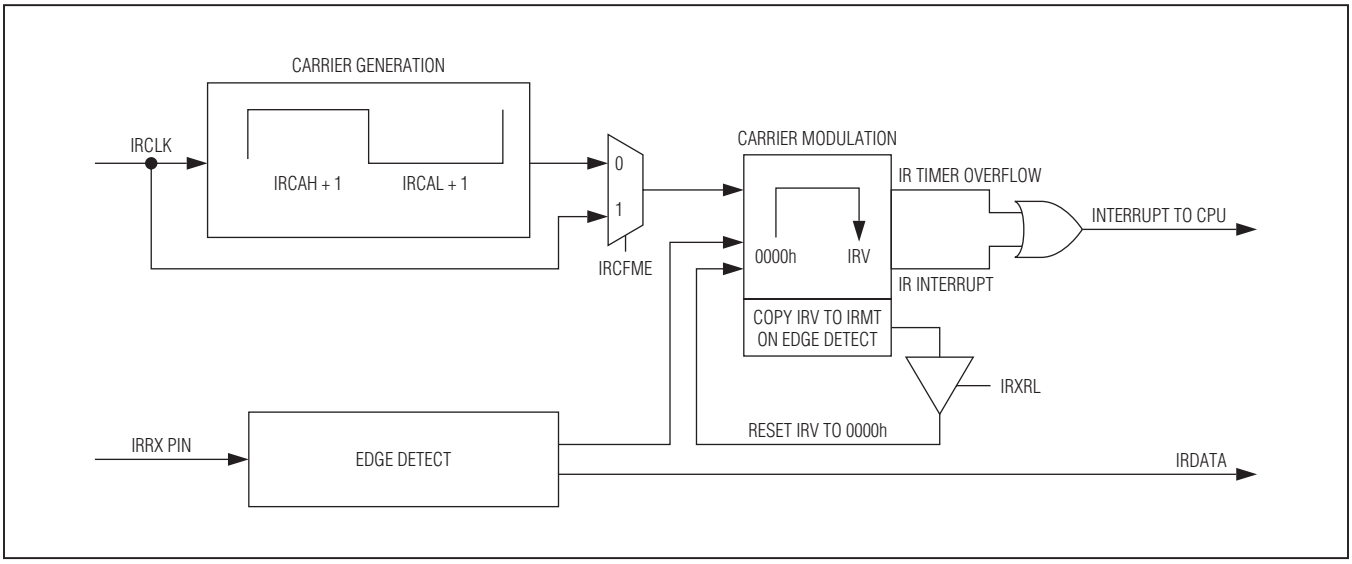


Figure 4. IR Capture

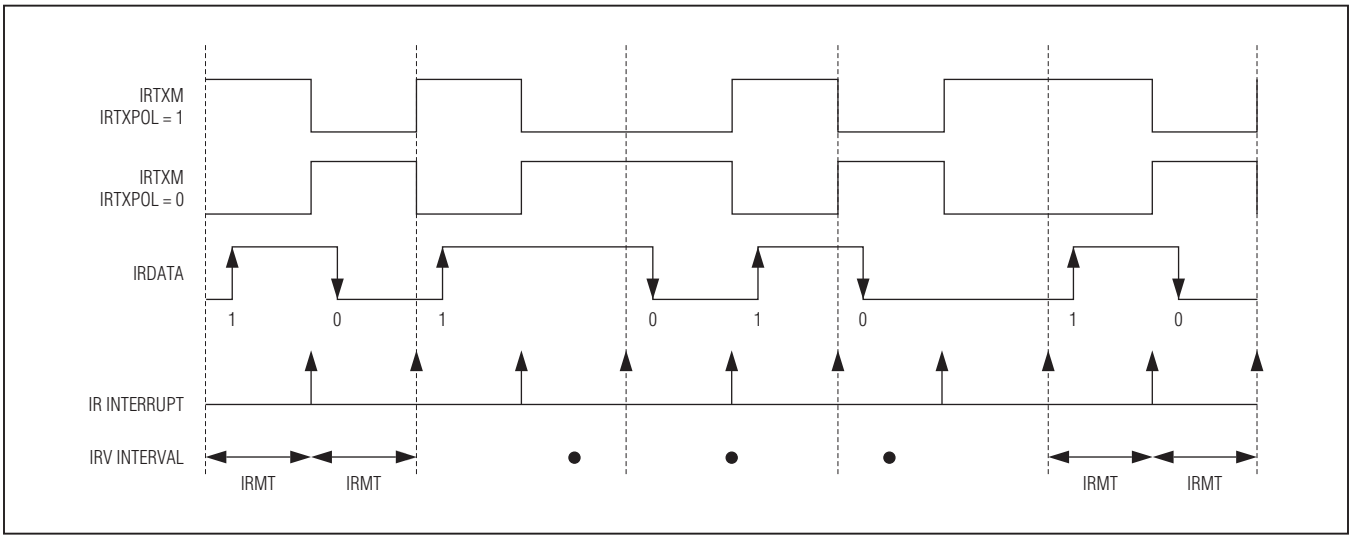
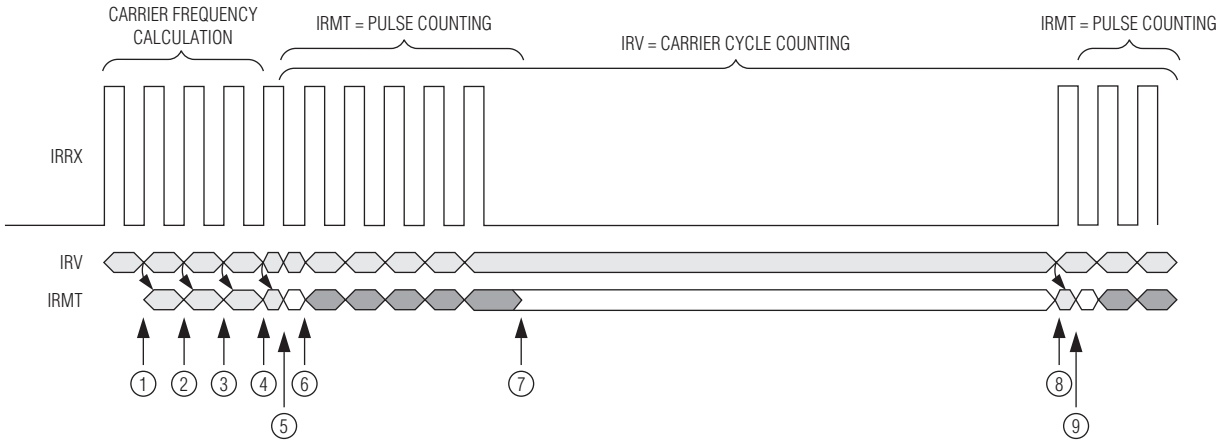


Figure 5. External IRTXM (Modulator) Output

IR Receive

When configured in receive mode (IRMODE = 0), the IR hardware supports the IRRX capture function (Figure 5). The IRRXSEL[1:0] bits define which edge(s) of the IRRX pin should trigger the IR timer capture function.

The IR module starts operating in the receive mode when IRMODE = 0 and IREN = 1. Once started, the IR timer (IRV) starts up counting from 0000h when a qualified capture event as defined by IRRXSEL happens. The IRV register is, by default, counting carrier cycles as defined by the IRCA register. However, the IR carrier frequency detect (IRCFME) bit can be set to 1 to allow clocking of the IRV register directly with the IRCLK for finer resolution. When IRCFME = 0, the IRCA defined carrier is counted by IRV (Figure 6). When IRCFME = 1, the IRCLK clocks the IRV register.



① TO ④ CAPTURE INTERRUPT (IRIF = 1).
IRV ≥ IRMT.
IRV = 0 (IF IRXRL = 1).

⑤ SOFTWARE SETS IRCA = CARRIER FREQUENCY.
SOFTWARE SETS RXBCNT = 1 (WHICH CLEARS IRMT = 0001 IN HARDWARE).
SOFTWARE CLEARS IRCFME = 0 SO THAT IRV COUNTS CARRIER CYCLES. IRV IS RESET TO 0 ON QUALIFIED EDGE DETECTION IF IRXRL = 1.
SOFTWARE ADDS TO IRMT THE NUMBER OF PULSES USED FOR CARRIER MEASUREMENT.
IRCA x 2x COUNTER FOR SPACE CAN BEGIN IMMEDIATELY (QUALIFIED EDGE RESETS).

⑥ QUALIFIED EDGE DETECTED: IRMT++
IRV RESET TO 0 IF IRXRL = 1.

⑦ IRCA x 2 PERIOD ELAPSES: IRIF = 1; CARRIER ABSENCE = SPACE.
BURST MARK = IRMT PULSES.
SOFTWARE CLEARS RXBCNT = 0 SO THAT WE CAPTURE ON THE NEXT QUALIFIED EDGE.

⑧ QUALIFIED EDGE DETECTED: IRIF = 1, CAPTURE IRV IRMT AS THE BURST SPACE (PLUS UP TO ONE CARRIER CYCLE).

⑨ SOFTWARE SET RXBCNT = 1 AS IN (5).
CONTINUE (5) TO (8) UNTIL LEARNING SPACE EXCEEDS SOME DURATION. IRV ROLLOVERS CAN BE USED.

Figure 7. Receive Burst-Count Example

16-Bit Timers/Counters

The MAXQ305 provides two timers/counters that support the following functions:

- 16-bit timer/counter
- 16-bit up/down autoreload
- Counter function of external pulse
- 16-bit timer with capture
- 16-bit timer with compare
- Input/output enhancements for pulse-width modulation
- Set/reset/toggle output state on comparator match
- Prescaler with 2n divider (for n = 0, 2, 4, 6, 8, 10)

USARTS

The MAXQ305 provides two Universal Synchronous/Asynchronous Receiver/Transmitter (USART) peripherals that include the following features:

- 2-wire interface
- Full-duplex operation for asynchronous data transfers
- Half-duplex operation for synchronous data transfers

Loading Flash Memory

An internal bootstrap loader allows reloading over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another microcontroller, or a connection to a PC serial port using a serial-to-JTAG converter such as the MAXQJTAG-001, available from Maxim. If in-system programmability is not required, a commercial gang programmer can be used for mass programming. Activating the JTAG interface and loading the test access port (TAP) with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to one during reset through the JTAG interface executes the bootstrap-loader mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

In addition, the ROM loader also enforces the memory-protection policies. Passwords that are 16 words are required to access the ROM loader interface.

Do not drive the LED or IRTX outputs while programming flash memory.

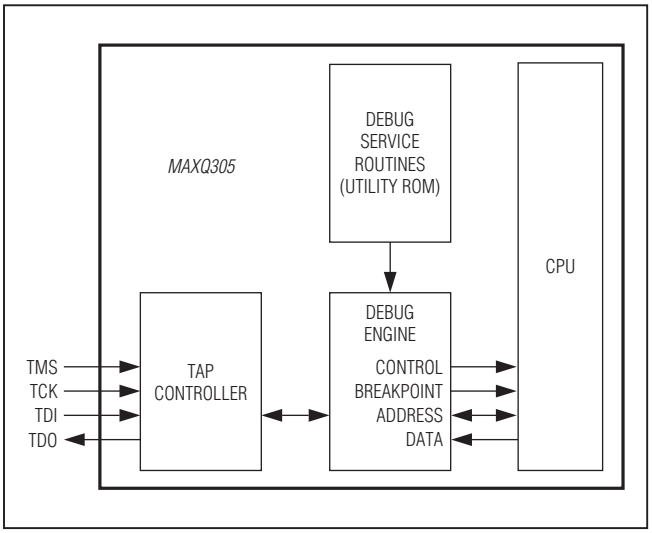


Figure 9. In-Circuit Debugger

Loading memory is not possible for ROM-only versions of the device.

In-Circuit Debug and JTAG Interface

Embedded debug hardware and software are developed and integrated to provide full in-circuit debugging capability in a user-application environment. These hardware and software features include the following:

- Debug engine
- Set of registers providing the ability to set breakpoints on register, code, or data using debug service routines stored in ROM

Collectively, these hardware and software features support two modes of in-circuit debug functionality:

- Background mode:

  CPU is executing the normal user program

  Allows the host to configure and set up the in-circuit debugger
- Debug mode:

  Debugger takes over the control of the CPU

  Read/write accesses to internal registers and memory

  Single-step of the CPU for trace operation

The interface to the debug engine is the TAP controller, as shown in Figure 9. The interface allows for communication with a bus master that can either be automatic test equipment or a component that interfaces to a higher level test bus as part of a complete system. The communication operates across a 4-wire serial interface from a dedicated TAP that is compatible with the JTAG IEEE Standard 1149. The TAP provides an independent serial channel to communicate synchronously with the host system.

To prevent unauthorized access of the protected memory regions through the JTAG interface, the debug engine prevents modification of the privilege registers and disallows all access to system memory, unless memory protection is disabled. In addition, all services (such as register display or modification) are denied when code is executing inside the system area. The debugger is not available for ROM-only versions of the device.

Operating Modes

The microcontroller has five power operating modes:

- High performance
- High voltage
- Green
- Idle
- Stop

The device is operating in high-performance mode when $V_{DD} > V_{DD\_PFM}$, the internal voltage regulator is enabled (HVREN = 1), the high-performance bit is set (PFMSEL = 1), and f_{HXFIN} = 12MHz. In this mode f_{SYSCLK} = 12MHz. The high-voltage regulator generates the voltages needed for flash memory programming, which is allowed in this mode.

The device is operating in high-voltage mode when $V_{DD} > V_{DD\_HV}$, HVREN = 1, PFMSEL = 0. In this mode $f_{SYSCLK} = f_{HFXIN}/3$. The high -oltage regulator generates the voltages needed for flash memory programming, which is allowed in this mode.

Green mode is the lowest power mode that allows code execution. In this mode HVREN = PFMSEL = 0. In this mode $f_{SYSCLK} = f_{HFXIN}/3$. Flash programming is not allowed in this mode.

Setting the IDLE bit in the CKCN register to 1 invokes the idle mode. Once in idle mode, all resources are preserved and all clocks remain active with the enabled peripherals, and power monitor continues to work, so the processor can exit the idle state using any of the interrupt sources that are enabled. The IDLE bit is cleared automatically once the idle state is exited; allowing the processor to execute the instruction that immediately follows the instruction that set the IDLE bit.

The lowest power mode of operation for the MAXQ305 is stop mode. The user software can enter stop mode any time the microcontroller is in a state where code does not need to be executed. In this mode, CPU state and memories are preserved, but the CPU is not actively running. Wake-up sources include external I/O interrupts, the power-fail warning interrupt, or a power-fail reset. The nanopower ring oscillator is an internal ultra-low-power (400nA) 8kHz ring oscillator that can be used to drive a wake-up timer that exits stop mode. The wake-up timer is programmable by software in steps of 125µs up to approximately 8s.

The power-fail monitor is always on during normal operation. However, it can be selectively disabled during stop mode to minimize power consumption. This feature is enabled using the power-fail monitor disable (PFD) bit in the PWCN register. The reset default state for the PFD bit is 1, which disables the power-fail monitor function during stop mode. If power-fail monitoring is disabled (PFD = 1) during stop mode, the circuitry responsible for generating a power-fail warning or reset is shut down and neither condition is detected. Thus, the $V_{DD} < V_{RST}$ condition does not invoke a reset state.

Power-Fail Detection

Figure 10, Figure 11, Figure 12, and Figure 13 show the power-fail detection and response during normal and stop mode operation. If a reset is caused by a power-fail, the power-fail monitor can be set to one of the following intervals:

- Always on—continuous monitoring
- 2^{11} nanopower ring oscillator clocks (~256ms)
- 2^{12} nanopower ring oscillator clocks (~512ms)
- 2^{13} nanopower ring oscillator clocks (~1.024s)

In the case where the power-fail circuitry is periodically turned on, the power-fail detection is turned on for two nanopower ring oscillator cycles. If $V_{DD} > V_{RST}$ during detection, V_{DD} is monitored for an additional nanopower ring oscillator period. If V_{DD} remains above V_{RST} for the third nanopower ring period, the CPU exits the reset state and resumes normal operation from utility ROM at 8000h after satisfying the crystal warm-up period.

If a reset is generated by any other event, such as the $\overline{\text{RESET}}$ pin being driven low externally or the watchdog timer, then the power-fail, internal regulator, and crystal remain on during the CPU reset. In these cases, the CPU exits the reset state in less than 20 external clock cycles after the reset source is removed.

RESET state in less than 20 crystal cycles after the reset source is removed.

Table 4. Power-Fail Detection States During Normal Operation

STATE	POWER-FAIL DETECTOR	REGOUT LDO	BACKUP REGULATOR	CRYSTAL OSCILLATOR	SRAM DATA RETENTION	NOTES
A	OFF	OFF	ON	OFF	—	$V_{DD} < V_{POR}$
B	OFF	OFF	ON	OFF	—	$V_{POR} < V_{DD} < V_{RST}$ nano-ring clock enabled X3 charge pump enabled
C	OFF	OFF	ON	OFF	—	$V_{DCX3} < V_{DCX3\_OK}$ Supply Voltage Monitor enabled
D	ON	ON	ON	ON	—	X2 charge pump enabled LDO enabled Crystal oscillator enabled
E	ON	ON	OFF	ON	—	$V_{DCX2} > V_{DCX2\_OK}$ $V_{REGOUT} > V_{REGOUT\_OK\_L}$ Backup regulator disabled CPU assume normal operation
F	ON	ON	OFF	ON	—	Power drop too short. Power-fail not detected
G	ON	ON	OFF	ON	—	$V_{RST} < V_{DD} < V_{PFW}$ PFI is set when $V_{RST} < V_{DD} < V_{PFW}$ and maintains this state for at least t_{PFW}, at which time a power-fail interrupt is generated (if enabled). CPU continues normal operation.
H	ON (periodically)	OFF	ON	OFF	YES	$V_{POR} < V_{DD} < V_{RST}$ Power-fail detected CPU goes into reset Power-fail monitor turned on periodically
I	OFF	OFF	ON	OFF	YES	$V_{DD} < V_{POR}$ Device held in reset, no operation allowed

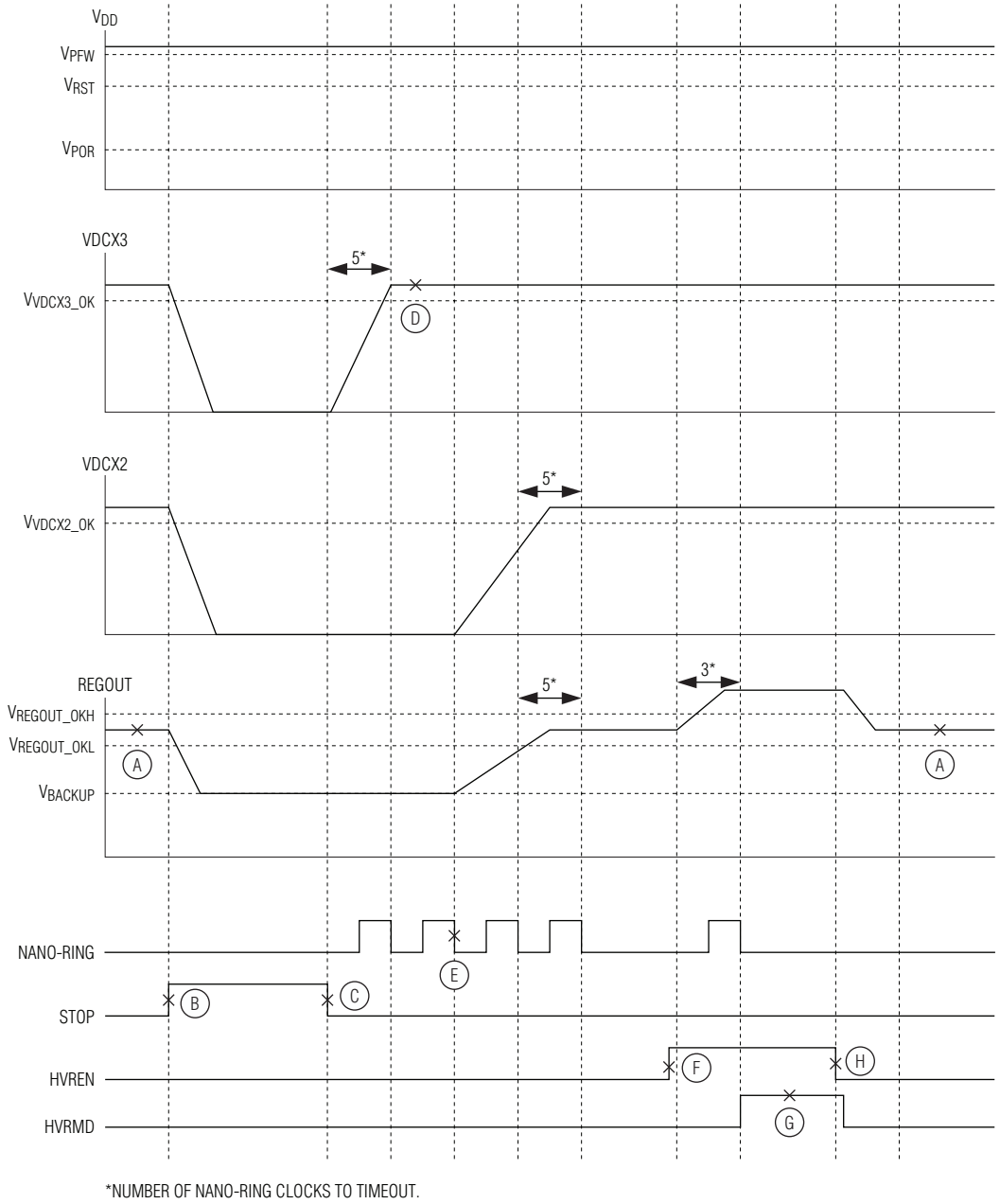


Figure 11. Stop Mode and High Voltage Mode Transition

Table 5. Stop Mode and High Voltage Mode Transition

STATE	POWER-FAIL DETECTOR	REGOUT LDO	BACKUP REGULATOR	CRYSTAL OSCILLATOR	SRAM DATA RETENTION	NOTES
A	ON	ON	OFF	ON	—	$V_{DCX2} > V_{DCX2\_OK}$ $V_{REGOUT\_OK\_L} < V_{REGOUT} < V_{REGOUT\_OK\_H}$ CPU operates normally Flash writes not allowed
B	OFF	OFF	ON	OFF	YES	Stop mode requested CPU stopped X3 charge pump, X2 charge pump, LDO, Power-fail detector and crystal oscillator disabled Backup regulator enabled
C	OFF	OFF	ON	OFF	YES	Stop mode exit requested nano-ring clock enabled X3 charge pump enabled
D	ON	OFF	ON	OFF	YES	$V_{DCX3} > V_{DCX3\_OK}$ Supply Voltage Monitor enabled
E	ON	ON	ON	ON	YES	X2 charge pump enabled LDO enabled Crystal oscillator enabled
F	ON	ON	OFF	ON	—	High voltage mode requested LDO output increased Nano-ring enabled
G	ON	ON	OFF	ON	—	High voltage mode accepted Flash writes allowed
H	ON	ON	OFF	ON	—	Low voltage mode requested Flash writes not allowed

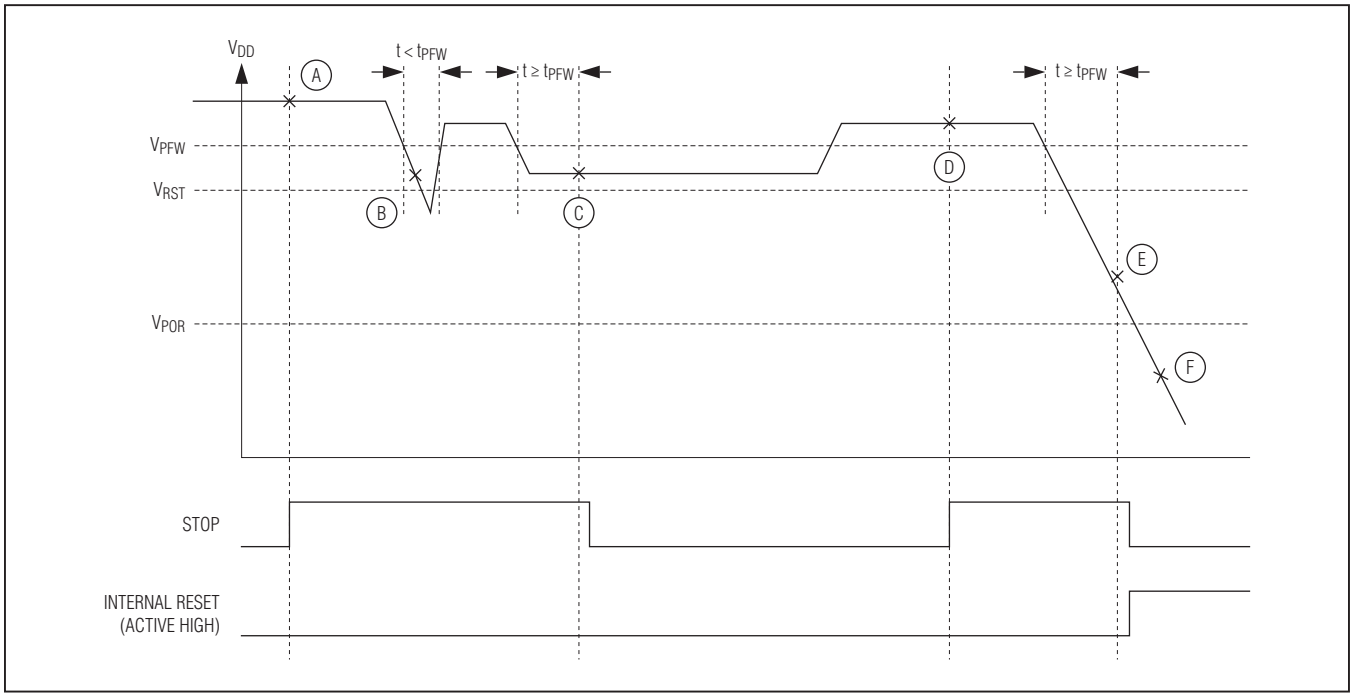


Figure 12. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

Table 6. Stop Mode Power-Fail Detection States with Power-Fail Monitor Enabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	On	Off	Off	Yes	Power drop too short. Power-fail not detected.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. Power-fail warning detected. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. Exit stop mode.
D	On	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
E	On (Periodically)	Off	Off	Yes	$V_{POR} < V_{DD} < V_{RST}$. Power-fail detected. CPU goes into reset. Power-fail monitor turns on periodically.
F	Off	Off	Off	—	$V_{DD} < V_{POR}$. Device held in reset. No operation allowed.

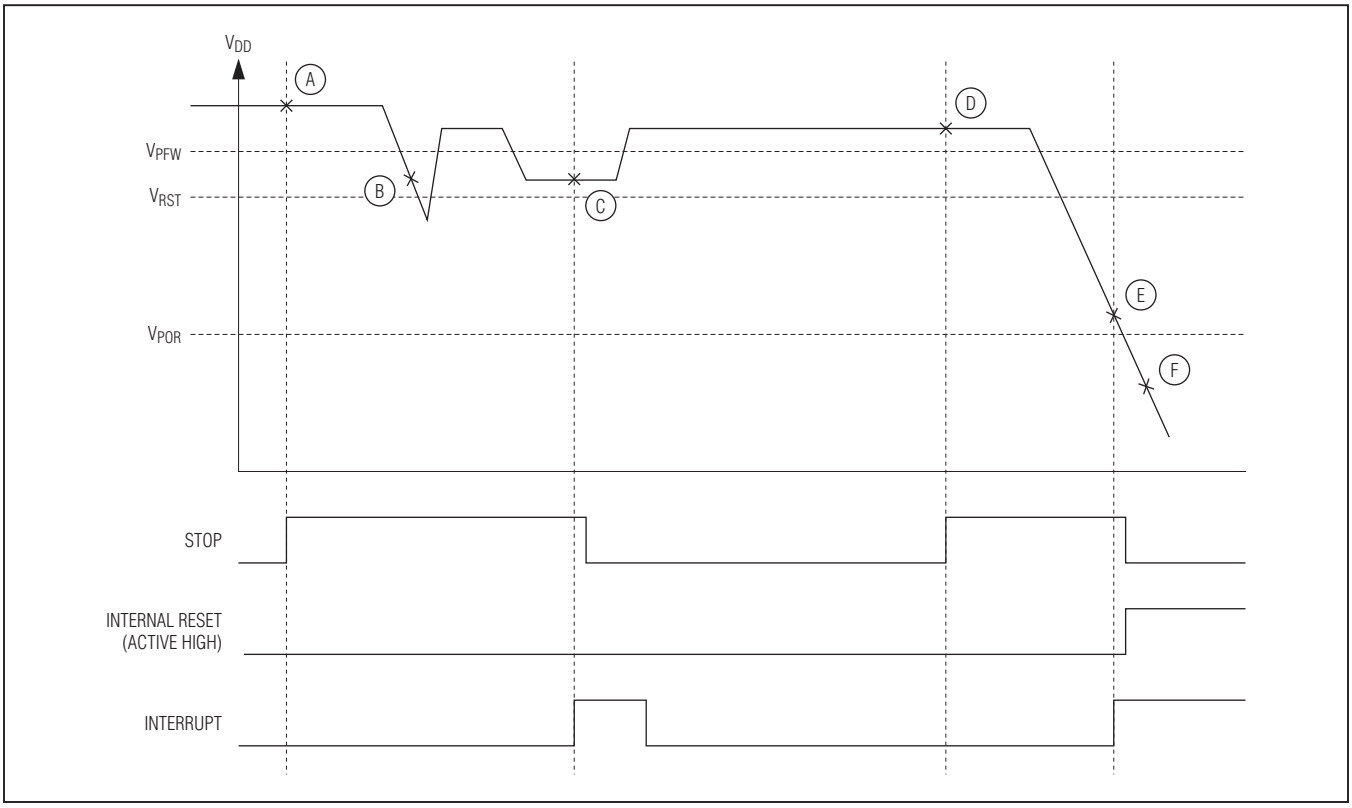


Figure 13. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

Table 7. Stop Mode Power-Fail Detection States with Power-Fail Monitor Disabled

STATE	POWER-FAIL	INTERNAL REGULATOR	CRYSTAL OSCILLATOR	SRAM RETENTION	COMMENTS
A	Off	Off	Off	Yes	Application enters stop mode. $V_{DD} > V_{RST}$. CPU in stop mode.
B	Off	Off	Off	Yes	$V_{DD} < V_{PFW}$. Power-fail not detected because power-fail monitor is disabled.
C	On	On	On	Yes	$V_{RST} < V_{DD} < V_{PFW}$. An interrupt occurs that causes the CPU to exit stop mode. Power-fail monitor is turned on, detects a power-fail warning, and sets the power-fail interrupt flag. Turn on regulator and crystal. Crystal warmup time, t_{XTAL_RDY}. On stop mode exit, CPU vectors to the higher priority of power-fail and the interrupt that causes stop mode exit.

Low-Voltage Microcontroller with Infrared Module

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/12	Initial release	—