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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	75
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	6K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f21388sdfp-30

Table 1.2 Specifications (2)

Item	Function	Description
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I^2C mode (I^2C-bus), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0	1 channel (also used for the I^2C bus)
	(I^2C bus) I^2C_0	1 channel (also used for the SSU)
LIN module	HW-LIN_0	Hardware LIN 1 channel (timer RJ_0, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 20 channels, sample and hold function, sweep mode
Comparator B		2 circuits
Touch sensor control unit (TSCU)		System CH × 4, electrostatic capacitive touch detection × 36
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Operating frequency/ Power supply voltage		CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz) Typ. 2.2 μA (VCC = 3.0 V, stop mode)
Operating ambient temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the D version if it is to be used.

1.2 Product List

Table 1.3 lists product information. Figure 1.1 shows the Product Part Number Structure.

Table 1.3 Product List **Current of Dec 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21388SNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	N version
R5F2138ASNFP	96 Kbytes		8 Kbytes		
R5F2138CSNFP	128 Kbytes		10 Kbytes		
R5F21388SDFP	64 Kbytes		6 Kbytes	PLQP0080KB-A	D version
R5F2138ASDFP	96 Kbytes		8 Kbytes		
R5F2138CSDFP	128 Kbytes		10 Kbytes		

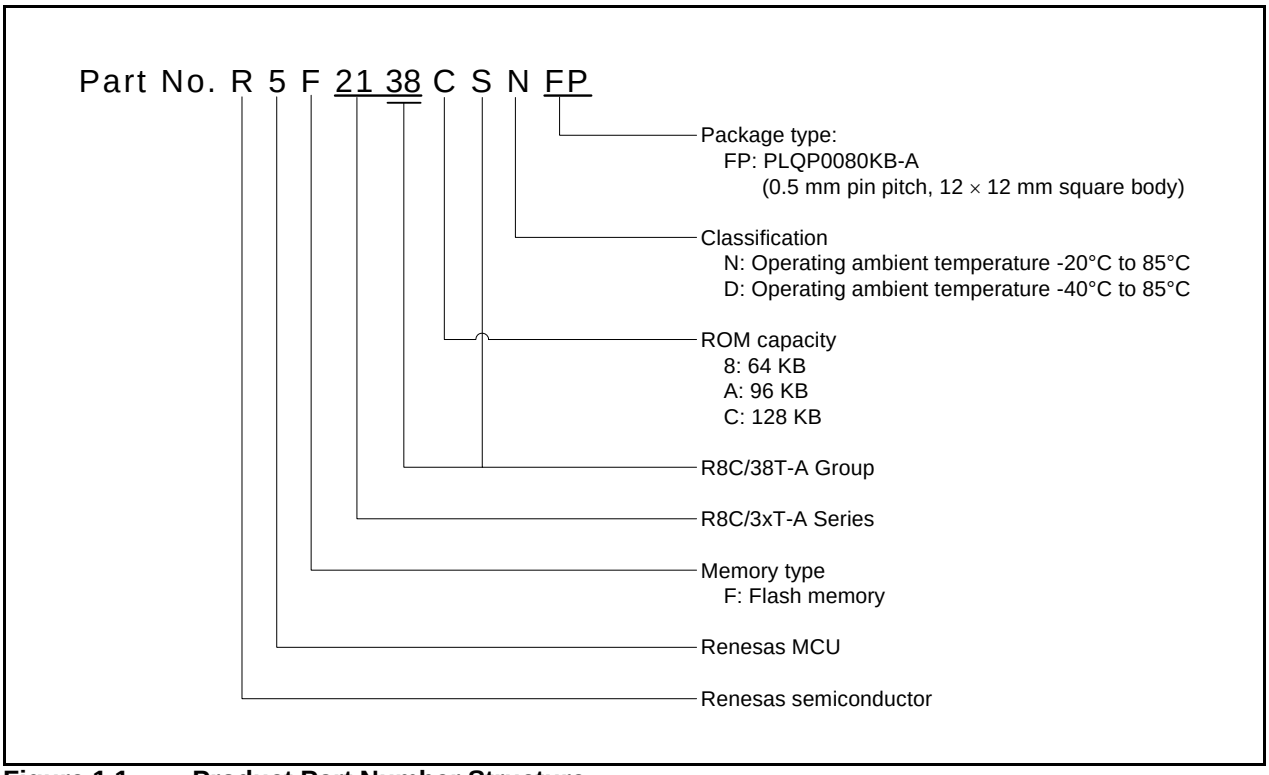

Figure 1.1 Product Part Number Structure

Table 1.4 Pin Name Information by Pin Number (INT, URAT0, and UART2) (1)

Port	Pin No.	INT					UART0						UART2						
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	SDA2	SCL2	CLK2
P0_0	72																		
P0_1	71							TXD_1											
P0_2	70									RXD_1									
P0_3	69											CLK_1							
P0_4	68																		
P0_5	67																		
P0_6	66																		
P0_7	65																		
P1_0	56																		
P1_1	55																		
P1_2	54																		
P1_3	53																		
P1_4	52						TXD_0												
P1_5	51		$\overline{INT1}$						RXD_0										
P1_6	50										CLK_0								
P1_7	49		$\overline{INT1}$																
P2_0	30		$\overline{INT1}$																
P2_1	29																		
P2_2	28																		
P2_3	27																		
P2_4	26																		
P2_5	25																		
P2_6	24																		
P2_7	23																		
P3_0	4																		
P3_1	36																		
P3_2	3		$\overline{INT1}$	$\overline{INT2}$															
P3_3	22				$\overline{INT3}$										$\overline{CTS2}$	$\overline{RTS2}$			
P3_4	21												TXD2	RXD2			SDA2	SCL2	
P3_5	20																		CLK2
P3_6	35																		
P3_7	19												TXD2	RXD2			SDA2	SCL2	
P4_2	5																		
P4_3	7																		
P4_4	8																		
P4_5	48	$\overline{INT0}$												RXD2				SCL2	
P4_6	12																		
P4_7	10																		
P5_0	18																		
P5_1	17																		
P5_2	16																		
P5_3	15																		
P5_4	14																		
P5_5	2																		
P5_6	1																		
P5_7	80																		
P6_0	77																		
P6_1	76																		
P6_2	75											CLK_1							
P6_3	74							TXD_1											
P6_4	73									RXD_1									
P6_5	47					$\overline{INT4}$						CLK_1							CLK2
P6_6	46			$\overline{INT2}$									TXD2				SDA2		
P6_7	45				$\overline{INT3}$														
P7_0	64																		
P7_1	63																		
P7_2	62																		
P7_3	61																		
P7_4	60																		
P7_5	59																		
P7_6	58																		
P7_7	57																		

Table 1.5 Pin Name Information by Pin Number (INT, URAT0, and UART2) (2)

Port	Pin No.	INT					UART0						UART2						
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	SDA2	SCL2	CLK2
P8_0	44																		
P8_1	43																		
P8_2	42																		
P8_3	41																		
P8_4	40																		
P8_5	39																		
P8_6	38																		
P8_7	37																		
P9_0	34																		
P9_1	33																		
P9_2	32																		
P9_3	31																		
P9_4	79																		
P9_5	78																		

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

3.2 Special Function Registers (SFRs)

An SFR (special function register) is a control register for a peripheral function. Tables 3.1 to 3.16 list the SFR Information. Table 3.17 lists the ID code Area, Option Function Select Area.

Table 3.1 SFR Information (1) (1)

Address	Symbol	Register Name	After Reset	Remarks
00000h				
00001h				
00002h				
00003h				
00004h	PM0	Processor Mode Register 0	00h	
00005h	PM1	Processor Mode Register 1	10000000b	
00006h				
00007h	PRCR	Protect Register	00h	
00008h	CM0	System Clock Control Register 0	00101000b	
00009h	CM1	System Clock Control Register 1	00100000b	
0000Ah	OCD	Oscillation Stop Detection Register	00h	
0000Bh	CM3	System Clock Control Register 3	00h	
0000Ch	CM4	System Clock Control Register 4	00000001b	
0000Dh				
0000Eh				
0000Fh				
00010h	CPSRF	Clock Prescaler Reset Flag	00h	
00011h				
00012h	FRA0	High-Speed On-Chip Oscillator Control Register 0	00h	
00013h				
00014h	FRA2	High-Speed On-Chip Oscillator Control Register 2	00h	
00015h				
00016h				
00017h				
00018h				
00019h				
0001Ah				
0001Bh				
0001Ch				
0001Dh				
0001Eh				
0001Fh				
00020h	RISR	Reset Interrupt Select Register	10000000b or 00000000b	(Note 2)
00021h	WDTR	Watchdog Timer Reset Register	FFh	
00022h	WDTS	Watchdog Timer Start Register	FFh	
00023h	WDTC	Watchdog Timer Control Register	01111111b	
00024h	CSPR	Count Source Protection Mode Register	10000000b or 00000000b	(Note 2)
00025h				
00026h				
00027h				
00028h	RSTFR	Reset Source Determination Register	00XXXXXXb	
00029h				
0002Ah				
0002Bh				
0002Ch	SVDC	STBY VDC Power Control Register	00h	
0002Dh				
0002Eh				
0002Fh				
00030h	CMPA	Voltage Monitor Circuit Control Register	00h	
00031h	VCAC	Voltage Monitor Circuit Edge Select Register	00h	
00032h	OCVREFCR	On-Chip Reference Voltage Control Register	00h	
00033h				
00034h	VCA2	Voltage Detection Register 2	00000000b or 00100000b	(Note 3)
00035h				
00036h	VD1LS	Voltage Detection 1 Level Select Register	00000111b	
00037h				
00038h	VW0C	Voltage Monitor 0 Circuit Control Register	1100XX10b or 1100XX11b	(Note 3)
00039h	VW1C	Voltage Monitor 1 Circuit Control Register	10001010b	

X: Undefined

Notes:

1. The blank areas are reserved. No access is allowed.
2. Depends on the CSPROINI bit in the OFS register.
3. Depends on the LVDASI bit in the OFS register.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.13 SFR Information (13) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C0Ah		Area for storing DTC transfer vector 10	XXh	
06C0Bh		Area for storing DTC transfer vector 11	XXh	
06C0Ch		Area for storing DTC transfer vector 12	XXh	
06C0Dh		Area for storing DTC transfer vector 13	XXh	
06C0Eh		Area for storing DTC transfer vector 14	XXh	
06C0Fh		Area for storing DTC transfer vector 15	XXh	
06C10h		Area for storing DTC transfer vector 16	XXh	
06C11h		Area for storing DTC transfer vector 17	XXh	
06C12h		Area for storing DTC transfer vector 18	XXh	
06C13h		Area for storing DTC transfer vector 19	XXh	
06C14h				
06C15h				
06C16h		Area for storing DTC transfer vector 22	XXh	
06C17h		Area for storing DTC transfer vector 23	XXh	
06C18h		Area for storing DTC transfer vector 24	XXh	
06C19h		Area for storing DTC transfer vector 25	XXh	
06C1Ah				
06C1Bh				
06C1Ch				
06C1Dh				
06C1Eh				
06C1Fh				
06C20h				
06C21h				
06C22h				
06C23h				
06C24h				
06C25h				
06C26h				
06C27h				
06C28h				
06C29h				
06C2Ah		Area for storing DTC transfer vector 42	XXh	
06C2Bh				
06C2Ch				
06C2Dh				
06C2Eh				
06C2Fh				
06C30h				
06C31h		Area for storing DTC transfer vector 49	XXh	
06C32h				
06C33h		Area for storing DTC transfer vector 51	XXh	
06C34h		Area for storing DTC transfer vector 52	XXh	
06C35h		Area for storing DTC transfer vector 53	XXh	
06C36h		Area for storing DTC transfer vector 54	XXh	
06C37h				
06C38h				
06C39h				
06C3Ah				
06C3Bh				
06C3Ch				
06C3Dh				
06C3Eh				
06C3Fh				
06C40h	DTCCR0	DTC Control Register 0	XXh	
06C41h	DTBLS0	DTC Block Size Register 0	XXh	
06C42h	DTCCT0	DTC Transfer Count Register 0	XXh	
06C43h	DTRLD0	DTC Transfer Count Reload Register 0	XXh	
06C44h	DTSAR0	DTC Source Address Register 0	XXXXh	
06C45h				
06C46h	DTDAR0	DTC Destination Address Register 0	XXXXh	
06C47h				
06C48h	DTCCR1	DTC Control Register 1	XXh	
06C49h	DTBLS1	DTC Block Size Register 1	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.14 SFR Information (14) (1)

Address	Symbol	Register Name	After Reset	Remarks
06C4Ah	DTCCT1	DTC Transfer Count Register 1	XXh	
06C4Bh	DTRLD1	DTC Transfer Count Reload Register 1	XXh	
06C4Ch	DTSAR1	DTC Source Address Register 1	XXXXh	
06C4Dh				
06C4Eh	DTDAR1	DTC Destination Address Register 1	XXXXh	
06C4Fh				
06C50h	DTCCR2	DTC Control Register 2	XXh	
06C51h	DTBLS2	DTC Block Size Register 2	XXh	
06C52h	DTCCT2	DTC Transfer Count Register 2	XXh	
06C53h	DTRLD2	DTC Transfer Count Reload Register 2	XXh	
06C54h	DTSAR2	DTC Source Address Register 2	XXXXh	
06C55h				
06C56h	DTDAR2	DTC Destination Address Register 2	XXXXh	
06C57h				
06C58h	DTCCR3	DTC Control Register 3	XXh	
06C59h	DTBLS3	DTC Block Size Register 3	XXh	
06C5Ah	DTCCT3	DTC Transfer Count Register 3	XXh	
06C5Bh	DTRLD3	DTC Transfer Count Reload Register 3	XXh	
06C5Ch	DTSAR3	DTC Source Address Register 3	XXXXh	
06C5Dh				
06C5Eh	DTDAR3	DTC Destination Address Register 3	XXXXh	
06C5Fh				
06C60h	DTCCR4	DTC Control Register 4	XXh	
06C61h	DTBLS4	DTC Block Size Register 4	XXh	
06C62h	DTCCT4	DTC Transfer Count Register 4	XXh	
06C63h	DTRLD4	DTC Transfer Count Reload Register 4	XXh	
06C64h	DTSAR4	DTC Source Address Register 4	XXXXh	
06C65h				
06C66h	DTDAR4	DTC Destination Address Register 4	XXXXh	
06C67h				
06C68h	DTCCR5	DTC Control Register 5	XXh	
06C69h	DTBLS5	DTC Block Size Register 5	XXh	
06C6Ah	DTCCT5	DTC Transfer Count Register 5	XXh	
06C6Bh	DTRLD5	DTC Transfer Count Reload Register 5	XXh	
06C6Ch	DTSAR5	DTC Source Address Register 5	XXXXh	
06C6Dh				
06C6Eh	DTDAR5	DTC Destination Address Register 5	XXXXh	
06C6Fh				
06C70h	DTCCR6	DTC Control Register 6	XXh	
06C71h	DTBLS6	DTC Block Size Register 6	XXh	
06C72h	DTCCT6	DTC Transfer Count Register 6	XXh	
06C73h	DTRLD6	DTC Transfer Count Reload Register 6	XXh	
06C74h	DTSAR6	DTC Source Address Register 6	XXXXh	
06C75h				
06C76h	DTDAR6	DTC Destination Address Register 6	XXXXh	
06C77h				
06C78h	DTCCR7	DTC Control Register 7	XXh	
06C79h	DTBLS7	DTC Block Size Register 7	XXh	
06C7Ah	DTCCT7	DTC Transfer Count Register 7	XXh	
06C7Bh	DTRLD7	DTC Transfer Count Reload Register 7	XXh	
06C7Ch	DTSAR7	DTC Source Address Register 7	XXXXh	
06C7Dh				
06C7Eh	DTDAR7	DTC Destination Address Register 7	XXXXh	
06C7Fh				
06C80h	DTCCR8	DTC Control Register 8	XXh	
06C81h	DTBLS8	DTC Block Size Register 8	XXh	
06C82h	DTCCT8	DTC Transfer Count Register 8	XXh	
06C83h	DTRLD8	DTC Transfer Count Reload Register 8	XXh	
06C84h	DTSAR8	DTC Source Address Register 8	XXXXh	
06C85h				
06C86h	DTDAR8	DTC Destination Address Register 8	XXXXh	
06C87h				
06C88h	DTCCR9	DTC Control Register 9	XXh	
06C89h	DTBLS9	DTC Block Size Register 9	XXh	
06C8Ah	DTCCT9	DTC Transfer Count Register 9	XXh	
06C8Bh	DTRLD9	DTC Transfer Count Reload Register 9	XXh	
06C8Ch	DTSAR9	DTC Source Address Register 9	XXXXh	
06C8Dh				
06C8Eh	DTDAR9	DTC Destination Address Register 9	XXXXh	
06C8Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.17 ID code Area, Option Function Select Area

Address	Symbol	Area Name	After Reset	Address size
:				
0FFDBh	OFS2	Option Function Select Register 2	(Note 1)	
:				
0FFDFh	ID1		(Note 2)	
:				
0FFE3h	ID2		(Note 2)	
:				
0FFEBh	ID3		(Note 2)	
:				
0FFEFh	ID4		(Note 2)	
:				
0FFF3h	ID5		(Note 2)	
:				
0FFF7h	ID6		(Note 2)	
:				
0FFFBh	ID7		(Note 2)	
:				
0FFFFh	OFS	Option Function Select Register	(Note 1)	

Notes:
1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the option function select area. Erasing the block including the option function select area sets the option function select area to FFh.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the ID code area. Erasing the block including the ID code area sets the ID code area to FFh.

Table 4.6 Flash Memory (Data flash Block A to Block D) Characteristics (Vcc = 2.7 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)		10,000 (2)	—	—	times
—	Byte program time (Program and erase endurance ≤ 1,000 times)		—	160	950	µs
—	Byte program time (Program and erase endurance > 1,000 times)		—	300	950	µs
—	Block erase time (Program and erase endurance ≤ 1,000 times)		—	0.2	1	s
—	Block erase time (Program and erase endurance > 1,000 times)		—	0.3	1	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	3 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 (N ver.) –40 (D ver.)	—	85	°C
—	Data hold time (6)	Ambient temperature = 55°C (7)	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100, 1,000 or 10,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. In addition, averaging the erasure endurance between blocks A to D can further reduce the actual erasure endurance. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. The data hold time includes 7,000 hours under an environment of ambient temperature 85°C.

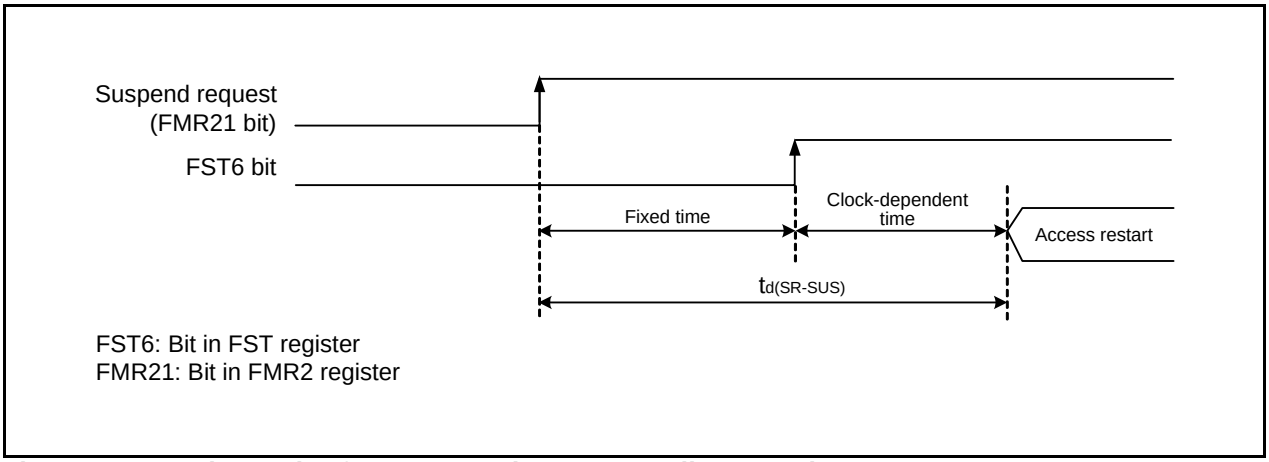

Figure 4.2 Time Delay from Suspend Request until Suspend

Table 4.7 Voltage Detection 0 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When Vcc falls	1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet0_2 (1)	When Vcc falls	2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)	When Vcc falls	3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 4.15 DC Characteristics (2) [3.3 V ≤ Vcc ≤ 5.5 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	20 MHz	Off	Off	125 kHz	No division	—		—	6.5	15	mA
			16 MHz	Off	Off	125 kHz	No division	—		—	5.3	12.5	mA
			10 MHz	Off	Off	125 kHz	No division	—		—	3.6	—	mA
			20 MHz	Off	Off	125 kHz	Divide-by-8	—		—	3.0	—	mA
			16 MHz	Off	Off	125 kHz	Divide-by-8	—		—	2.2	—	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	—	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	400	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	—	FMR27 = 1 SVC0 = 0		—	85	400	µA
			Off	32 kHz	Off	Off	—	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	47	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	100	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	90	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 3.3 V to 5.5 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 4.17 DC Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified))

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	10 MHz	Off	Off	125 kHz	No division	—		—	3.5	10	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	7.5	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	No division	—		—	4.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	Divide-by-8	—		—	1.5	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	390	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	40	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 4.19 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—		—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—		—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz (3)	125 kHz	No division	—		—	2.5	10	mA
			Off	Off	5 MHz (3)	125 kHz	Divide-by-8	—		—	1.7	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	300	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	350	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

4.5 AC Characteristics

Table 4.20 Timing Requirements of Clock Synchronous Serial I/O with Chip Select (during Master Operation) (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
t_{SUCYC}	SSCK clock cycle time		4.00	—	—	t_{CYC} (1)
t_{HI}	SSCK clock high width		0.40	—	0.60	t_{SUCYC}
t_{LO}	SSCK clock low width		0.40	—	0.60	t_{SUCYC}
t_{RISE}	SSCK clock rising time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	0.50	t_{CYC} (1)
		1.8 V ≤ Vcc < 2.7 V	—	—	1.00	t_{CYC} (1)
t_{FALL}	SSCK clock falling time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	0.50	t_{CYC} (1)
		1.8 V ≤ Vcc < 2.7 V	—	—	1.00	t_{CYC} (1)
t_{SU}	SSI, SSO data input setup time	4.5 V ≤ Vcc ≤ 5.5 V	60	—	—	ns
		2.7 V ≤ Vcc < 4.5 V	70	—	—	ns
		1.8 V ≤ Vcc < 2.7 V	100	—	—	ns
t_H	SSI, SSO data input hold time	2.7 V ≤ Vcc ≤ 5.5 V	2.00	—	—	t_{CYC} (1)
		1.8 V ≤ Vcc < 2.7 V	2.00	—	—	t_{CYC} (1)
t_{LEAD}	$\overline{SCS}$-SCK output delay time		0.5 t_{SUCYC} - 1 t_{CYC}	—	—	ns
t_{LAG}	SCK -$\overline{SCS}$ output valid time		0.5 t_{SUCYC} - 1 t_{CYC}	—	—	ns
t_{OD}	SSO data output delay time	2.7 V ≤ Vcc ≤ 5.5 V	—	—	30.00	ns
		1.8 V ≤ Vcc < 2.7 V	—	—	1.00	t_{CYC} (1)

Note:
1. 1t_{CYC} = 1/f1 (s)

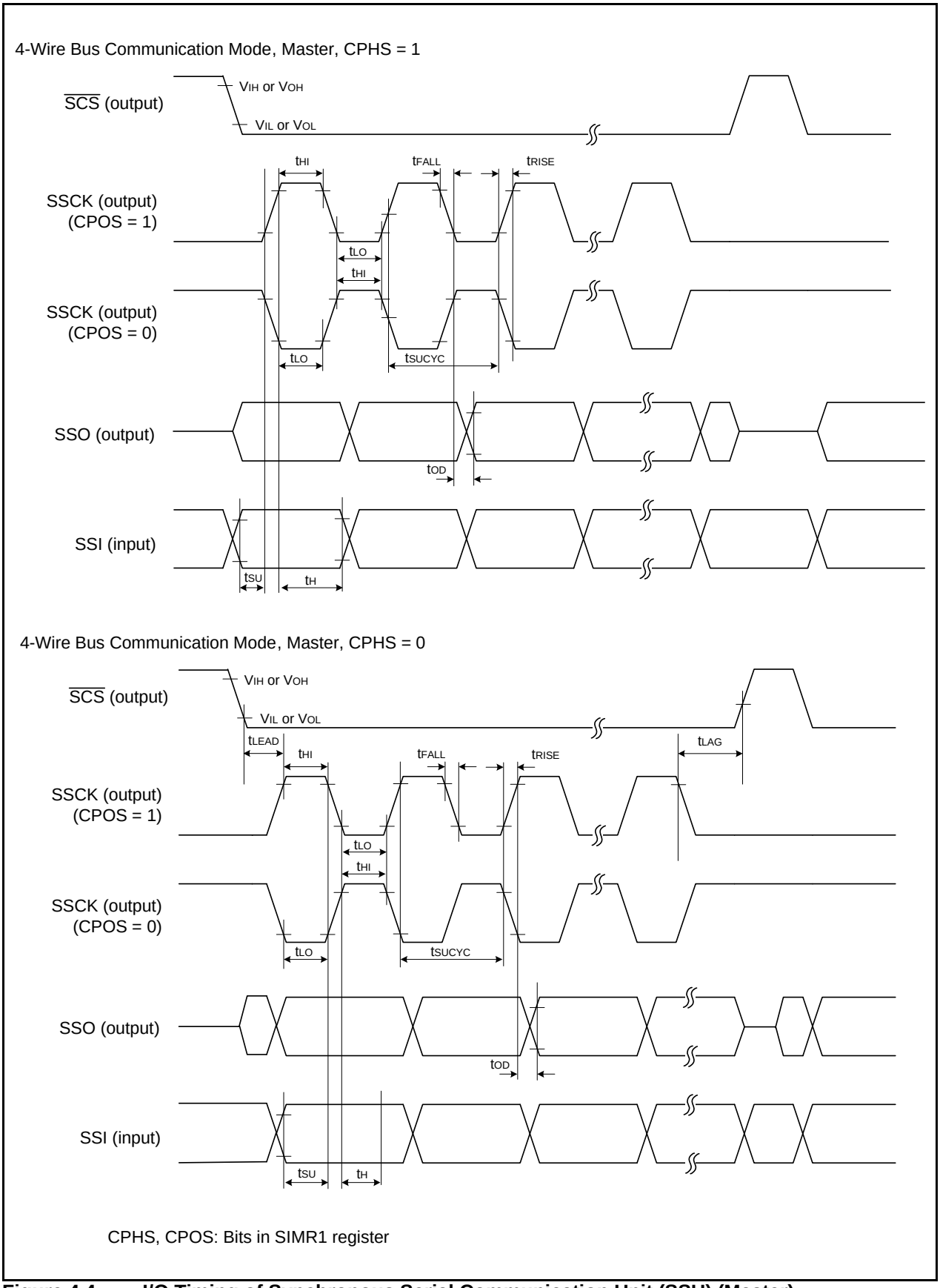

Figure 4.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

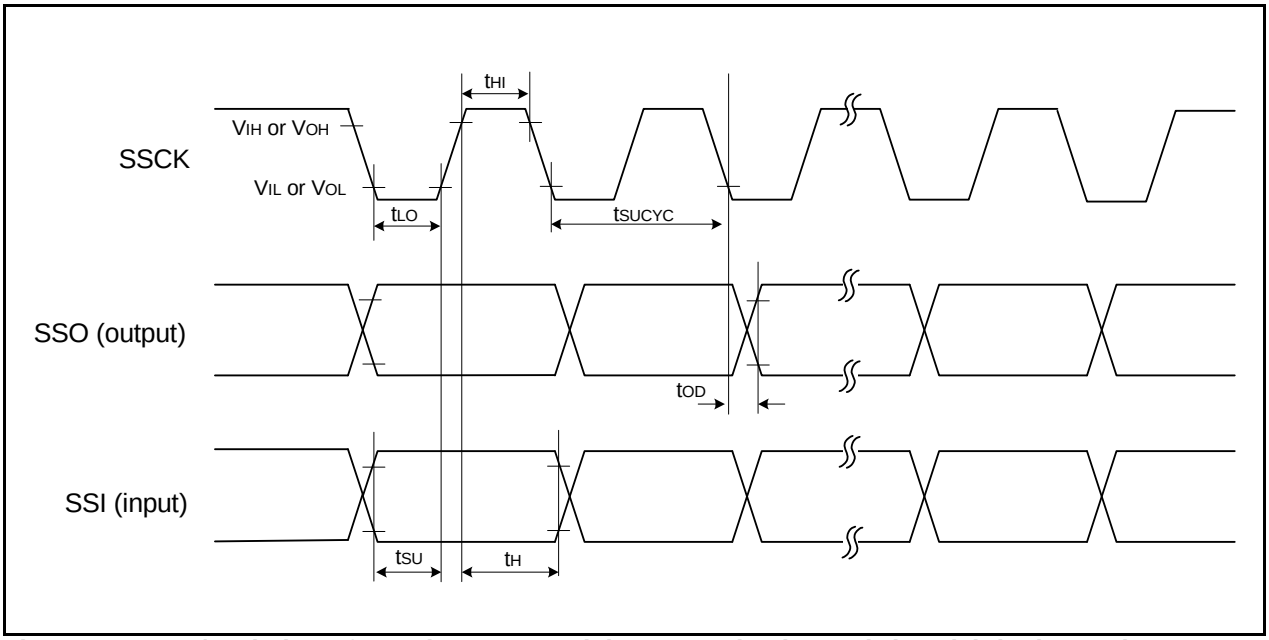

Figure 4.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

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