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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	75
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2138asdfp-30

Table 1.2 Specifications (2)

Item	Function	Description
Serial interface	UART0_0 and UART0_1	2 channels Clock synchronous serial I/O mode, clock asynchronous serial I/O mode
	UART2	1 channel Clock synchronous serial I/O mode, clock asynchronous serial I/O mode, I^2C mode (I^2C-bus), multiprocessor communication mode
Clock Synchronous serial interface	(SSU) SSU_0	1 channel (also used for the I^2C bus)
	(I^2C bus) I^2C_0	1 channel (also used for the SSU)
LIN module	HW-LIN_0	Hardware LIN 1 channel (timer RJ_0, UART0_0, or UART0_1 used)
A/D converter		Resolution: 10 bits × 20 channels, sample and hold function, sweep mode
Comparator B		2 circuits
Touch sensor control unit (TSCU)		System CH × 4, electrostatic capacitive touch detection × 36
CRC calculator		CRC-CCITT ($X^{16} + X^{12} + X^5 + 1$), CRC-16 ($X^{16} + X^{15} + X^2 + 1$) compliant
Flash memory		• Program/erase voltage: VCC = 2.7 V to 5.5 V • Program/erase endurance: 10,000 times (data flash) 1,000 times (program ROM) • Program security: ROM code protect, ID code check • Debug functions: On-chip debug, on-board flash rewrite function • BGO (background operation) function (data flash)
Operating frequency/ Power supply voltage		CPU clock = 20 MHz (VCC = 2.7 V to 5.5 V) CPU clock = 5 MHz (VCC = 1.8 V to 5.5 V)
Current consumption		Typ. 6.5 mA (VCC = 5.0 V, f(XIN) = 20 MHz) Typ. 3.5 mA (VCC = 3.0 V, f(XIN) = 10 MHz) Typ. 4.0 μA (VCC = 3.0 V, wait mode f(XCIN) = 32 kHz) Typ. 2.2 μA (VCC = 3.0 V, stop mode)
Operating ambient temperature		-20°C to 85°C (N version) -40°C to 85°C (D version) (1)
Package		80-pin LQFP Package code: PLQP0080KB-A (previous code: 80P6Q-A)

Note:
1. Specify the D version if it is to be used.

1.2 Product List

Table 1.3 lists product information. Figure 1.1 shows the Product Part Number Structure.

Table 1.3 Product List **Current of Dec 2011**

Part No.	Internal ROM Capacity		Internal RAM Capacity	Package Type	Remarks
	Program ROM	Data Flash			
R5F21388SNFP	64 Kbytes	1 Kbyte × 4	6 Kbytes	PLQP0080KB-A	N version
R5F2138ASNFP	96 Kbytes		8 Kbytes		
R5F2138CSNFP	128 Kbytes		10 Kbytes		
R5F21388SDFP	64 Kbytes		6 Kbytes	PLQP0080KB-A	D version
R5F2138ASDFP	96 Kbytes		8 Kbytes		
R5F2138CSDFP	128 Kbytes		10 Kbytes		

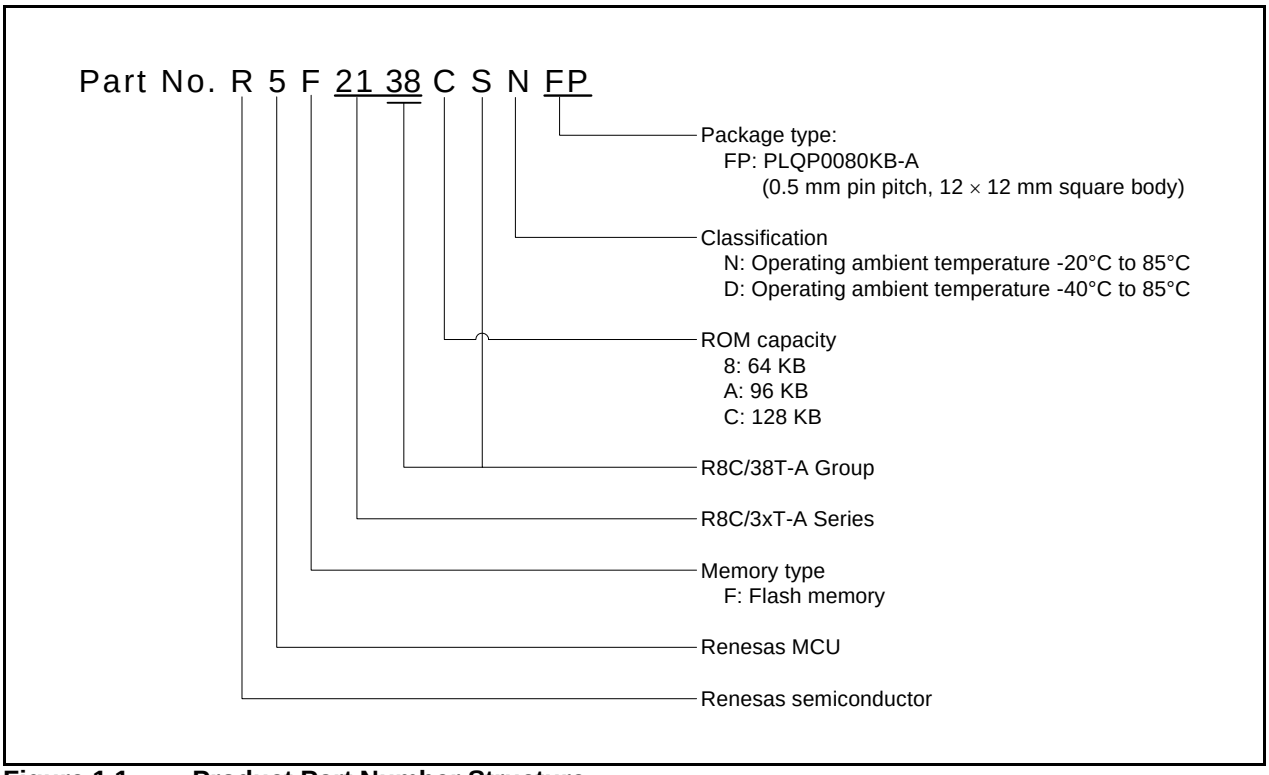

Figure 1.1 Product Part Number Structure

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

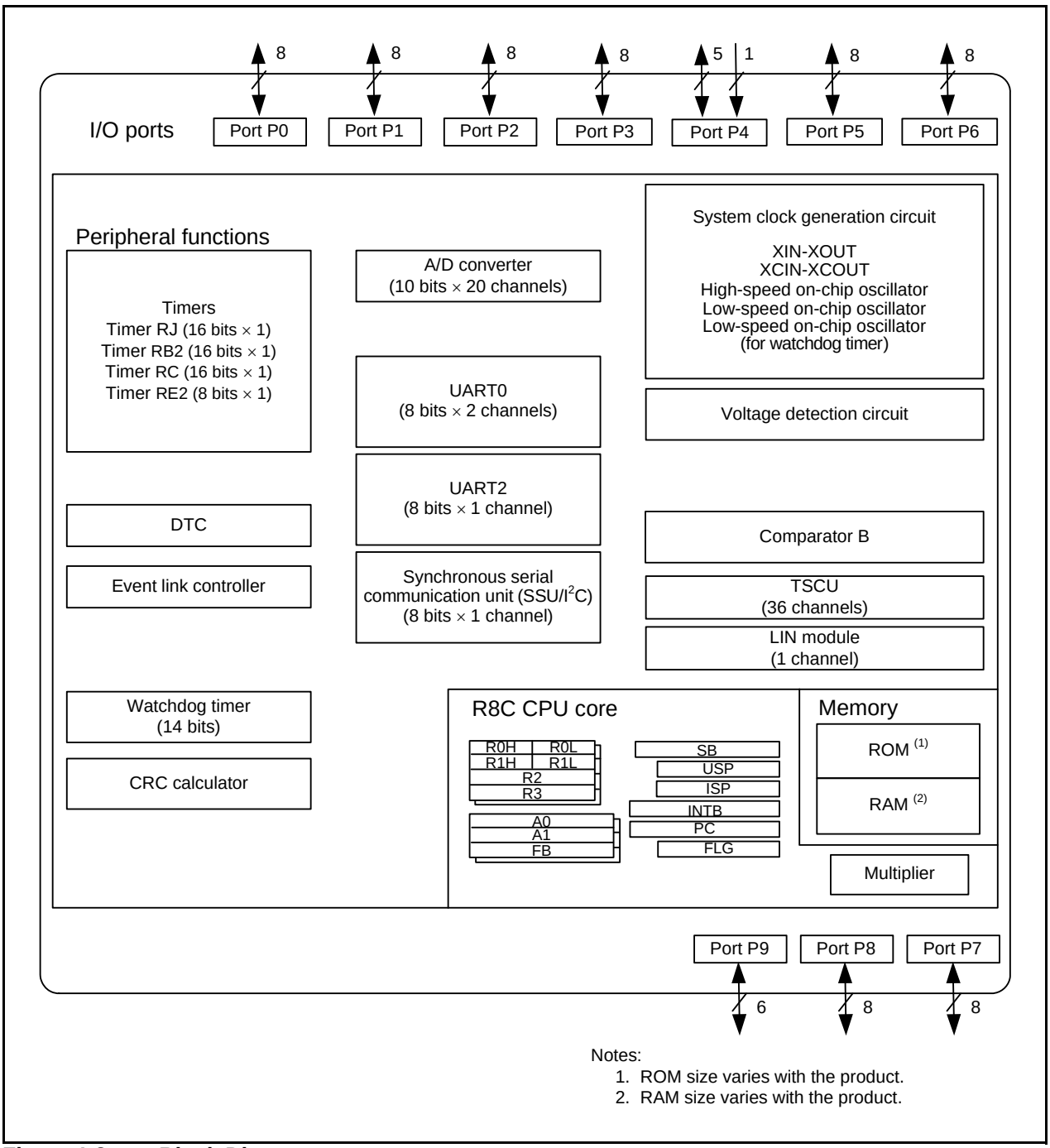

Figure 1.2 Block Diagram

Table 1.4 Pin Name Information by Pin Number (INT, URAT0, and UART2) (1)

Port	Pin No.	INT					UART0						UART2						
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	SDA2	SCL2	CLK2
P0_0	72																		
P0_1	71							TXD_1											
P0_2	70									RXD_1									
P0_3	69											CLK_1							
P0_4	68																		
P0_5	67																		
P0_6	66																		
P0_7	65																		
P1_0	56																		
P1_1	55																		
P1_2	54																		
P1_3	53																		
P1_4	52						TXD_0												
P1_5	51		$\overline{INT1}$						RXD_0										
P1_6	50										CLK_0								
P1_7	49		$\overline{INT1}$																
P2_0	30		$\overline{INT1}$																
P2_1	29																		
P2_2	28																		
P2_3	27																		
P2_4	26																		
P2_5	25																		
P2_6	24																		
P2_7	23																		
P3_0	4																		
P3_1	36																		
P3_2	3		$\overline{INT1}$	$\overline{INT2}$															
P3_3	22				$\overline{INT3}$										$\overline{CTS2}$	$\overline{RTS2}$			
P3_4	21												TXD2	RXD2			SDA2	SCL2	
P3_5	20																		CLK2
P3_6	35																		
P3_7	19												TXD2	RXD2			SDA2	SCL2	
P4_2	5																		
P4_3	7																		
P4_4	8																		
P4_5	48	$\overline{INT0}$												RXD2				SCL2	
P4_6	12																		
P4_7	10																		
P5_0	18																		
P5_1	17																		
P5_2	16																		
P5_3	15																		
P5_4	14																		
P5_5	2																		
P5_6	1																		
P5_7	80																		
P6_0	77																		
P6_1	76																		
P6_2	75											CLK_1							
P6_3	74							TXD_1											
P6_4	73									RXD_1									
P6_5	47					$\overline{INT4}$						CLK_1							CLK2
P6_6	46			$\overline{INT2}$									TXD2				SDA2		
P6_7	45				$\overline{INT3}$														
P7_0	64																		
P7_1	63																		
P7_2	62																		
P7_3	61																		
P7_4	60																		
P7_5	59																		
P7_6	58																		
P7_7	57																		

Table 1.6 Pin Name Information by Pin Number (SSU/I²C, Timer RJ, and Timer RB2) (1)

Port	Pin No.	SSU/I²C						Timer RJ		Timer RB2
		SCL_0	SDA_0	SSI_0	$\overline{SCS\_0}$	SSCK_0	SSO_0	TRJO_0	TRJIO_0	TRBO_0
P0_0	72									
P0_1	71									
P0_2	70									
P0_3	69									
P0_4	68									
P0_5	67									
P0_6	66									
P0_7	65									
P1_0	56									
P1_1	55									
P1_2	54									
P1_3	53									TRBO_0
P1_4	52									
P1_5	51								TRJIO_0	
P1_6	50									
P1_7	49									
P2_0	30									
P2_1	29									
P2_2	28									
P2_3	27									
P2_4	26									
P2_5	25									
P2_6	24									
P2_7	23									
P3_0	4							TRJO_0		
P3_1	36									
P3_2	3								TRJIO_0	
P3_3	22				$\overline{SCS\_0}$					
P3_4	21			SSI_0						
P3_5	20	SCL_0				SSCK_0				
P3_6	35									
P3_7	19		SDA_0				SSO_0			
P4_2	5									
P4_3	7									
P4_4	8									
P4_5	48									
P4_6	12									
P4_7	10									
P5_0	18									
P5_1	17									
P5_2	16									
P5_3	15									
P5_4	14									
P5_5	2								TRJIO_0	
P5_6	1									
P5_7	80									
P6_0	77									
P6_1	76									
P6_2	75									
P6_3	74									
P6_4	73									
P6_5	47									
P6_6	46									
P6_7	45									
P7_0	64									
P7_1	63									
P7_2	62									
P7_3	61									
P7_4	60									
P7_5	59									
P7_6	58									
P7_7	57									

Table 1.9 Pin Name Information by Pin Number (Timer RC, Timer RE2, and Others) (2)

Port	Pin No.	Timer RC						Timer RE2	Others		
		TRCCLK_0	TRCIOA_0	TRCIOB_0	TRCIOC_0	TRCIOD_0	TRCTRG_0	TMRE2O			
P8_0	44										CH06
P8_1	43										CH07
P8_2	42										CHxA0
P8_3	41										CHxA1
P8_4	40										CHxB
P8_5	39										CHxC
P8_6	38										CH08
P8_7	37										CH09
P9_0	34										CH12
P9_1	33										CH13
P9_2	32										CH14
P9_3	31										CH15
P9_4	79										CH29
P9_5	78										CH30

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

2.8.7 Interrupt Enable Flag (I)

The I flag enables maskable interrupts. Interrupts are disabled when the I flag is 0, and are enabled when the I flag is 1. The I flag is set to 0 when an interrupt request is acknowledged.

2.8.8 Stack Pointer Select Flag (U)

ISP is selected when the U flag is 0. USP is selected when the U flag is 1. The U flag is set to 0 when a hardware interrupt request is acknowledged or the INT instruction for a software interrupt numbered from 0 to 31 is executed.

2.8.9 Processor Interrupt Priority Level (IPL)

IPL is 3 bits wide and assigns eight processor interrupt priority levels from 0 to 7. If a requested interrupt has higher priority than IPL, the interrupt is enabled.

2.8.10 Reserved Bit

The write value must be 0. The read value is undefined.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h				
00159h				
0015Ah				
0015Bh				
0015Ch				
0015Dh				
0015Eh				
0015Fh				
00160h				
00161h				
00162h				
00163h				
00164h				
00165h				
00166h				
00167h				
00168h				
00169h				
0016Ah				
0016Bh				
0016Ch				
0016Dh				
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register Timer RE2 Second Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register Timer RE2 Minute Data Register	00h	
00172h	TREHR	Timer RE2 Hour Data Register	00h	
00173h	TREWK	Timer RE2 Day-of-the-Week Data Register	00h	
00174h	TREDY	Timer RE2 Day Data Register	00000001b	
00175h	TREMON	Timer RE2 Month Data Register	00000001b	
00176h	TREYR	Timer RE2 Year Data Register	00h	
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h	TREADJ	Timer RE2 Clock Error Correction Register	00h	

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.10 SFR Information (10) (1)

Address	Symbol	Register Name	After Reset	Remarks
002C0h	PUR0	Pull-Up Control Register 0	00h	
002C1h	PUR1	Pull-Up Control Register 1	00h	
002C2h	PUR2	Pull-Up Control Register 2	00h	
002C3h				
002C4h				
002C5h				
002C6h				
002C7h				
002C8h	P1DRR	Port P1 Drive Capacity Control Register	00h	
002C9h	P2DRR	Port P2 Drive Capacity Control Register	00h	
002CAh				
002CBh				
002CCh	DRR0	Drive Capacity Control Register 0	00h	
002CDh	DRR1	Drive Capacity Control Register 1	00h	
002CEh	DRR2	Drive Capacity Control Register 2	00h	
002CFh				
002D0h	VLT0	Input Threshold Control Register 0	00h	
002D1h	VLT1	Input Threshold Control Register 1	00h	
002D2h	VLT2	Input Threshold Control Register 2	00h	
002D3h				
002D4h				
002D5h				
002D6h				
002D7h				
002D8h				
002D9h				
002DAh				
002DBh				
002DCh				
002DDh				
002DEh				
002DFh				
002E0h	PORT0	Port P0 Register	XXh	
002E1h	PORT1	Port P1 Register	XXh	
002E2h	PD0	Port P0 Direction Register	00h	
002E3h	PD1	Port P1 Direction Register	00h	
002E4h	PORT2	Port P2 Register	XXh	
002E5h	PORT3	Port P3 Register	XXh	
002E6h	PD2	Port P2 Direction Register	00h	
002E7h	PD3	Port P3 Direction Register	00h	
002E8h	PORT4	Port P4 Register	XXh	
002E9h	PORT5	Port P5 Register	XXh	
002EAh	PD4	Port P4 Direction Register	00h	
002EBh	PD5	Port P5 Direction Register	00h	
002ECh	PORT6	Port P6 Register	XXh	
002EDh	PORT7	Port P7 Register	XXh	
002EEh	PD6	Port P6 Direction Register	00h	
002EFh	PD7	Port P7 Direction Register	00h	
002F0h	PORT8	Port P8 Register	XXh	
002F1h	PORT9	Port P9 Register	XXh	
002F2h	PD8	Port P8 Direction Register	00h	
002F3h	PD9	Port P9 Direction Register	00h	
002F4h				
002F5h				
002F6h				
002F7h				
002F8h				
002F9h				
002FAh				
002FBh				
002FCh				
002FDh				
002FEh				
002FFh				
00300h to 003FFh				

Note:
1. The blank areas are reserved. No access is allowed.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
Vcc/AVcc ICEVcc	Supply voltage		–0.3 to 6.5	V
V_I	Input voltage		–0.3 to Vcc + 0.3	V
V_O	Output voltage		–0.3 to Vcc + 0.3	V
P_d	Power dissipation	–40°C ≤ Topr ≤ 85°C	500	mW
T_{opr}	Operating ambient temperature		–20 to 85 (N version)/ –40 to 85 (D version)	°C
T_{stg}	Storage temperature		–65 to 150	°C

4.3 Peripheral Function Characteristics

Table 4.3 A/D Converter Characteristics
(Vcc/AVcc = Vref = 2.2 V to 5.5 V, Vss = 0 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
—	Resolution		V_{ref} = AVcc		—	—	10	Bit
—	Absolute accuracy	10-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN19 input	—	—	±3	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN19 input	—	—	±5	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN19 input	—	—	±5	LSB
			V_{ref} = AVcc = 2.2 V	AN0 to AN19 input	—	—	±5	LSB
		8-bit mode	V_{ref} = AVcc = 5.0 V	AN0 to AN19 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.3 V	AN0 to AN19 input	—	—	±2	LSB
			V_{ref} = AVcc = 3.0 V	AN0 to AN19 input	—	—	±2	LSB
			V_{ref} = AVcc = 2.2 V	AN0 to AN19 input	—	—	±2	LSB
ϕAD	A/D conversion clock		4.0 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	20	MHz
			3.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	16	MHz
			2.7 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	10	MHz
			2.2 V ≤ V_{ref} = AVcc ≤ 5.5 V (1)		2	—	5	MHz
—	Tolerance level impedance				—	3	—	kΩ
I_{vref}	Vref current		Vcc = 5 V, XIN = f1 = fAD = 20 MHz		—	45	—	µA
t_{CONV}	Conversion time	10-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
		8-bit mode	V_{ref} = AVcc = 5.0 V, ϕAD = 20 MHz		2.2	—	—	µs
t_{SAMP}	Sampling time		ϕAD = 20 MHz		0.8	—	—	µs
V_{ref}	Reference voltage				2.2	—	AVcc	V
V_{IA}	Analog input voltage (2)				0	—	V_{ref}	V
OCVREF	On-chip reference voltage		2MHz ≤ ϕAD ≤ 4MHz		1.19	1.34	1.49	V

Notes:
1. If the CPU and the flash memory stop, the A/D conversion result will be undefined.
2. When the analog input voltage exceeds the reference voltage, the A/D conversion result will be 3FFh in 10-bit mode and FFh in 8-bit mode.

Table 4.4 Comparator B Characteristics
(Vcc/AVcc = 2.2 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{ref}	IVREF1, IVREF3 input reference voltage		0	—	Vcc – 1.4	V
V_I	IVCMP1, IVCMP3 input voltage		–0.3	—	Vcc + 0.3	V
—	Offset		—	5	100	mV
t_d	Comparator output delay time (1)	V_I = V_{ref} ±100 mV	—	0.1	—	µs
I_{CMP}	Comparator operating current	Vcc = 5.0 V	—	17.5	—	µA

Note:
1. When the digital filter is not selected.

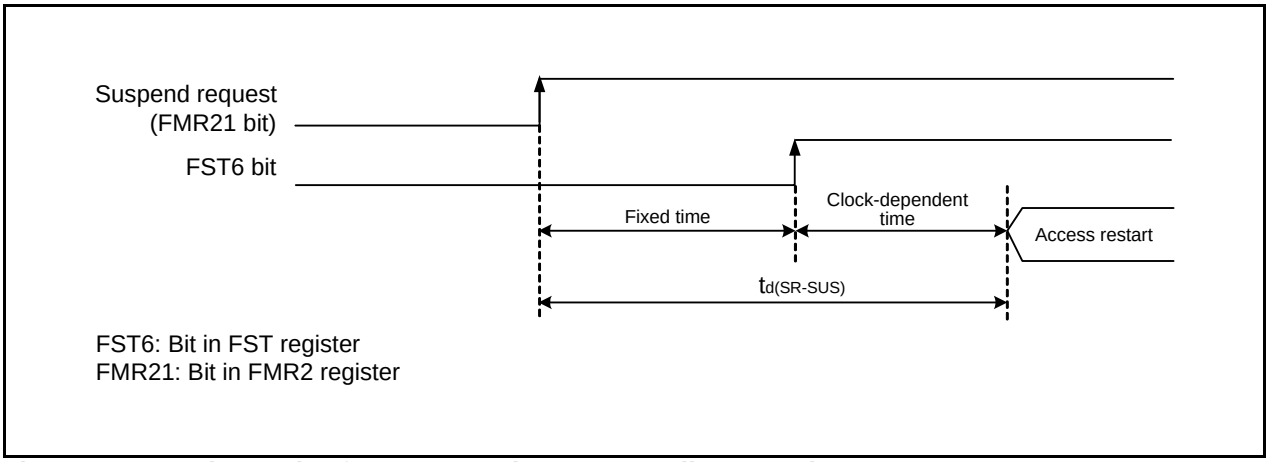

Figure 4.2 Time Delay from Suspend Request until Suspend

Table 4.7 Voltage Detection 0 Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
V_{det0}	Voltage detection level Vdet0_0 (1)	When Vcc falls	1.80	1.90	2.05	V
	Voltage detection level Vdet0_1 (1)	When Vcc falls	2.15	2.35	2.55	V
	Voltage detection level Vdet0_2 (1)	When Vcc falls	2.70	2.85	3.05	V
	Voltage detection level Vdet0_3 (1)	When Vcc falls	3.55	3.80	4.05	V
—	Voltage detection 0 circuit response time (2)	At the falling of Vcc from 5 V to (Vdet0 – 0.1) V	—	6	150	µs
—	Voltage detection circuit self power consumption	VCA25 = 1, Vcc = 5.0 V	—	1.5	—	µA
$t_{d(E-A)}$	Waiting time until voltage detection circuit operation starts (3)		—	—	100	µs

Notes:
1. The voltage detection level must be selected with bits VDSEL0 and VDSEL1 in the OFS register.
2. Time until the voltage monitor 0 reset is generated after the voltage passes V_{det0}.
3. Necessary time until the voltage detection circuit operates when setting to 1 again after setting the VCA25 bit in the VCA2 register to 0.

Table 4.12 Low-Speed On-Chip Oscillator Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	3	—	µA

Table 4.13 Power Supply Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (1)		—	—	2,000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

4.4 DC Characteristics

Table 4.14 DC Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V] (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –20 mA	Vcc – 2.0	—	Vcc	V
			Drive capacity is low	I_{OH} = –5 mA	Vcc – 2.0	—	Vcc	V
				I_{OH} = –200 µA	Vcc – 0.3	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL}= 20 mA	—	—	2.0	V
			Drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
				I_{OL} = 200 µA	—	—	0.45	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, $\overline{RXD\_0}$, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5.0 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Table 4.16 DC Characteristics (3) [2.7 V ≤ Vcc < 4.2 V] (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3.0 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

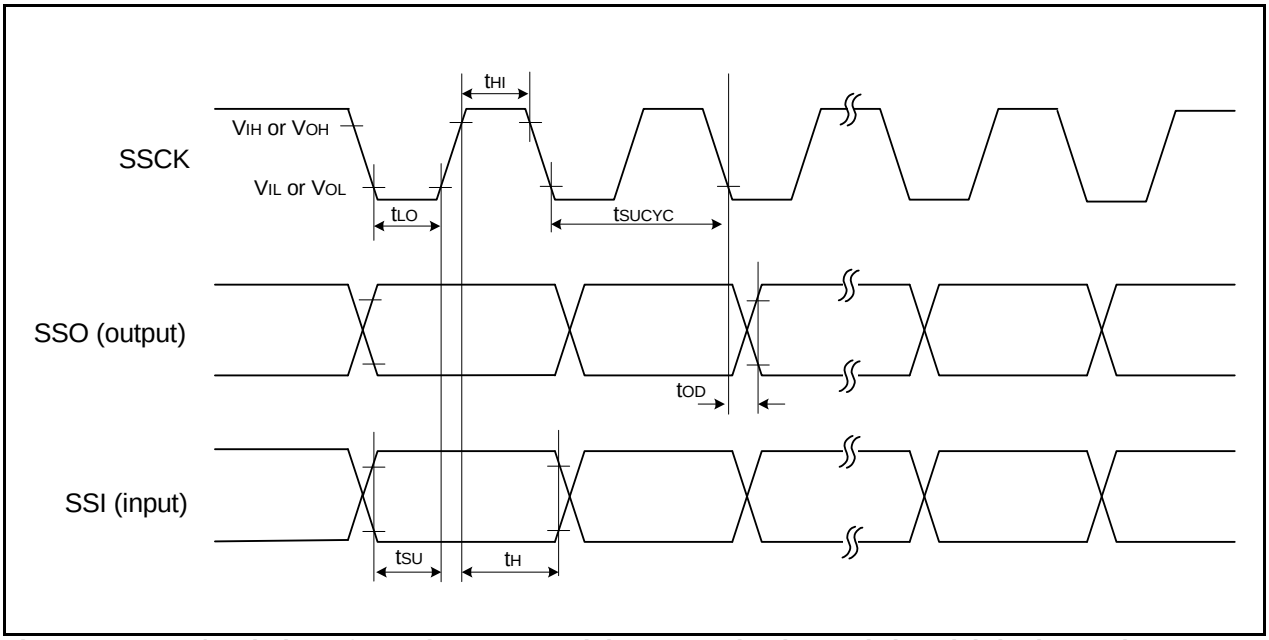

Figure 4.6 I/O Timing of Synchronous Serial Communication Unit (SSU) (Clock Synchronous Communication Mode)

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

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