Renesas Electronics America Inc - R5F2138ASNFP#30 Datasheet

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I²C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	75
Program Memory Size	96KB (96K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2138asnfp-30

1.3 Block Diagram

Figure 1.2 shows the Block Diagram.

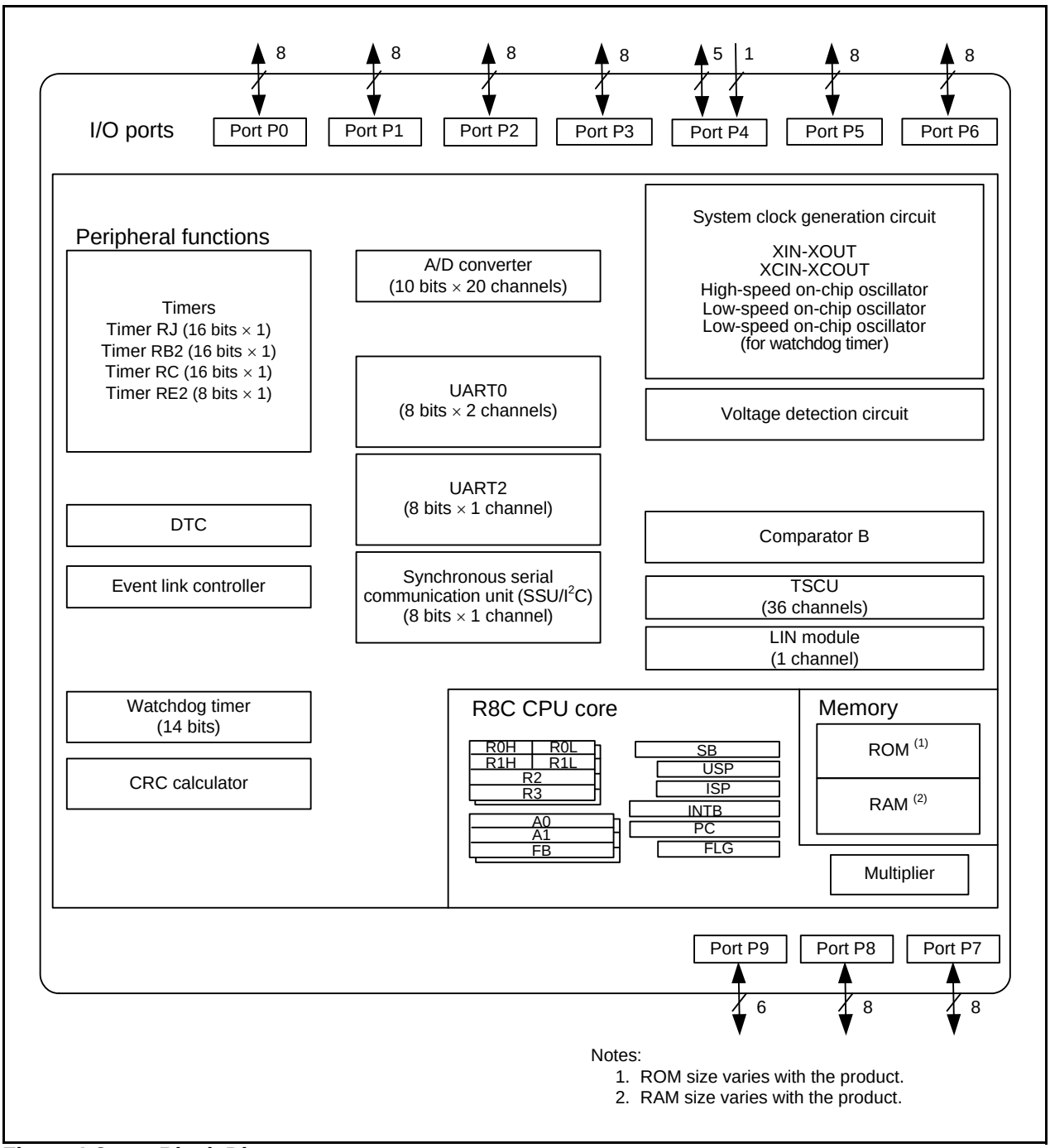


Figure 1.2 Block Diagram

1.4 Pin Assignment

Figure 1.3 shows Pin Assignment (Top View). Tables 1.4 to 1.9 list the Pin Name Information by Pin Number.

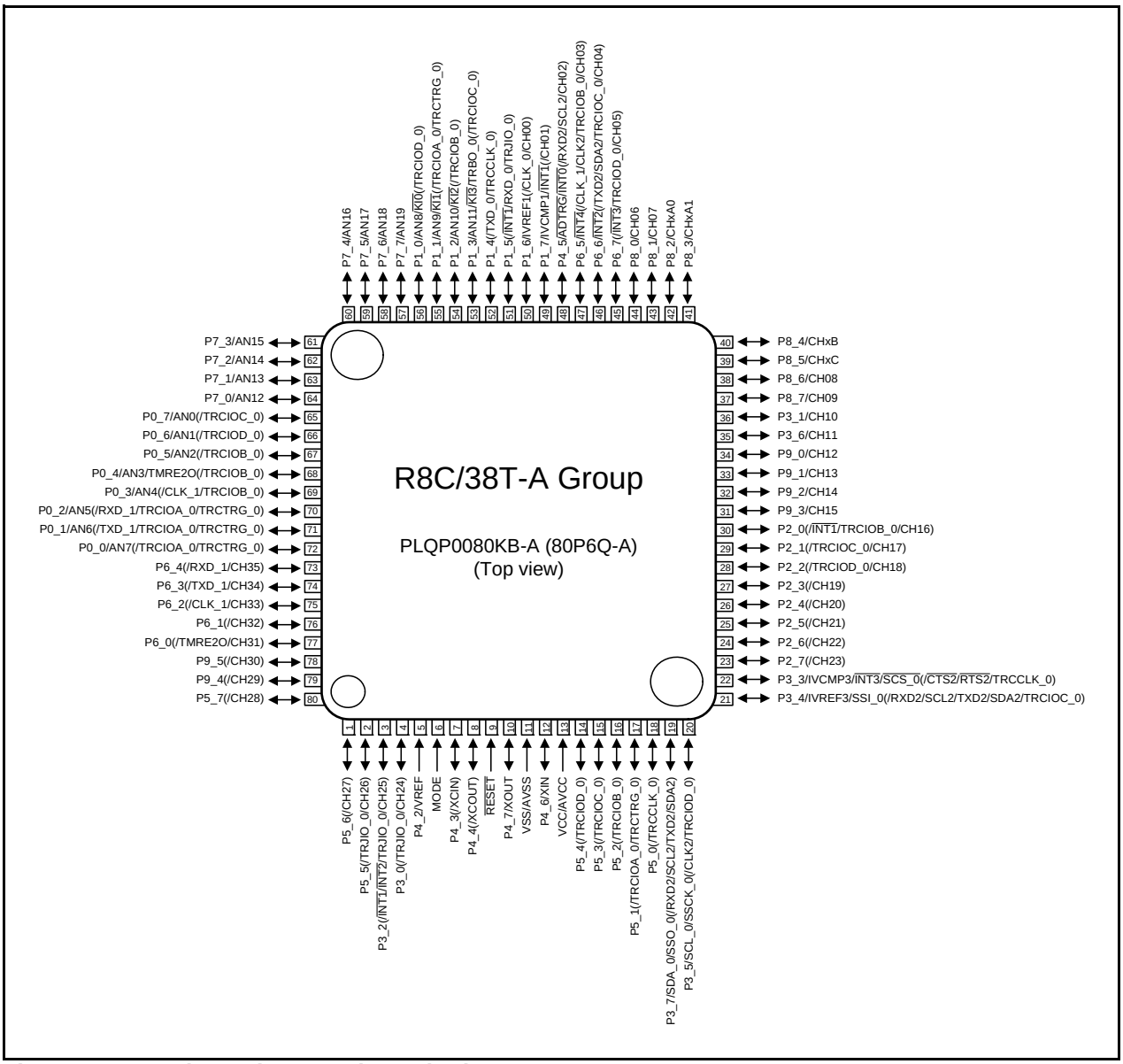


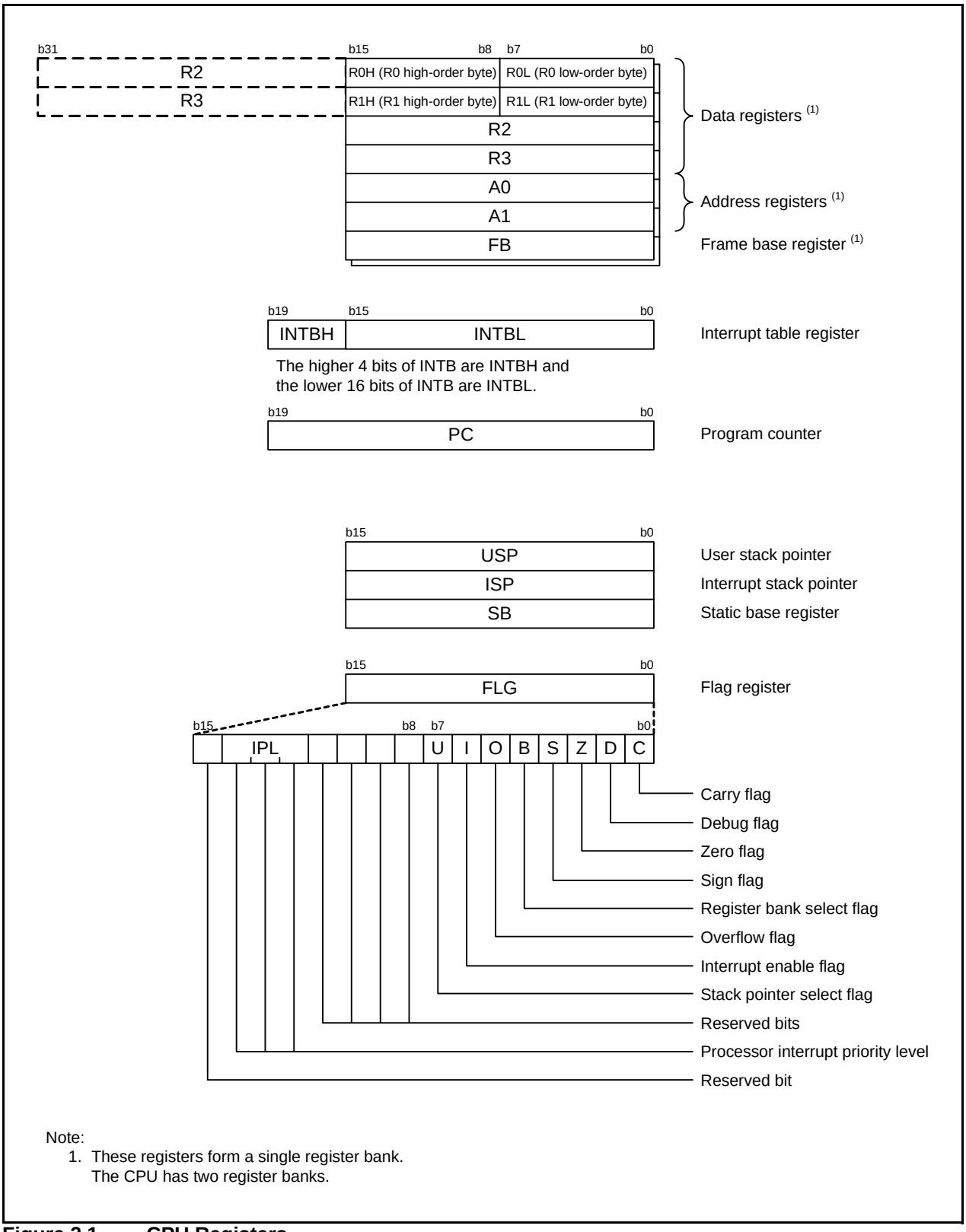
Figure 1.3 Pin Assignment (Top View)

Table 1.5 Pin Name Information by Pin Number (INT, URAT0, and UART2) (2)

Port	Pin No.	INT					UART0						UART2						
		$\overline{INT0}$	$\overline{INT1}$	$\overline{INT2}$	$\overline{INT3}$	$\overline{INT4}$	TXD_0	TXD_1	RXD_0	RXD_1	CLK_0	CLK_1	TXD2	RXD2	$\overline{CTS2}$	$\overline{RTS2}$	SDA2	SCL2	CLK2
P8_0	44																		
P8_1	43																		
P8_2	42																		
P8_3	41																		
P8_4	40																		
P8_5	39																		
P8_6	38																		
P8_7	37																		
P9_0	34																		
P9_1	33																		
P9_2	32																		
P9_3	31																		
P9_4	79																		
P9_5	78																		

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.



Note:
1. These registers form a single register bank.
The CPU has two register banks.

Figure 2.1 CPU Registers

2.1 Data Registers (R0, R1, R2, and R3)

R0 is a 16-bit register for transfer, arithmetic, and logic operations. The same applies to R1 through R3. R0 can be split into high-order (R0H) and low-order (R0L) registers to be used separately as 8-bit data registers. The same applies to R1H and R1L. R2 can be combined with R0 and used as a 32-bit data register (R2R0). Similarly, R3 and R1 can be used as a 32-bit data register.

2.2 Address Registers (A0 and A1)

A0 is a 16-bit register for address register indirect addressing and address register relative addressing. It is also used for transfer, arithmetic, and logic operations. A1 functions in the same manner as A0. A1 can be combined with A0 and used as a 32-bit address register (A1A0).

2.3 Frame Base Register (FB)

FB is a 16-bit register used for FB relative addressing.

2.4 Interrupt Table Register (INTB)

INTB is a 20-bit register that indicates the start address of a relocatable interrupt vector table.

2.5 Program Counter (PC)

PC is a 20-bit register that indicates the address of the next instruction to be executed.

2.6 User Stack Pointer (USP) and Interrupt Stack Pointer (ISP)

The stack pointers (SP), USP and ISP, are each 16 bits wide. The U flag of the FLG register is used to switch between USP and ISP.

2.7 Static Base Register (SB)

SB is a 16-bit register used for SB relative addressing.

2.8 Flag Register (FLG)

FLG is an 11-bit register that indicates the CPU state.

2.8.1 Carry Flag (C)

The C flag retains carry, borrow, or shift-out bits that have been generated in the arithmetic and logic unit.

2.8.2 Debug Flag (D)

The D flag is for debugging only. It must only be set to 0.

2.8.3 Zero Flag (Z)

The Z flag is set to 1 when an arithmetic operation results in 0. Otherwise it is set to 0.

2.8.4 Sign Flag (S)

The S flag is set to 1 when an arithmetic operation results in a negative value. Otherwise it is set to 0.

2.8.5 Register Bank Select Flag (B)

Register bank 0 is selected when the B flag is 0. Register bank 1 is selected when this flag is 1.

2.8.6 Overflow Flag (O)

The O flag is set to 1 when an operation results in an overflow. Otherwise it is set to 0.

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRE_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:
1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Symbol	Register Name	After Reset	Remarks
0023Ah	MSTCR2	Module Standby Control Register 2	00h	
0023Bh	MSTCR3	Module Standby Control Register 3	00h	
0023Ch	MSTCR4	Module Standby Control Register 4	00h	
0023Dh				
0023Eh				
0023Fh				
00240h				
00241h				
00242h				
00243h				
00244h				
00245h				
00246h				
00247h				
00248h				
00249h				
0024Ah				
0024Bh				
0024Ch				
0024Dh				
0024Eh				
0024Fh				
00250h				
00251h				
00252h	FST	Flash Memory Status Register	10000X00b	
00253h				
00254h	FMR0	Flash Memory Control Register 0	00h	
00255h	FMR1	Flash Memory Control Register 1	00h	
00256h	FMR2	Flash Memory Control Register 2	00h	
00257h				
00258h				
00259h				
0025Ah				
0025Bh				
0025Ch				
0025Dh				
0025Eh				
0025Fh				
00260h	AIADR0L	Address Match Interrupt Address 0L Register	XXXXh	
00261h				
00262h	AIADR0H	Address Match Interrupt Address 0H Register	0000XXXXb	
00263h	AIEN0	Address Match Interrupt Enable 0 Register	00h	
00264h	AIADR1L	Address Match Interrupt Address 1L Register	XXXXh	
00265h				
00266h	AIADR1H	Address Match Interrupt Address 1H Register	0000XXXXb	
00267h	AIEN1	Address Match Interrupt Enable 1 Register	00h	
00268h				
00269h				
0026Ah				
0026Bh				
0026Ch				
0026Dh				
0026Eh				
0026Fh				
00270h				
00271h				
00272h				
00273h				
00274h				
00275h				
00276h				
00277h				
00278h				
00279h				
0027Ah				
0027Bh				
0027Ch				
0027Dh				
0027Eh				
0027Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.12 SFR Information (12) (1)

Address	Symbol	Register Name	After Reset	Remarks
06B00h	TSCUCR0	TSCU Control Register 0	0000h	
06B01h				
06B02h	TSCUCR1	TSCU Control Register 1	0000000000010000b	
06B03h				
06B04h	TSCUMR	TSCU Mode Register	0000000010000000b	
06B05h				
06B06h	TSCUTCR0A	TSCU Timing Control Register 0A	0000000001111111b	
06B07h				
06B08h	TSCUTCR0B	TSCU Timing Control Register 0B	0000000001111111b	
06B09h				
06B0Ah	TSCUTCR1	TSCU Timing Control Register 1	0000000000000001b	
06B0Bh				
06B0Ch	TSCUTCR2	TSCU Timing Control Register 2	0000h	
06B0Dh				
06B0Eh	TSCUTCR3	TSCU Timing Control Register 3	0000h	
06B0Fh				
06B10h	TSCUCHC	TSCU Channel Control Register	0011111100000000b	
06B11h				
06B12h	TSCUFR	TSCU Flag Register	0000h	
06B13h				
06B14h	TSCUSTC	TSCU Status Counter Register	0000h	
06B15h				
06B16h	TSCUSCS	TSCU Secondary Counter Set Register	0000000000100000b	
06B17h				
06B18h	TSCUSCC	TSCU Secondary Counter	0000000000100000b	
06B19h				
06B1Ah	TSCUDBR	TSCU Data Buffer Register	0000h	
06B1Bh				
06B1Ch	TSCUPRC	TSCU Primary Counter	0000h	
06B1Dh				
06B1Eh	TSCURVR0	TSCU Random Value Store Register 0	0000h	
06B1Fh				
06B20h	TSCURVR1	TSCU Random Value Store Register 1	0000h	
06B21h				
06B22h	TSCURVR2	TSCU Random Value Store Register 2	0000h	
06B23h				
06B24h	TSCURVR3	TSCU Random Value Store Register 3	0000h	
06B25h				
06B26h	TSIE0	TSCU Input Enable Register 0	0000h	
06B27h				
06B28h	TSIE1	TSCU Input Enable Register 1	0000h	
06B29h				
06B2Ah	TSIE2	TSCU Input Enable Register 2	0000h	
06B2Bh				
06B2Ch	TSCHSEL0	TSCUCHXA Select Register 0	0000h	
06B2Dh				
06B2Eh	TSCHSEL1	TSCUCHXA Select Register 1	0000h	
06B2Fh				
06B30h	TSCHSEL2	TSCUCHXA Select Register 2	0000h	
06B31h				
06B32h to 06BFFh				
06C00h		Area for storing DTC transfer vector 0	XXh	
06C01h		Area for storing DTC transfer vector 1	XXh	
06C02h		Area for storing DTC transfer vector 2	XXh	
06C03h		Area for storing DTC transfer vector 3	XXh	
06C04h		Area for storing DTC transfer vector 4	XXh	
06C05h				
06C06h				
06C07h				
06C08h		Area for storing DTC transfer vector 8	XXh	
06C09h		Area for storing DTC transfer vector 9	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.16 SFR Information (16) (1)

Address	Symbol	Register Name	After Reset	Remarks
06CD0h	DTCCR18	DTC Control Register 18	XXh	
06CD1h	DTBLS18	DTC Block Size Register 18	XXh	
06CD2h	DTCCT18	DTC Transfer Count Register 18	XXh	
06CD3h	DTRLD18	DTC Transfer Count Reload Register 18	XXh	
06CD4h	DTSAR18	DTC Source Address Register 18	XXXXh	
06CD5h				
06CD6h	DTDAR18	DTC Destination Address Register 18	XXXXh	
06CD7h				
06CD8h	DTCCR19	DTC Control Register 19	XXh	
06CD9h	DTBLS19	DTC Block Size Register 19	XXh	
06CDAh	DTCCT19	DTC Transfer Count Register 19	XXh	
06CDBh	DTRLD19	DTC Transfer Count Reload Register 19	XXh	
06CDCh	DTSAR19	DTC Source Address Register 19	XXXXh	
06CDDh				
06CDEh	DTDAR19	DTC Destination Address Register 19	XXXXh	
06CDFh				
06CE0h	DTCCR20	DTC Control Register 20	XXh	
06CE1h	DTBLS20	DTC Block Size Register 20	XXh	
06CE2h	DTCCT20	DTC Transfer Count Register 20	XXh	
06CE3h	DTRLD20	DTC Transfer Count Reload Register 20	XXh	
06CE4h	DTSAR20	DTC Source Address Register 20	XXXXh	
06CE5h				
06CE6h	DTDAR20	DTC Destination Address Register 20	XXXXh	
06CE7h				
06CE8h	DTCCR21	DTC Control Register 21	XXh	
06CE9h	DTBLS21	DTC Block Size Register 21	XXh	
06CEAh	DTCCT21	DTC Transfer Count Register 21	XXh	
06CEBh	DTRLD21	DTC Transfer Count Reload Register 21	XXh	
06CECh	DTSAR21	DTC Source Address Register 21	XXXXh	
06CEDh				
06CEEh	DTDAR21	DTC Destination Address Register 21	XXXXh	
06CEFh				
06CF0h	DTCCR22	DTC Control Register 22	XXh	
06CF1h	DTBLS22	DTC Block Size Register 22	XXh	
06CF2h	DTCCT22	DTC Transfer Count Register 22	XXh	
06CF3h	DTRLD22	DTC Transfer Count Reload Register 22	XXh	
06CF4h	DTSAR22	DTC Source Address Register 22	XXXXh	
06CF5h				
06CF6h	DTDAR22	DTC Destination Address Register 22	XXXXh	
06CF7h				
06CF8h	DTCCR23	DTC Control Register 23	XXh	
06CF9h	DTBLS23	DTC Block Size Register 23	XXh	
06CFAh	DTCCT23	DTC Transfer Count Register 23	XXh	
06CFBh	DTRLD23	DTC Transfer Count Reload Register 23	XXh	
06CFCh	DTSAR23	DTC Source Address Register 23	XXXXh	
06CFDh				
06CFEh	DTDAR23	DTC Destination Address Register 23	XXXXh	
06CFFh				
06D00h to 06FFFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 4.5 Flash Memory (Program ROM) Characteristics (Vcc = 2.7 V to 5.5 V, Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	Program/erase endurance (1)		1,000 (2)	—	—	times
—	Byte program time (Program and erase endurance ≤ 100 times)		—	—	—	µs
—	Byte program time (Program and erase endurance ≤ 1,000 times)		—	—	—	µs
—	Word program time (Program and erase endurance ≤ 100 times)	Topr = 25°C, Vcc = 5.0 V	—	100	200	µs
—	Word program time (Program and erase endurance ≤ 100 times)		—	100	400	µs
—	Word program time (Program and erase endurance ≤ 1,000 times)		—	100	650	µs
—	Block erase time		—	0.3	4	s
$t_{d(SR-SUS)}$	Time delay from suspend request until suspend		—	—	5 + CPU clock × 3 cycles	ms
—	Interval from erase start/restart until following suspend request		0	—	—	µs
—	Time from suspend until erase restart		—	—	30 + CPU clock × 1 cycle	µs
$t_{d(CMDRST-READY)}$	Time from when command is forcibly terminated until reading is enabled		—	—	30 + CPU clock × 1 cycle	µs
—	Program, erase voltage		2.7	—	5.5	V
—	Read voltage		1.8	—	5.5	V
—	Program, erase temperature		–20 (N ver.) –40 (D ver.)	—	85	°C
—	Data hold time (6)	Ambient temperature = 55°C (7)	20	—	—	year

Notes:
1. Definition of programming/erasure endurance
   The programming and erasure endurance is defined on a per-block basis.
   If the programming and erasure endurance is n (n = 100 or 1,000), each block can be erased n times. For example, if 1,024 1-byte writes are performed to different addresses in block A, a 1 Kbyte block, and then the block is erased, the programming/erasure endurance still stands at one.
   However, the same address must not be programmed more than once per erase operation (overwriting prohibited).
2. Endurance to guarantee all electrical characteristics after program and erase. (1 to Min. value can be guaranteed).
3. In a system that executes multiple programming operations, the actual erasure count can be reduced by writing to sequential addresses in turn so that as much of the block as possible is used up before performing an erase operation. For example, when programming groups of 16 bytes, the effective number of rewrites can be minimized by programming up to 128 groups before erasing them all in one operation. It is also advisable to retain data on the erasure endurance of each block and limit the number of erase operations to a certain number.
4. If an error occurs during block erase, attempt to execute the clear status register command, then execute the block erase command at least three times until the erase error does not occur.
5. Customers desiring program/erase failure rate information should contact their Renesas technical support representative.
6. The data hold time includes time that the power supply is off or the clock is not supplied.
7. The data hold time includes 7,000 hours under an environment of ambient temperature 85°C.

Table 4.12 Low-Speed On-Chip Oscillator Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
fLOCO	Low-speed on-chip oscillator frequency		60	125	250	kHz
—	Oscillation stability time	Vcc = 5.0 V, Topr = 25°C	—	30	100	µs
—	Self power consumption at oscillation	Vcc = 5.0 V, Topr = 25°C	—	3	—	µA

Table 4.13 Power Supply Circuit Characteristics (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
$t_{d(P-R)}$	Time for internal power supply stabilization during power-on (1)		—	—	2,000	µs

Note:
1. Waiting time until the internal power supply generation circuit stabilizes during power-on.

4.4 DC Characteristics

Table 4.14 DC Characteristics (1) [4.2 V ≤ Vcc ≤ 5.5 V] (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –20 mA	Vcc – 2.0	—	Vcc	V
			Drive capacity is low	I_{OH} = –5 mA	Vcc – 2.0	—	Vcc	V
				I_{OH} = –200 µA	Vcc – 0.3	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL}= 20 mA	—	—	2.0	V
			Drive capacity is low	I_{OL} = 5 mA	—	—	2.0	V
				I_{OL} = 200 µA	—	—	0.45	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, $\overline{RXD\_0}$, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	1.2	—	V
		$\overline{RESET}$	Vcc = 5.0 V		0.1	1.2	—	V
I_{IH}	Input high current		V_I = 5.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		25	50	100	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Table 4.16 DC Characteristics (3) [2.7 V ≤ Vcc < 4.2 V] (Measurement conditions: Vcc = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/ –40°C to 85°C (D version))

Symbol	Parameter		Conditions		Standard			Unit
					Min.	Typ.	Max.	
V_{OH}	Output high voltage	Other than XOUT	Drive capacity is high	I_{OH} = –5 mA	Vcc – 0.5	—	Vcc	V
			Drive capacity is low	I_{OH} = –1 mA	Vcc – 0.5	—	Vcc	V
		XOUT		I_{OH} = –200 µA	1.0	—	Vcc	V
V_{OL}	Output low voltage	Other than XOUT	Drive capacity is high	I_{OL} = 5 mA	—	—	0.5	V
			Drive capacity is low	I_{OL} = 1 mA	—	—	0.5	V
		XOUT		I_{OL} = 200 µA	—	—	0.5	V
V_{T+}-V_{T-}	Hysteresis	$\overline{INT0}$ to $\overline{INT4}$, $\overline{KI0}$ to $\overline{KI3}$, TRJIO_0, TRCCLK_0, TRCTRG_0, TRCIOA_0, TRCIOB_0, TRCIOC_0, TRCIOD_0, CLK_0, CLK_1, RXD_0, RXD_1, $\overline{CTS2}$, SCL2, SDA2, CLK2, RXD2, $\underline{SCL\_0}$, SDA_0, SSI_0, $\overline{SCS\_0}$, SSCK_0, SSO_0			0.1	0.4	—	V
		$\overline{RESET}$	Vcc = 3.0 V		0.1	0.5	—	V
I_{IH}	Input high current		V_I = 3.0 V		—	—	1.0	µA
I_{IL}	Input low current		V_I = 0 V		—	—	–1.0	µA
R_{PULLUP}	Pull-up resistance		V_I = 0 V		42	84	168	kΩ
R_{fXIN}	Feedback resistance	XIN			—	0.3	—	MΩ
R_{fXCIN}	Feedback resistance	XCIN			—	8	—	MΩ
V_{RAM}	RAM hold voltage		During stop mode		1.8	—	—	V

Table 4.17 DC Characteristics (4) [2.7 V ≤ Vcc < 3.3 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified))

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	10 MHz	Off	Off	125 kHz	No division	—		—	3.5	10	mA
			10 MHz	Off	Off	125 kHz	Divide-by-8	—		—	1.5	7.5	mA
		High-speed on-chip oscillator mode	Off	Off	20 MHz (3)	125 kHz	No division	—		—	7.0	15	mA
			Off	Off	20 MHz (3)	125 kHz	Divide-by-8	—		—	3.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	No division	—		—	4.0	—	mA
			Off	Off	10 MHz (3)	125 kHz	Divide-by-8	—		—	1.5	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	390	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	400	µA
			Off	32 kHz	Off	Off	No division	FMSTP = 1 SVC0 = 0	Program operation on RAM Flash memory off	—	40	—	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6.0	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 2.7 V to 3.3 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 4.19 DC Characteristics (6) [1.8 V ≤ Vcc < 2.7 V] (Topr = –20°C to 85°C (N version)/–40°C to 85°C (D version), unless otherwise specified)

Symbol	Parameter	Conditions								Standard (4)			Unit
			Oscillation		On-Chip Oscillator		CPU Clock	Low-Power-Consumption Setting	Other	Min.	Typ.	Max.	
			XIN (2)	XCIN	High-Speed	Low-Speed							
Icc	Power supply current (1)	High-speed clock mode	5 MHz	Off	Off	125 kHz	No division	—		—	2.2	—	mA
			5 MHz	Off	Off	125 kHz	Divide-by-8	—		—	0.8	—	mA
		High-speed on-chip oscillator mode	Off	Off	5 MHz (3)	125 kHz	No division	—		—	2.5	10	mA
			Off	Off	5 MHz (3)	125 kHz	Divide-by-8	—		—	1.7	—	mA
			Off	Off	4 MHz (3)	125 kHz	Divide-by-16	MSTIIC = 1 MSTTRC = 1		—	1	—	mA
		Low-speed on-chip oscillator mode	Off	Off	Off	125 kHz	Divide-by-8	FMR27 = 1 SVC0 = 0		—	90	300	µA
		Low-speed clock mode	Off	32 kHz	Off	Off	No division	FMR27 = 1 SVC0 = 0		—	80	350	µA
		Wait mode	Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock operation	—	15	90	µA
			Off	Off	Off	125 kHz	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	4	80	µA
			Off	32 kHz	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 SVC0 = 1	While a WAIT instruction is executed Peripheral clock off	—	3.5	—	µA
		Stop mode	Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 25°C Peripheral clock off	—	2.2	6	µA
			Off	Off	Off	Off	—	VCA27 = 0 VCA26 = 0 VCA25 = 0 CM10 = 1	Topr = 85°C Peripheral clock off	—	30	—	µA

Notes:
1. Vcc = 1.8 V to 2.7 V, single-chip mode, output pins are open, and other pins are Vss.
2. XIN is set to square wave input.
3. fHOCO-F
4. The typical value (Typ.) indicates the current value when the CPU and the memory operate.
   The maximum value (Max.) indicates the current value when the CPU, the memory, and the peripheral functions operate and the flash memory is programmed/erased.

Table 4.24 Timing Requirements of Serial Interface (Internal clock selected as transfer clock (master communication))

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{d(C-Q)}$	TXDi output delay time	—	200	—	30	—	10	ns
$t_{su(D-C)}$	RXDi input setup time (1)	150	—	120	—	90	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	90	—	ns

i = 0 or 1

Note:

1. External pin load condition CL = 30 pF

Table 4.25 Timing Requirements of Serial Interface (External clock selected as transfer clock (slave communication))

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{c(CK)}$	CLKi input cycle time	800	—	300	—	200	—	ns
$t_{w(CKH)}$	CLKi input high width	400	—	150	—	100	—	ns
$t_{w(CKL)}$	CLKi input low width	400	—	150	—	100	—	ns
$t_{d(C-Q)}$	TXDi output delay time	—	200	—	120	—	90	ns
$t_{su(D-C)}$	RXDi input setup time	150	—	30	—	10	—	ns
$t_{h(C-D)}$	RXDi input hold time	90	—	90	—	90	—	ns

i = 0 or 1

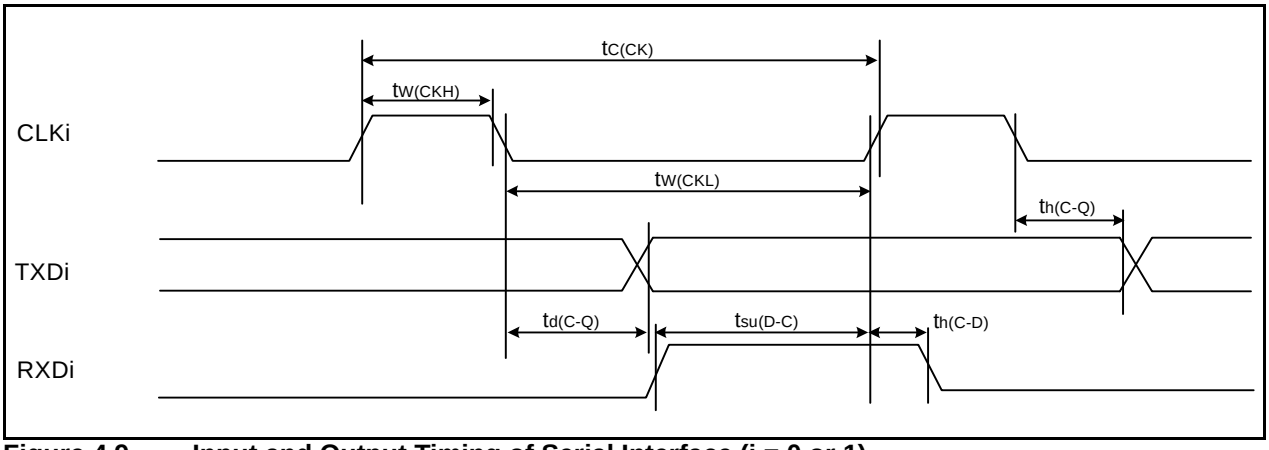


Figure 4.9 Input and Output Timing of Serial Interface (i = 0 or 1)

Table 4.26 Timing Requirements of External Interrupt $\overline{INTi}$ (i = 0 to 4) and Key Input Interrupt $\overline{KIj}$ (j = 0 to 3)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
$t_{W(INH)}$	$\overline{INTi}$ input high width, $\overline{KIj}$ input high width	1000 (1)	—	380 (1)	—	250 (1)	—	ns
$t_{W(INL)}$	$\overline{INTi}$ input low width, $\overline{KIj}$ input low width	1000 (2)	—	380 (2)	—	250 (2)	—	ns

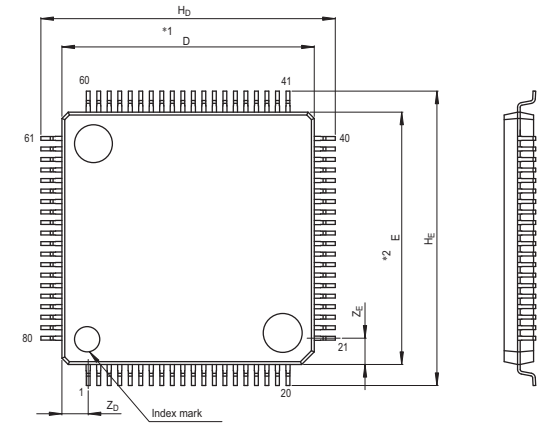
Notes:
1. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input high pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.
2. When selecting the digital filter by the $\overline{INTi}$ input filter select bit, use an $\overline{INTi}$ input low pulse width of either (1/digital filter sampling frequency × 3) or the minimum value of standard, whichever is greater.

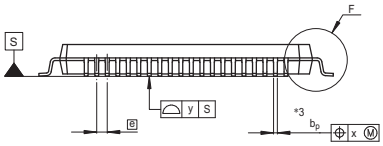
Figure 4.10 Input Timing of External Interrupt $\overline{INTi}$ and Key Input Interrupt $\overline{KIj}$ (i = 0 to 4; j = 0 to 3)

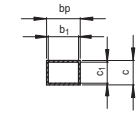
Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.

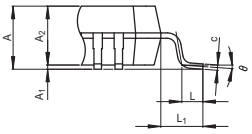
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LQFP80-12x12-0.50	PLQP0080KB-A	80P6Q-A	0.5g







Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A_2	—	1.4	—
H_D	13.8	14.0	14.2
H_E	13.8	14.0	14.2
A	—	—	1.7
A_1	0	0.1	0.2
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	10°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.3	0.5	0.7
L_1	—	1.0	—

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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