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"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	R8C
Core Size	16-Bit
Speed	20MHz
Connectivity	I ² C, LINbus, SIO, SSU, UART/USART
Peripherals	POR, PWM, Voltage Detect, WDT
Number of I/O	75
Program Memory Size	128KB (128K x 8)
Program Memory Type	FLASH
EEPROM Size	4K x 8
RAM Size	10K x 8
Voltage - Supply (Vcc/Vdd)	1.8V ~ 5.5V
Data Converters	A/D 20x10b
Oscillator Type	Internal
Operating Temperature	-20°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	80-LQFP
Supplier Device Package	80-LQFP (12x12)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/r5f2138csnfp-30

Table 1.6 Pin Name Information by Pin Number (SSU/I²C, Timer RJ, and Timer RB2) (1)

Port	Pin No.	SSU/I ² C						Timer RJ		Timer RB2
		SCL_0	SDA_0	SSI_0	SCS_0	SSCK_0	SSO_0	TRJO_0	TRJIO_0	TRBO_0
P0_0	72									
P0_1	71									
P0_2	70									
P0_3	69									
P0_4	68									
P0_5	67									
P0_6	66									
P0_7	65									
P1_0	56									
P1_1	55									
P1_2	54									
P1_3	53									TRBO_0
P1_4	52									
P1_5	51								TRJIO_0	
P1_6	50									
P1_7	49									
P2_0	30									
P2_1	29									
P2_2	28									
P2_3	27									
P2_4	26									
P2_5	25									
P2_6	24									
P2_7	23									
P3_0	4							TRJO_0		
P3_1	36									
P3_2	3								TRJIO_0	
P3_3	22				SCS_0					
P3_4	21			SSI_0						
P3_5	20	SCL_0				SSCK_0				
P3_6	35									
P3_7	19		SDA_0				SSO_0			
P4_2	5									
P4_3	7									
P4_4	8									
P4_5	48									
P4_6	12									
P4_7	10									
P5_0	18									
P5_1	17									
P5_2	16									
P5_3	15									
P5_4	14									
P5_5	2								TRJIO_0	
P5_6	1									
P5_7	80									
P6_0	77									
P6_1	76									
P6_2	75									
P6_3	74									
P6_4	73									
P6_5	47									
P6_6	46									
P6_7	45									
P7_0	64									
P7_1	63									
P7_2	62									
P7_3	61									
P7_4	60									
P7_5	59									
P7_6	58									
P7_7	57									

Table 1.7 Pin Name Information by Pin Number (SSU/I²C, Timer RJ, and Timer RB2) (2)

Port	Pin No.	SSU/I ² C						Timer RJ		Timer RB2
		SCL_0	SDA_0	SSI_0	SCS_0	SSCK_0	SSO_0	TRJO_0	TRJO_0	TRBO_0
P8_0	44									
P8_1	43									
P8_2	42									
P8_3	41									
P8_4	40									
P8_5	39									
P8_6	38									
P8_7	37									
P9_0	34									
P9_1	33									
P9_2	32									
P9_3	31									
P9_4	79									
P9_5	78									

2. Central Processing Unit (CPU)

Figure 2.1 shows the 13 CPU Registers. The registers R0, R1, R2, R3, A0, A1, and FB form a single register bank. The CPU has two register banks.

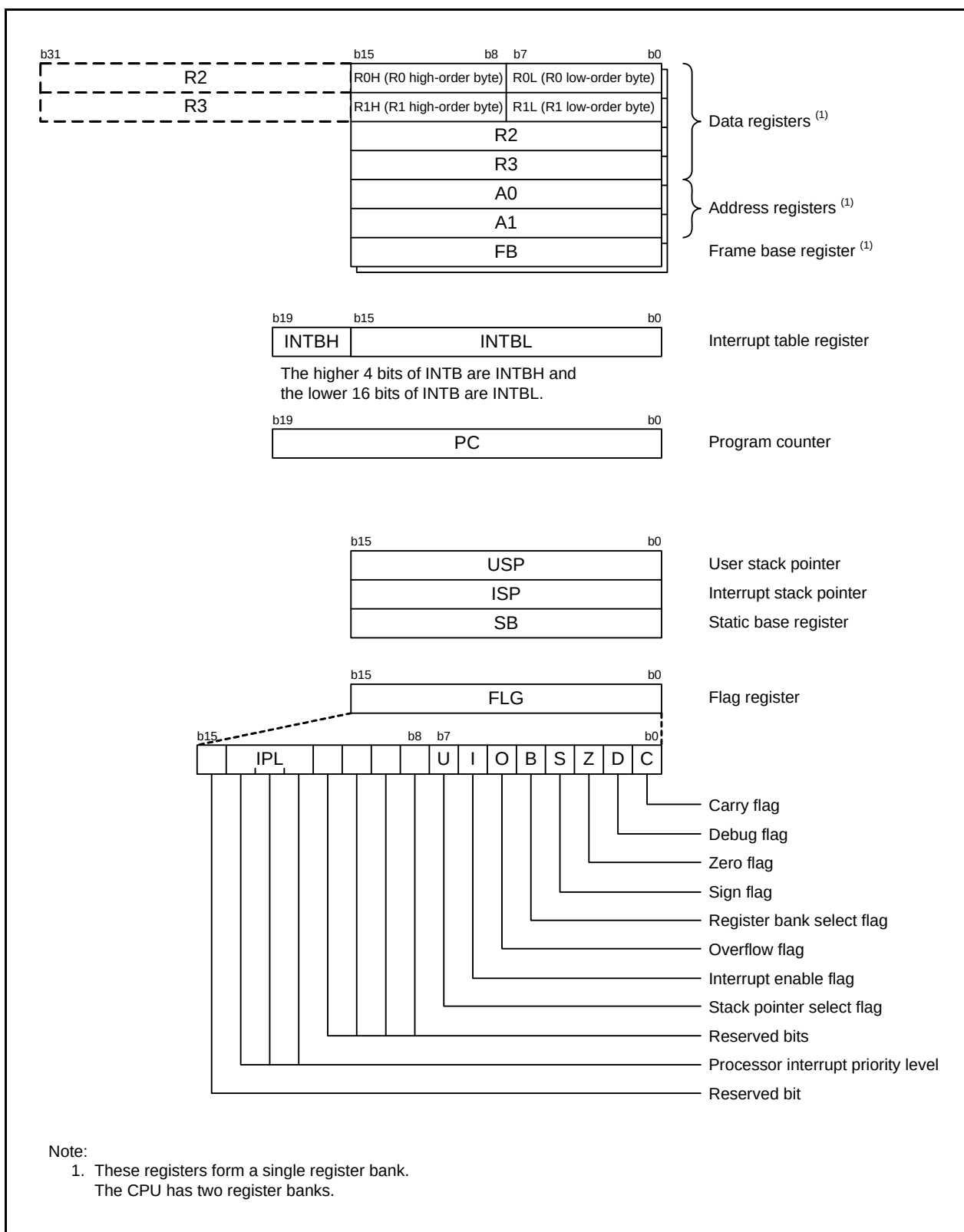


Figure 2.1 CPU Registers

Table 3.5 SFR Information (5) (1)

Address	Symbol	Register Name	After Reset	Remarks
000FAh				
000FBh				
000FCh				
000FDh				
000FEh				
000FFh				
00100h				
00101h				
00102h				
00103h				
00104h				
00105h				
00106h				
00107h				
00108h				
00109h				
0010Ah				
0010Bh				
0010Ch				
0010Dh				
0010Eh				
0010Fh				
00110h	TRJ_0	Timer RJ_0 Counter Register	FFFFh	
00111h				
00112h	TRJCR_0	Timer RJ_0 Control Register	00h	
00113h	TRJIOC_0	Timer RJ_0 I/O Control Register	00h	
00114h	TRJMR_0	Timer RJ_0 Mode Register	00h	
00115h	TRJISR_0	Timer RJ_0 Event Pin Select Register	00h	
00116h				
00117h				
00118h				
00119h				
0011Ah				
0011Bh				
0011Ch				
0011Dh				
0011Eh				
0011Fh				
00120h				
00121h				
00122h				
00123h				
00124h				
00125h				
00126h				
00127h				
00128h				
00129h				
0012Ah				
0012Bh				
0012Ch				
0012Dh				
0012Eh				
0012Fh				
00130h	TRBCR_0	Timer RB2_0 Control Register	00h	
00131h	TRBOCR_0	Timer RB2_0 One-Shot Control Register	00h	
00132h	TRBIOC_0	Timer RB2_0 I/O Control Register	00h	
00133h	TRBMR_0	Timer RB2_0 Mode Register	00h	
00134h	TRBPRES_0	Timer RB2_0 Prescaler Register	FFh	
00135h	TRBPR_0	Timer RB2_0 Primary Register	FFh	
00136h	TRBSC_0	Timer RB2_0 Secondary Register	FFh	
00137h	TRBIR_0	Timer RB2_0 Interrupt Request Register	00h	
00138h	TRCNT_0	Timer RC_0 Counter	0000h	
00139h				

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.6 SFR Information (6) (1)

Address	Symbol	Register Name	After Reset	Remarks
0013Ah	TRCGRA_0	Timer RC_0 General Register A	FFFFh	
0013Bh				
0013Ch	TRCGRB_0	Timer RC_0 General Register B	FFFFh	
0013Dh				
0013Eh	TRCGRC_0	Timer RC_0 General Register C	FFFFh	
0013Fh				
00140h	TRCGRD_0	Timer RC_0 General Register D	FFFFh	
00141h				
00142h	TRCMR_0	Timer RC_0 Mode Register	01001000b	
00143h	TRCCR1_0	Timer RC_0 Control Register 1	00h	
00144h	TRCIER_0	Timer RC_0 Interrupt Enable Register	01110000b	
00145h	TRCSR_0	Timer RC_0 Status Register	01110000b	
00146h	TRCIOR0_0	Timer RC_0 I/O Control Register 0	10001000b	
00147h	TRCIOR1_0	Timer RC_0 I/O Control Register 1	10001000b	
00148h	TRCCR2_0	Timer RC_0 Control Register 2	00011000b	
00149h	TRCDF_0	Timer RC_0 Digital Filter Function Select Register	00h	
0014Ah	TRCOER_0	Timer RC_0 Output Enable Register	01111111b	
0014Bh	TRCADCR_0	Timer RC_0 A/D Conversion Trigger Control Register	11110000b	
0014Ch	TRCOPR_0	Timer RC_0 Output Waveform Manipulation Register	00h	
0014Dh	TRCELCCR_0	Timer RC_0 ELC Cooperation Control Register	00h	
0014Eh				
0014Fh				
00150h				
00151h				
00152h				
00153h				
00154h				
00155h				
00156h				
00157h				
00158h				
00159h				
0015Ah				
0015Bh				
0015Ch				
0015Dh				
0015Eh				
0015Fh				
00160h				
00161h				
00162h				
00163h				
00164h				
00165h				
00166h				
00167h				
00168h				
00169h				
0016Ah				
0016Bh				
0016Ch				
0016Dh				
0016Eh				
0016Fh				
00170h	TRESEC	Timer RE2 Counter Data Register Timer RE2 Second Data Register	00h	
00171h	TREMIN	Timer RE2 Compare Data Register Timer RE2 Minute Data Register	00h	
00172h	TREHR	Timer RE2 Hour Data Register	00h	
00173h	TREWK	Timer RE2 Day-of-the-Week Data Register	00h	
00174h	TREDY	Timer RE2 Day Data Register	00000001b	
00175h	TREMON	Timer RE2 Month Data Register	00000001b	
00176h	TREYR	Timer RE2 Year Data Register	00h	
00177h	TRECR	Timer RE2 Control Register	00000100b	
00178h	TRECSR	Timer RE2 Count Source Select Register	00001000b	
00179h	TREADJ	Timer RE2 Clock Error Correction Register	00h	

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.7 SFR Information (7) (1)

Address	Symbol	Register Name	After Reset	Remarks
0017Ah	TREIFR	Timer RE2 Interrupt Flag Register	00h	
0017Bh	TREIER	Timer RE2 Interrupt Enable Register	00h	
0017Ch	TREAMN	Timer RE2 Alarm Minute Register	00h	
0017Dh	TREahr	Timer RE2 Alarm Hour Register	00h	
0017Eh	TREAwK	Timer RE2 Alarm Day-of-the-Week Register	00h	
0017Fh	TREPRC	Timer RE2 Protect Register	00h	
00180h to 001FFh				
00200h	AD0	A/D Register 0	00h	
00201h			00h	
00202h	AD1	A/D Register 1	00h	
00203h			00h	
00204h	AD2	A/D Register 2	00h	
00205h			00h	
00206h	AD3	A/D Register 3	00h	
00207h			00h	
00208h	AD4	A/D Register 4	00h	
00209h			00h	
0020Ah	AD5	A/D Register 5	00h	
0020Bh			00h	
0020Ch	AD6	A/D Register 6	00h	
0020Dh			00h	
0020Eh	AD7	A/D Register 7	00h	
0020Fh			00h	
00210h				
00211h				
00212h				
00213h				
00214h	ADMOD	A/D Mode Register	00h	
00215h	ADINSEL	A/D Input Select Register	11000000b	
00216h	ADCON0	A/D Control Register 0	00h	
00217h	ADCON1	A/D Control Register 1	00h	
00218h				
00219h				
0021Ah				
0021Bh				
0021Ch				
0021Dh				
0021Eh				
0021Fh				
00220h				
00221h				
00222h				
00223h				
00224h				
00225h				
00226h				
00227h				
00228h	INTCMP	Comparator B Control Register 0	00h	
00229h				
0022Ah				
0022Bh				
0022Ch				
0022Dh				
0022Eh				
0022Fh				
00230h	INTEN	External Input Enable Register 0	00h	
00231h	INTEN1	External Input Enable Register 1	00h	
00232h	INTF	INT Input Filter Select Register 0	00h	
00233h	INTF1	INT Input Filter Select Register 1	00h	
00234h	INTPOL	INT Input Polarity Switch Register	00h	
00235h				
00236h	KIEN	Key Input Interrupt Enable Register	00h	
00237h				
00238h	MSTCR0	Module Standby Control Register 0	00h	
00239h	MSTCR1	Module Standby Control Register 1	00h	

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.8 SFR Information (8) (1)

Address	Symbol	Register Name	After Reset	Remarks
0023Ah	MSTCR2	Module Standby Control Register 2	00h	
0023Bh	MSTCR3	Module Standby Control Register 3	00h	
0023Ch	MSTCR4	Module Standby Control Register 4	00h	
0023Dh				
0023Eh				
0023Fh				
00240h				
00241h				
00242h				
00243h				
00244h				
00245h				
00246h				
00247h				
00248h				
00249h				
0024Ah				
0024Bh				
0024Ch				
0024Dh				
0024Eh				
0024Fh				
00250h				
00251h				
00252h	FST	Flash Memory Status Register	10000X00b	
00253h				
00254h	FMR0	Flash Memory Control Register 0	00h	
00255h	FMR1	Flash Memory Control Register 1	00h	
00256h	FMR2	Flash Memory Control Register 2	00h	
00257h				
00258h				
00259h				
0025Ah				
0025Bh				
0025Ch				
0025Dh				
0025Eh				
0025Fh				
00260h	AIADR0L	Address Match Interrupt Address 0L Register	XXXXh	
00261h				
00262h	AIADR0H	Address Match Interrupt Address 0H Register	0000XXXXb	
00263h	AIEN0	Address Match Interrupt Enable 0 Register	00h	
00264h	AIADR1L	Address Match Interrupt Address 1L Register	XXXXh	
00265h				
00266h	AIADR1H	Address Match Interrupt Address 1H Register	0000XXXXb	
00267h	AIEN1	Address Match Interrupt Enable 1 Register	00h	
00268h				
00269h				
0026Ah				
0026Bh				
0026Ch				
0026Dh				
0026Eh				
0026Fh				
00270h				
00271h				
00272h				
00273h				
00274h				
00275h				
00276h				
00277h				
00278h				
00279h				
0027Ah				
0027Bh				
0027Ch				
0027Dh				
0027Eh				
0027Fh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.13 SFR Information (13) ⁽¹⁾

Address	Symbol	Register Name	After Reset	Remarks
06C0Ah		Area for storing DTC transfer vector 10	XXh	
06C0Bh		Area for storing DTC transfer vector 11	XXh	
06C0Ch		Area for storing DTC transfer vector 12	XXh	
06C0Dh		Area for storing DTC transfer vector 13	XXh	
06C0Eh		Area for storing DTC transfer vector 14	XXh	
06C0Fh		Area for storing DTC transfer vector 15	XXh	
06C10h		Area for storing DTC transfer vector 16	XXh	
06C11h		Area for storing DTC transfer vector 17	XXh	
06C12h		Area for storing DTC transfer vector 18	XXh	
06C13h		Area for storing DTC transfer vector 19	XXh	
06C14h				
06C15h				
06C16h		Area for storing DTC transfer vector 22	XXh	
06C17h		Area for storing DTC transfer vector 23	XXh	
06C18h		Area for storing DTC transfer vector 24	XXh	
06C19h		Area for storing DTC transfer vector 25	XXh	
06C1Ah				
06C1Bh				
06C1Ch				
06C1Dh				
06C1Eh				
06C1Fh				
06C20h				
06C21h				
06C22h				
06C23h				
06C24h				
06C25h				
06C26h				
06C27h				
06C28h				
06C29h				
06C2Ah		Area for storing DTC transfer vector 42	XXh	
06C2Bh				
06C2Ch				
06C2Dh				
06C2Eh				
06C2Fh				
06C30h				
06C31h		Area for storing DTC transfer vector 49	XXh	
06C32h				
06C33h		Area for storing DTC transfer vector 51	XXh	
06C34h		Area for storing DTC transfer vector 52	XXh	
06C35h		Area for storing DTC transfer vector 53	XXh	
06C36h		Area for storing DTC transfer vector 54	XXh	
06C37h				
06C38h				
06C39h				
06C3Ah				
06C3Bh				
06C3Ch				
06C3Dh				
06C3Eh				
06C3Fh				
06C40h	DTCCR0	DTC Control Register 0	XXh	
06C41h	DTBLS0	DTC Block Size Register 0	XXh	
06C42h	DTCC0	DTC Transfer Count Register 0	XXh	
06C43h	DTRL0	DTC Transfer Count Reload Register 0	XXh	
06C44h	DTSAR0	DTC Source Address Register 0	XXXXh	
06C45h				
06C46h	DTDAR0	DTC Destination Address Register 0	XXXXh	
06C47h				
06C48h	DTCCR1	DTC Control Register 1	XXh	
06C49h	DTBLS1	DTC Block Size Register 1	XXh	

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.16 SFR Information (16) ⁽¹⁾

Address	Symbol	Register Name	After Reset	Remarks
06CD0h	DTCCR18	DTC Control Register 18	XXh	
06CD1h	DTBLS18	DTC Block Size Register 18	XXh	
06CD2h	DTCCT18	DTC Transfer Count Register 18	XXh	
06CD3h	DTRL18	DTC Transfer Count Reload Register 18	XXh	
06CD4h	DTSAR18	DTC Source Address Register 18	XXXXh	
06CD5h				
06CD6h	DTDAR18	DTC Destination Address Register 18	XXXXh	
06CD7h				
06CD8h	DTCCR19	DTC Control Register 19	XXh	
06CD9h	DTBLS19	DTC Block Size Register 19	XXh	
06CDAh	DTCCT19	DTC Transfer Count Register 19	XXh	
06CDBh	DTRL19	DTC Transfer Count Reload Register 19	XXh	
06CDC	DTSAR19	DTC Source Address Register 19	XXXXh	
06CDDh				
06CDEh	DTDAR19	DTC Destination Address Register 19	XXXXh	
06CDFh				
06CE0h	DTCCR20	DTC Control Register 20	XXh	
06CE1h	DTBLS20	DTC Block Size Register 20	XXh	
06CE2h	DTCCT20	DTC Transfer Count Register 20	XXh	
06CE3h	DTRL20	DTC Transfer Count Reload Register 20	XXh	
06CE4h	DTSAR20	DTC Source Address Register 20	XXXXh	
06CE5h				
06CE6h	DTDAR20	DTC Destination Address Register 20	XXXXh	
06CE7h				
06CE8h	DTCCR21	DTC Control Register 21	XXh	
06CE9h	DTBLS21	DTC Block Size Register 21	XXh	
06CEAh	DTCCT21	DTC Transfer Count Register 21	XXh	
06CEBh	DTRL21	DTC Transfer Count Reload Register 21	XXh	
06CECh	DTSAR21	DTC Source Address Register 21	XXXXh	
06CEDh				
06CEEh	DTDAR21	DTC Destination Address Register 21	XXXXh	
06CEFh				
06CF0h	DTCCR22	DTC Control Register 22	XXh	
06CF1h	DTBLS22	DTC Block Size Register 22	XXh	
06CF2h	DTCCT22	DTC Transfer Count Register 22	XXh	
06CF3h	DTRL22	DTC Transfer Count Reload Register 22	XXh	
06CF4h	DTSAR22	DTC Source Address Register 22	XXXXh	
06CF5h				
06CF6h	DTDAR22	DTC Destination Address Register 22	XXXXh	
06CF7h				
06CF8h	DTCCR23	DTC Control Register 23	XXh	
06CF9h	DTBLS23	DTC Block Size Register 23	XXh	
06CFAh	DTCCT23	DTC Transfer Count Register 23	XXh	
06CFBh	DTRL23	DTC Transfer Count Reload Register 23	XXh	
06CFCh	DTSAR23	DTC Source Address Register 23	XXXXh	
06CFDh				
06CFEh	DTDAR23	DTC Destination Address Register 23	XXXXh	
06CFFh				
06D00h to 06FFFh				

X: Undefined

Note:

1. The blank areas are reserved. No access is allowed.

Table 3.17 ID code Area, Option Function Select Area

Address	Symbol	Area Name	After Reset	Address size
0FFDBh	OFS2	Option Function Select Register 2	(Note 1)	
0FFDFh	ID1		(Note 2)	
0FFE3h	ID2		(Note 2)	
0FFEBh	ID3		(Note 2)	
0FFEFh	ID4		(Note 2)	
0FFF3h	ID5		(Note 2)	
0FFF7h	ID6		(Note 2)	
0FFFBh	ID7		(Note 2)	
0FFFFh	OFS	Option Function Select Register	(Note 1)	

Notes:

1. The option function select area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the option function select area. Erasing the block including the option function select area sets the option function select area to FFh.
2. The ID code area is allocated in the flash memory, not in the SFRs. Set appropriate values as ROM data by a program. Do not perform any additional writes to the ID code area. Erasing the block including the ID code area sets the ID code area to FFh.

4. Electrical Characteristics

4.1 Absolute Maximum Ratings

Table 4.1 Absolute Maximum Ratings

Symbol	Parameter	Condition	Rated Value	Unit
V _{CC} /A _V _{CC} I _{CE} V _{CC}	Supply voltage		−0.3 to 6.5	V
V _I	Input voltage		−0.3 to V _{CC} + 0.3	V
V _O	Output voltage		−0.3 to V _{CC} + 0.3	V
P _d	Power dissipation	−40°C ≤ T _{opr} ≤ 85°C	500	mW
T _{opr}	Operating ambient temperature		−20 to 85 (N version)/ −40 to 85 (D version)	°C
T _{stg}	Storage temperature		−65 to 150	°C

4.2 Recommended Operating Conditions

Table 4.2 Recommended Operating Conditions (1)
(V_{CC} = 1.8 V to 5.5 V, T_{opr} = –20°C to 85°C (N version)/–40°C to 85°C (D version),
unless otherwise specified)

Symbol	Parameter			Conditions	Standard			Unit	
					Min.	Typ.	Max.		
V _{CC} /AV _{CC}	Supply voltage				1.8	—	5.5	V	
V _{SS} /AV _{SS}	Supply voltage				—	0	—	V	
V _{IH}	Input high voltage	Other than CMOS input				0.8V _{CC}	—	V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.5V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.55V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.65V _{CC}	—	V _{CC}	V
				Input level selection: 0.5V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.65V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.7V _{CC}	—	V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0.8V _{CC}	—	V _{CC}	V
				Input level selection: 0.7V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0.85V _{CC}	—	V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0.85V _{CC}	—	V _{CC}	V
		1.8 V ≤ V _{CC} < 2.7 V	0.85V _{CC}		—	V _{CC}	V		
	External clock input (XOUT)				1.2	—	V _{CC}	V	
V _{IL}	Input low voltage	Other than CMOS input				0	—	0.2V _{CC}	V
		CMOS input	Input level switching function (I/O port)	Input level selection: 0.35V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.2V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.2V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2V _{CC}	V
				Input level selection: 0.5V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.4V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.3V _{CC}	V
					1.8 V ≤ V _{CC} < 2.7 V	0	—	0.2V _{CC}	V
				Input level selection: 0.7V _{CC}	4.0 V ≤ V _{CC} ≤ 5.5 V	0	—	0.55V _{CC}	V
					2.7 V ≤ V _{CC} < 4.0 V	0	—	0.45V _{CC}	V
		1.8 V ≤ V _{CC} < 2.7 V	0		—	0.35V _{CC}	V		
	External clock input (XOUT)				0	—	0.4	V	
I _{OH} (sum)	Peak sum output high current	Sum of all pins I _{OH} (peak)		—	—	–80	mA		
I _{OH} (sum)	Average sum output high current	Sum of all pins I _{OH} (avg)		—	—	–40	mA		
I _{OH} (peak)	Peak output high current	When drive capacity is low		—	—	–10	mA		
		When drive capacity is high		—	—	–40	mA		
I _{OH} (avg)	Average output high current	When drive capacity is low		—	—	–5	mA		
		When drive capacity is high		—	—	–20	mA		
I _{OL} (sum)	Peak sum output low current	Sum of all pins I _{OL} (peak)		—	—	80	mA		
I _{OL} (sum)	Average sum output low current	Sum of all pins I _{OL} (avg)		—	—	40	mA		
I _{OL} (peak)	Peak output low current	When drive capacity is low		—	—	10	mA		
		When drive capacity is high		—	—	40	mA		
I _{OL} (avg)	Average output low current	When drive capacity is low		—	—	5	mA		
		When drive capacity is high		—	—	20	mA		
f _(XIN)	XIN clock input oscillation frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(XCIN)	XCIN clock input oscillation frequency			1.8 V ≤ V _{CC} ≤ 5.5 V	—	32.768	50	kHz	
f _{HOCO}	Count source for timer RC			2.7 V ≤ V _{CC} ≤ 5.5 V	32	—	40	MHz	
f _{HOCO-F}	f _{HOCO-F} frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
—	System clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	
f _(BCLK)	CPU clock frequency			2.7 V ≤ V _{CC} ≤ 5.5 V	—	—	20	MHz	
				1.8 V ≤ V _{CC} < 2.7 V	—	—	5	MHz	

Note:

1. The average output current indicates the average value of current measured during 100 ms.

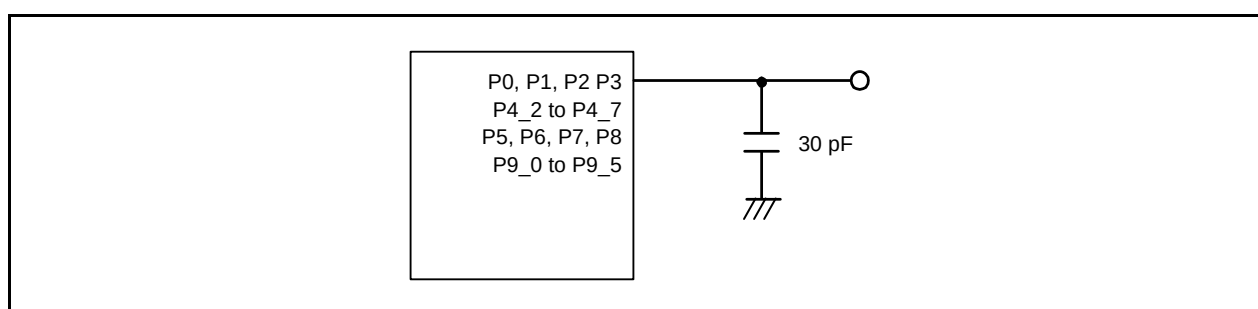


Figure 4.1 Timing Measurement Circuit for Ports P0, P1, P2, P3, P4_2 to P4_7, P5, P6, P7, P8, and P9_0 to P9_5

Table 4.10 Power-On Reset Circuit Characteristics ⁽¹⁾
(Measurement conditions: V_{CC} = 1.8 V to 5.5 V, Topr = –20°C to 85°C (N version)/
–40°C to 85°C (D version))

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
trth	External power VCC rise gradient		0	—	50,000	mV/msec

Note:

- To use the power-on reset function, enable voltage monitor 0 reset by setting the LVDAS bit in the OFS register to 0.

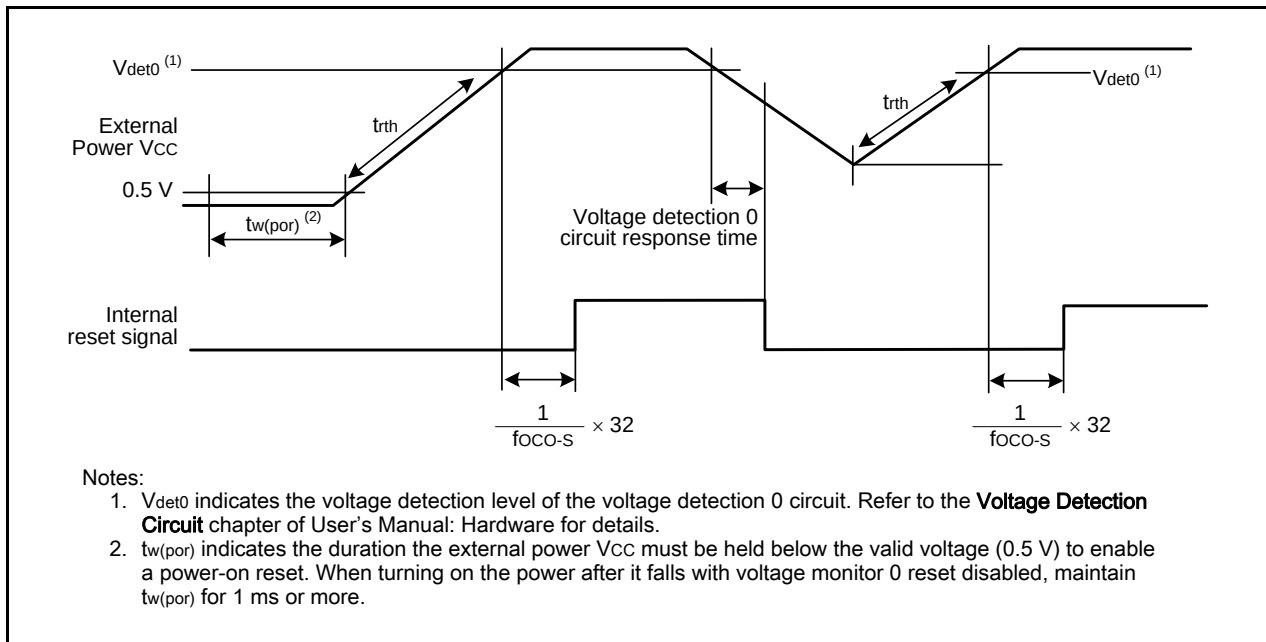


Figure 4.3 Power-on Reset Circuit Characteristics

Table 4.11 High-Speed On-Chip Oscillator Circuit Characteristics

Symbol	Parameter	Conditions	Standard			Unit
			Min.	Typ.	Max.	
—	High-speed on-chip oscillator frequency after reset	V _{CC} = 1.8 V to 5.5 V, –20°C ≤ Topr ≤ 85°C	—	40	—	MHz
—	High-speed on-chip oscillator frequency when 01b or 10b is written to bits FRA25 and FRA24 in the FRA2 register ⁽¹⁾	(N version) –40°C ≤ Topr ≤ 85°C (D version)	—	36.864	—	MHz
—	High-speed on-chip oscillator frequency when 10b is written to bits FRA25 and FRA24 in the FRA2 register		—	32	—	MHz
—	High-speed on-chip oscillator frequency dependence on temperature and power supply voltage ⁽²⁾		–1.5	—	1.5	%
—	Oscillation stability time	V _{CC} = 5.0 V, Topr = 25°C	—	250	—	μs
—	Self power consumption at oscillation	V _{CC} = 5.0 V, Topr = 25°C	—	500	—	μA

Notes:

- This enables the setting errors of bit rates such as 9600 bps and 38400 bps to be 0% when the serial interface is used in UART mode.
- This indicates the precision error for the oscillation frequency of the high-speed on-chip oscillator.

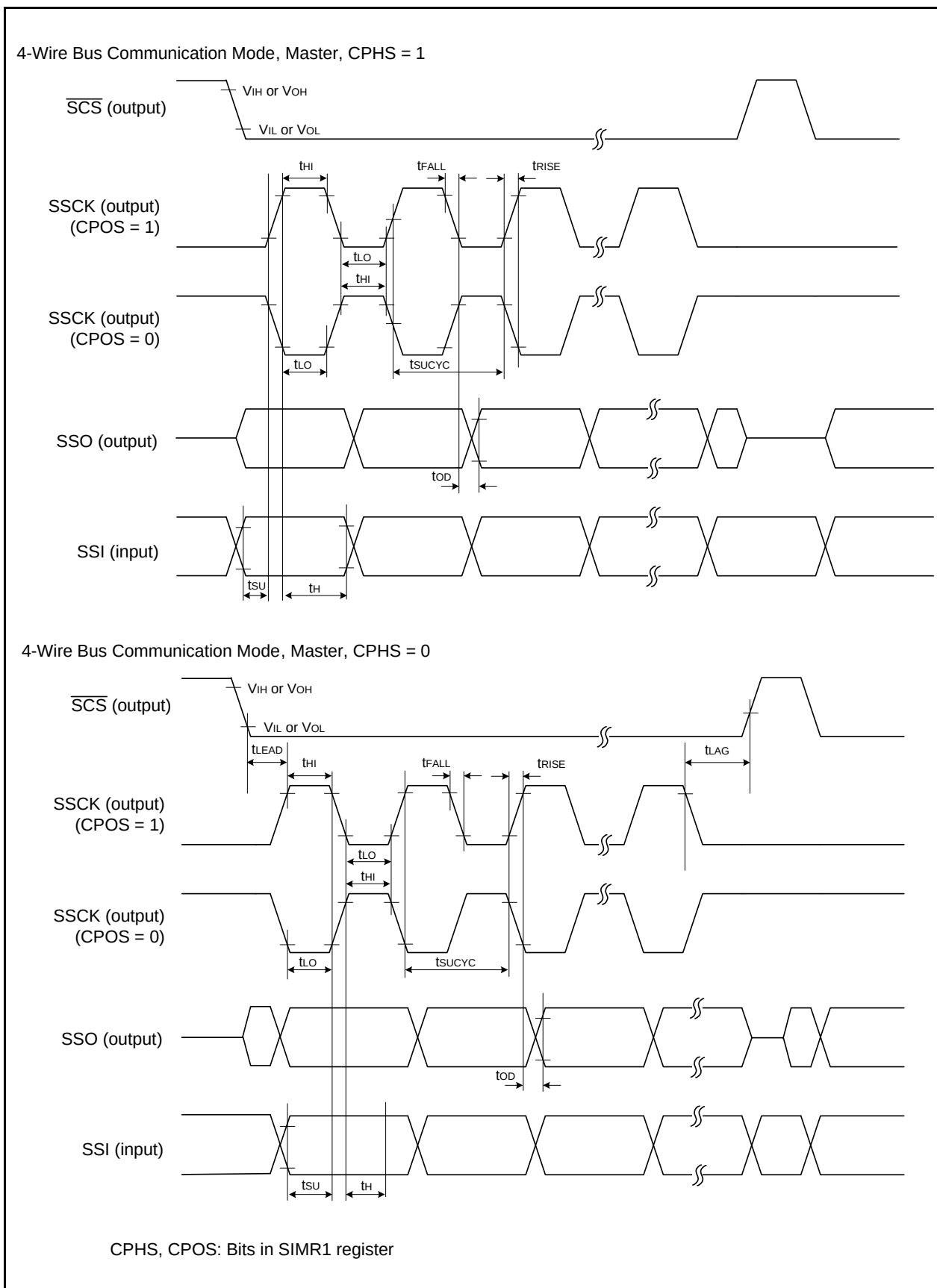


Figure 4.4 I/O Timing of Synchronous Serial Communication Unit (SSU) (Master)

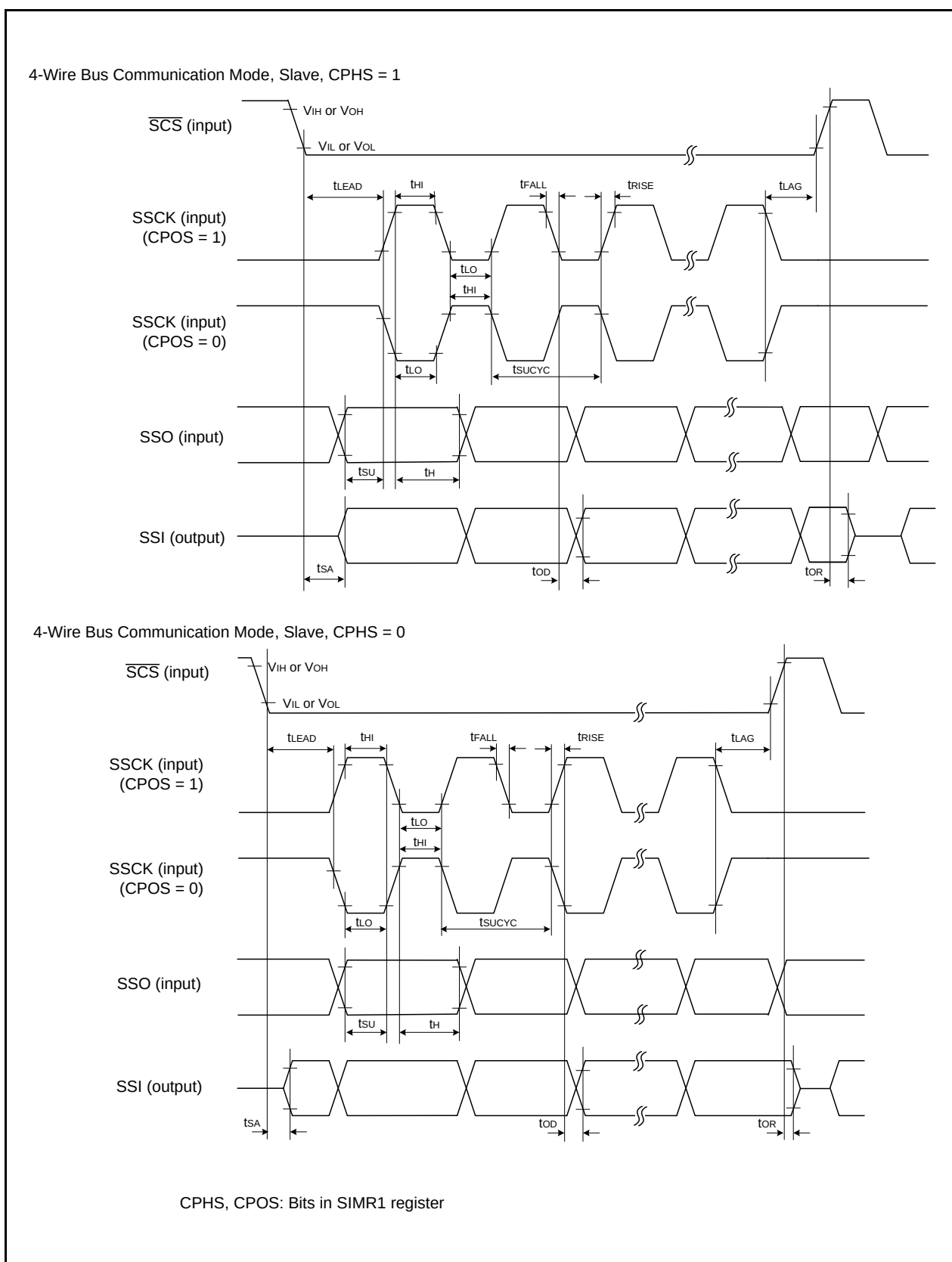
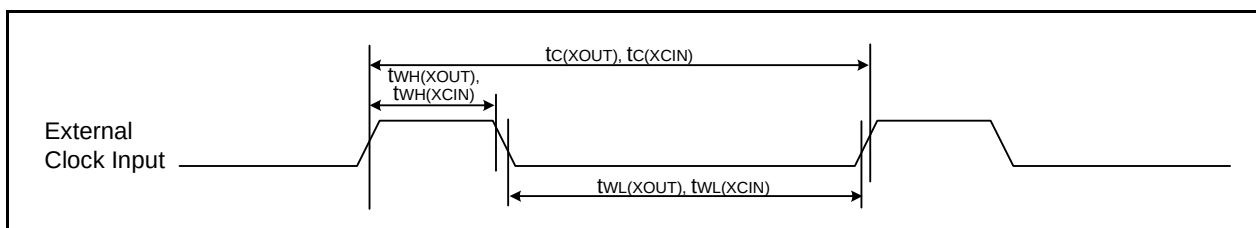


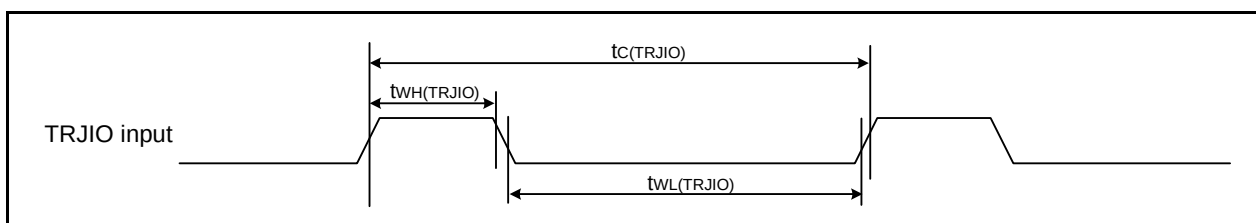
Figure 4.5 I/O Timing of Synchronous Serial Communication Unit (SSU) (Slave)

Table 4.22 External Clock Input (XOUT, XCIN)

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (XOUT)	XOUT input cycle time	200	—	50	—	50	—	ns
t _{WH} (XOUT)	XOUT input high width	90	—	24	—	24	—	ns
t _{WL} (XOUT)	XOUT input low width	90	—	24	—	24	—	ns
t _c (XCIN)	XCIN input cycle time	14	—	14	—	14	—	μs
t _{WH} (XCIN)	XCIN input high width	7	—	7	—	7	—	μs
t _{WL} (XCIN)	XCIN input low width	7	—	7	—	7	—	μs

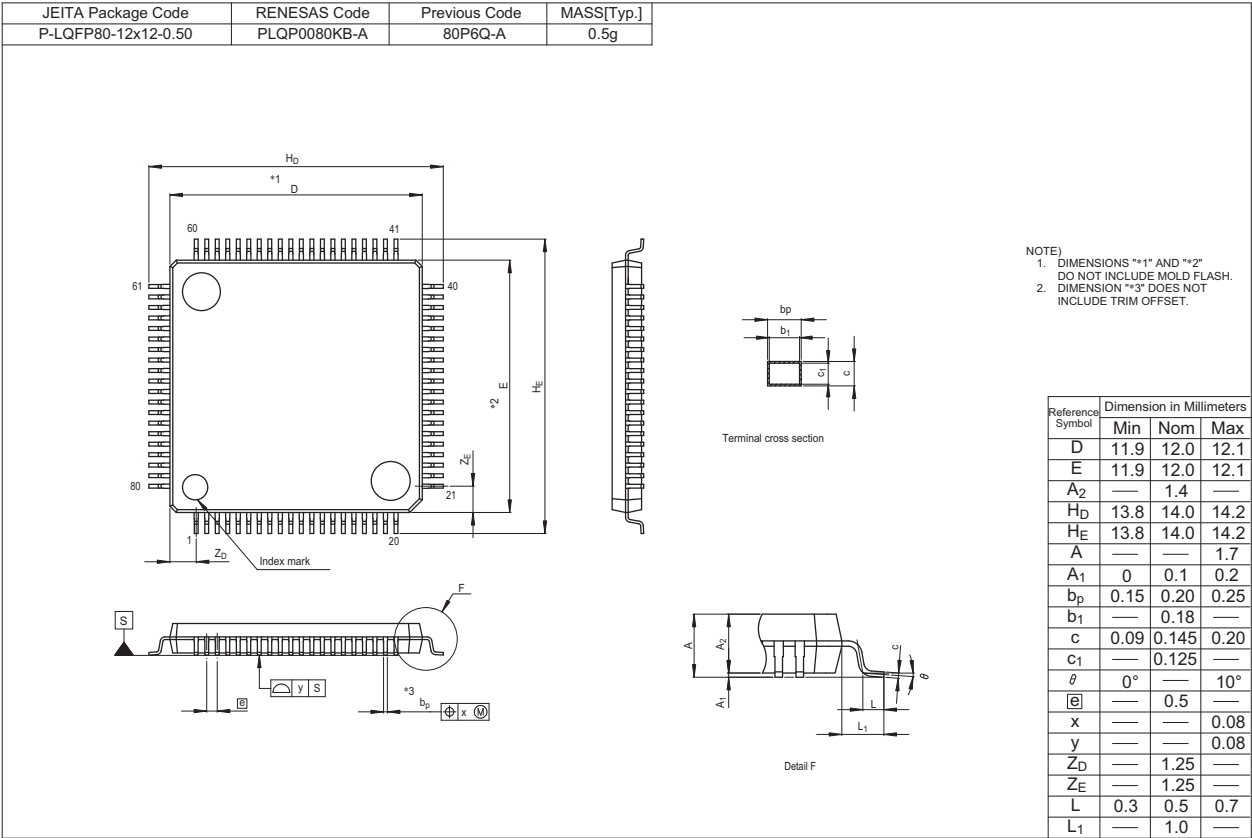
**Figure 4.7 External Clock Input Timing Diagram****Table 4.23 Timing Requirements of TRJIO**

Symbol	Parameter	Standard						Unit
		Vcc = 2.2 V, Topr = 25°C		Vcc = 3 V, Topr = 25°C		Vcc = 5 V, Topr = 25°C		
		Min.	Max.	Min.	Max.	Min.	Max.	
t _c (TRJIO)	TRJIO input cycle time	500	—	300	—	100	—	ns
t _{WH} (TRJIO)	TRJIO input high width	200	—	120	—	40	—	ns
t _{WL} (TRJIO)	TRJIO input low width	200	—	120	—	40	—	ns

**Figure 4.8 Input Timing of TRJIO**

Appendix 1. Package Dimensions

Diagrams showing the latest package dimensions and mounting information are available in the “Packages” section of the Renesas Electronics website.



REVISION HISTORY	R8C/38T-A Group User's Manual: Datasheet
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Rev.	Date	Description	
		Page	Summary
0.01	Feb 23, 2011	—	First Edition issued
1.00	Dec 09, 2011	All pages	"Preliminary", "Under development" deleted, "sensor control unit" → "touch sensor control unit"
		2, 3	Tables 1.1 and 1.2 revised
		6	Figure 1.3 revised
		16	2.1 revised
		19, 20, 22 to 25, 27 to 31	Tables 3.1, 3.2, 3.4 to 3.7, 3.9 to 3.13
		35	Table 3.17 revised, Note 2 added
		36 to 59	"4. Electrical Characteristics" added

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General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins

Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.

- The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

The state of the product is undefined at the moment when power is supplied.

- The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.

In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.

In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

Access to reserved addresses is prohibited.

- The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

- When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.

- The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.