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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | 4125 |
| Number of Logic Elements/Cells | 41250 |
| Total RAM Bits | 2244096 |
| Number of I/O | 613 |
| Number of Gates | - |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | - |
| Package / Case | 780-BBGA, FCBGA |
| Supplier Device Package | 780-FBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/intel/hc1s40f780nad |

Table 2–1 illustrates the differences between HardCopy Stratix and Stratix devices.

*Table 2–1. HardCopy Stratix and Stratix Device Comparison (Part 1 of 2)*

| HardCopy Stratix | Stratix |
|---|---|
| Customized device. All reprogrammability support is removed and no configuration is required. | Re-programmable with configuration is required upon power-up. |
| Average of 50% performance improvement over corresponding FPGA *(1)*. | High-performance FPGA. |
| Average of 40% less power consumption compared to corresponding FPGA *(1)*. | Standard FPGA power consumption. |
| Contact Altera for information regarding specific IP support. | IP support for all devices is available. |
| Double data rate (DDR) SDRAM maximum operating frequency is pending characterization. | DDR SDRAM can operate at 200 MHz for -5 speed grade devices. |
| All routing connections are direct and all unused routing is removed. | MultiTrack™ routing stitches together routing resources to provide a path. |
| HC1S30 and HC1S40 devices have two M-RAM blocks. HC1S80 devices have six M-RAM blocks. | EP1S30 and EP1S40 devices have four M-RAM blocks. EP1S80 devices have nine M-RAM blocks. |
| It is not possible to initialize M512 and M4K RAM contents during power-up. | The contents of M512 and M4K RAM blocks can be preloaded during configuration with data specified in a memory initialization file (**.mif**). |
| The contents of memory output registers are unknown after power-on reset (POR). | The contents of memory output registers are initialized to '0' after POR. |
| HC1S30 and HC1S40 devices have six PLLs. | HC1S30 devices have 10 PLLs. HC1S40 devices have 12 PLLs. |
| PLL dynamic reconfiguration uses ROM for information. This reconfiguration is performed in the back-end and does not affect the migration flow. | PLL dynamic reconfiguration uses a MIF to initialize a RAM resource with information. |
| The I/O elements (IOEs) are equivalent but not identical to FPGA IOEs due to slight design optimizations for HardCopy devices. | The IOEs are optimized for the FPGA architecture. |

Although memory resource implementation is equivalent, the number of specific M-RAM blocks are not necessarily the same between corresponding Stratix and HardCopy Stratix devices. Table 2–3 shows the number of M-RAM blocks available in each device.

*Table 2–3. HardCopy Stratix and Stratix M-RAM Block Comparison*

| HardCopy Stratix | | Stratix | |
|---|---|---|---|
| **Device** | **M-RAM Blocks** | **Device** | **M-RAM Blocks** |
| HC1S25 | 2 | EP1S25 | 2 |
| HC1S30 | 2 | EP1S30 | 4 |
| HC1S40 | 2 | EP1S40 | 4 |
| HC1S60 | 6 | EP1S60 | 6 |
| HC1S830 | 6 | EP1S830 | 9 |

In HardCopy Stratix devices, it is not possible to preload RAM contents using a MIF after powering up; the output registers of memory blocks will have unknown values. This occurs because there is no configuration process that is executed.

Violating the setup or hold time requirements on address registers could corrupt the memory contents. This requirement applies to both read and write operations.

Table 2–4 illustrates the differences between HardCopy Stratix and Stratix memory.

*Table 2–4. HardCopy Stratix and Stratix Memory Comparison*

| HardCopy Stratix | Stratix |
|---|---|
| HC1S30 and HC1S40 devices have two M-RAM blocks. HC1S80 devices have six M-RAM blocks. | EP1S30 and EP1S40 devices have four M-RAM blocks. EP1S80 devices have nine M-RAM blocks. |
| It is not possible to initialize M512 and M4k RAM contents during power-up. | The contents of M512 and M4K RAM blocks can be preloaded during configuration with data specified in a MIF. |
| The contents of memory output registers are unknown after POR. | The contents of memory output registers are initialized to '0' after POR. |

- In instant on mode, the HardCopy Stratix device is available for use shortly after the device receives power. The on-chip POR circuit resets all registers. The CONF_DONE output is tri-stated once the POR has elapsed. No configuration device or configuration data is necessary.
- In instant on after 50 ms mode, the HardCopy Stratix device performs in a fashion similar to the instant on mode, except that there is an additional delay of 50 ms, during which time the device is held in reset stage. The CONF_DONE output is pulled low during this time, and then tri-stated after the 50 ms have elapsed. No configuration device or configuration data is necessary for this option.
- In configuration emulation mode, the HardCopy series device emulates the behavior of an APEX or Stratix FPGA during its configuration phase. When this mode is used, the HardCopy device uses a configuration emulation circuit to receive configuration bit streams. When all the configuration data is received, the HardCopy series device transitions into an initialization phase and releases the CONF_DONE pin to be pulled high. Pulling the CONF_DONE pin high signals that the HardCopy series device is ready for normal operation. If the optional open-drain INIT_DONE output is used, the normal operation is delayed until this signal is released by the HardCopy series device.

HardCopy II and some HardCopy Stratix devices do not support configuration emulation mode.

Instant on and instant on after 50 ms modes are the recommended power-up modes because these modes are similar to an ASIC's functionality upon power-up. No changes to the existing board design or the configuration software are required.

All three modes provide significant benefits to system designers. They enable seamless migration of the design from the FPGA device to the HardCopy device with no changes to the existing board design or the configuration software. The pull-up resistors on *n*CONFIG, *n*STATUS, and CONF_DONE should be left on the printed circuit board.

For more information, refer to the *HardCopy Series Configuration Emulation* chapter in the *HardCopy Series Handbook*.

## Hot Socketing

HardCopy Stratix devices support hot socketing without any external components. In a hot socketing situation, a device's output buffers are turned off during system power up or power down. To simplify board design, HardCopy Stratix devices support any power-up or power-down sequence ($V_{CCIO}$ and $V_{CCINT}$). For mixed-voltage environments, you can

*Table 4–3. HardCopy Stratix Device DC Operating Conditions* *Note (7)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_I$ | Input pin leakage current | $V_I = V_{CCIOmax}$ to 0 V *(8)* | –10 | | 10 | µA |
| $I_{OZ}$ | Tri-stated I/O pin leakage current | $V_O = V_{CCIOmax}$ to 0 V *(8)* | –10 | | 10 | µA |
| $I_{CC0}$ | $V_{CC}$ supply current (standby) (All memory blocks in power-down mode) | $V_I$ = ground, no load, no toggling inputs | | | | mA |
| $R_{CONF}$ | Value of I/O pin pull-up resistor before and during configuration | Vi=0; $V_{CCIO}$ = 3.3 V *(9)* | 15 | 25 | 50 | kΩ |
| | | Vi=0; $V_{CCIO}$ = 2.5 V *(9)* | 20 | 45 | 70 | kΩ |
| | | Vi=0; $V_{CCIO}$ = 1.8 V *(9)* | 30 | 65 | 100 | kΩ |
| | | Vi=0; $V_{CCIO}$ = 1.5 V *(9)* | 50 | 100 | 150 | kΩ |
| | Recommended value of I/O pin external pull-down resistor before and during configuration | | | 1 | 2 | kΩ |

***Notes to Tables 4–1 through 4–3:***

(1) Refer to the *Operating Requirements for Altera Devices* Data Sheet.

(2) Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse affects on the device.

(3) Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.

(4) Maximum $V_{CC}$ rise time is 100 ms, and $V_{CC}$ must rise monotonically.

(5) $V_{CCIO}$ maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.

(6) All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before $V_{CCINT}$ and $V_{CCIO}$ are powered.

(7) Typical values are for $T_A$ = 25 °C, $V_{CCINT}$ = 1.5 V, and $V_{CCIO}$ = 1.5 V, 1.8 V, 2.5 V, and 3.3 V.

(8) This value is specified for normal device operation. The value may vary during power up. This applies for all $V_{CCIO}$ settings (3.3, 2.5, 1.8, and 1.5 V).

(9) Pin pull-up resistance values will be lower if an external source drives the pin higher than $V_{CCIO}$.

*Table 4–10. 3.3-V PCML Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ | Input differential voltage swing | | 300 | | 600 | mV |
| $V_{ICM}$ | Input common mode voltage | | 1.5 | | 3.465 | V |
| $V_{OD}$ | Output differential voltage | | 300 | 370 | 500 | mV |
| $\Delta V_{OD}$ | Change in $V_{OD}$ between high and low | | | | 50 | mV |
| $V_{OCM}$ | Output common mode voltage | | 2.5 | 2.85 | 3.3 | V |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ between high and low | | | | 50 | mV |
| $V_T$ | Output termination voltage | | | $V_{CCIO}$ | | V |
| $R_1$ | Output external pull-up resistors | | 45 | 50 | 55 | Ω |
| $R_2$ | Output external pull-up resistors | | 45 | 50 | 55 | Ω |

*Table 4–11. LVPECL Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | I/O supply voltage | | 3.135 | 3.3 | 3.465 | V |
| $V_{ID}$ | Input differential voltage swing | | 300 | | 1,000 | mV |
| $V_{ICM}$ | Input common mode voltage | | 1 | | 2 | V |
| $V_{OD}$ | Output differential voltage | $R_L$ = 100 Ω | 525 | 700 | 970 | mV |
| $V_{OCM}$ | Output common mode voltage | $R_L$ = 100 Ω | 1.5 | 1.7 | 1.9 | V |
| $R_L$ | Receiver differential input resistor | | 90 | 100 | 110 | Ω |

*Table 4–22. SSTL-3 Class II Specifications (Part 2 of 2)*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH(DC)}$ | High-level DC input voltage | | $V_{REF}$ + 0.2 | | $V_{CCIO}$ + 0.3 | V |
| $V_{IL(DC)}$ | Low-level DC input voltage | | –0.3 | | $V_{REF}$ – 0.2 | V |
| $V_{IH(AC)}$ | High-level AC input voltage | | $V_{REF}$ + 0.4 | | | V |
| $V_{IL(AC)}$ | Low-level AC input voltage | | | | $V_{REF}$ – 0.4 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = –16 mA *(1)* | $V_{TT}$ + 0.8 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 16 mA *(1)* | | | $V_{TT}$ – 0.8 | V |

*Table 4–23. 3.3-V AGP 2× Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{REF}$ | Reference voltage | | 0.39 × $V_{CCIO}$ | | 0.41 × $V_{CCIO}$ | V |
| $V_{IH}$ | High-level input voltage *(4)* | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage *(4)* | | | | 0.3 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –0.5 mA | 0.9 × $V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1.5 mA | | | 0.1 × $V_{CCIO}$ | V |

*Table 4–24. 3.3-V AGP 1× Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 3.15 | 3.3 | 3.45 | V |
| $V_{IH}$ | High-level input voltage *(4)* | | 0.5 × $V_{CCIO}$ | | $V_{CCIO}$ + 0.5 | V |
| $V_{IL}$ | Low-level input voltage *(4)* | | | | 0.3 × $V_{CCIO}$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OUT}$ = –0.5 mA | 0.9 × $V_{CCIO}$ | | 3.6 | V |
| $V_{OL}$ | Low-level output voltage | $I_{OUT}$ = 1.5 mA | | | 0.1 × $V_{CCIO}$ | V |

*Table 4–25. 1.5-V HSTL Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.4 | 1.5 | 1.6 | V |
| $V_{REF}$ | Input reference voltage | | 0.68 | 0.75 | 0.9 | V |
| $V_{TT}$ | Termination voltage | | 0.7 | 0.75 | 0.8 | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.3 | | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 8 mA *(1)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –8 mA *(1)* | | | 0.4 | V |

*Table 4–26. 1.5-V HSTL Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.4 | 1.5 | 1.6 | V |
| $V_{REF}$ | Input reference voltage | | 0.68 | 0.75 | 0.9 | V |
| $V_{TT}$ | Termination voltage | | 0.7 | 0.75 | 0.8 | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF}$ + 0.1 | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.3 | | $V_{REF}$ – 0.1 | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF}$ + 0.2 | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF}$ – 0.2 | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 16 mA *(1)* | $V_{CCIO}$ – 0.4 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –16 mA *(1)* | | | 0.4 | V |

*Table 4–27. 1.8-V HSTL Class I Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.80 | 1.95 | V |
| $V_{REF}$ | Input reference voltage | | 0.70 | 0.90 | 0.95 | V |
| $V_{TT}$ | Termination voltage | | | $V_{CCIO} \times 0.5$ | | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF} + 0.1$ | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.5 | | $V_{REF} – 0.1$ | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF} + 0.2$ | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF} – 0.2$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 8 mA *(1)* | $V_{CCIO} – 0.4$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –8 mA *(1)* | | | 0.4 | V |

*Table 4–28. 1.8-V HSTL Class II Specifications*

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CCIO}$ | Output supply voltage | | 1.65 | 1.80 | 1.95 | V |
| $V_{REF}$ | Input reference voltage | | 0.70 | 0.90 | 0.95 | V |
| $V_{TT}$ | Termination voltage | | | $V_{CCIO} \times 0.5$ | | V |
| $V_{IH}$ (DC) | DC high-level input voltage | | $V_{REF} + 0.1$ | | | V |
| $V_{IL}$ (DC) | DC low-level input voltage | | –0.5 | | $V_{REF} – 0.1$ | V |
| $V_{IH}$ (AC) | AC high-level input voltage | | $V_{REF} + 0.2$ | | | V |
| $V_{IL}$ (AC) | AC low-level input voltage | | | | $V_{REF} – 0.2$ | V |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 16 mA *(1)* | $V_{CCIO} – 0.4$ | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OH}$ = –16 mA *(1)* | | | 0.4 | V |

Tables 4–40 through 4–41 show the external timing parameters on column and row pins for HC1S60 devices.

*Table 4–40. HC1S60 External I/O Timing on Column Pins Using Global Clock Networks*

| Parameter | Performance | | Unit |
|---|---|---|---|
| | Min | Max | |
| $t_{INSU}$ | 2.000 | | ns |
| $t_{INH}$ | 0.000 | | ns |
| $t_{OUTCO}$ | 3.051 | 6.977 | ns |
| $t_{XZ}$ | 2.991 | 6.853 | ns |
| $t_{ZX}$ | 2.991 | 6.853 | ns |
| $t_{INSUPLL}$ | 1.315 | | ns |
| $t_{INHPLL}$ | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.029 | 2.323 | ns |
| $t_{XZPLL}$ | 0.969 | 2.199 | ns |
| $t_{ZXPLL}$ | 0.969 | 2.199 | ns |

*Table 4–41. HC1S60 External I/O Timing on Row Pins Using Global Clock Networks*

| Parameter | Performance | | Unit |
|---|---|---|---|
| | Min | Max | |
| $t_{INSU}$ | 2.232 | | ns |
| $t_{INH}$ | 0.000 | | ns |
| $t_{OUTCO}$ | 3.182 | 7.286 | ns |
| $t_{XZ}$ | 3.209 | 7.354 | ns |
| $t_{ZX}$ | 3.209 | 7.354 | ns |
| $t_{INSUPLL}$ | 1.651 | | ns |
| $t_{INHPLL}$ | 0.000 | | ns |
| $t_{OUTCOPLL}$ | 1.154 | 2.622 | ns |
| $t_{XZPLL}$ | 1.181 | 2.690 | ns |
| $t_{ZXPLL}$ | 1.181 | 2.690 | ns |

Table 4–50 shows the high-speed I/O timing for HardCopy Stratix devices.

*Table 4–50. High-Speed I/O Specifications (Part 1 of 2)* Notes (1), (2)

| Symbol | Conditions | Performance | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| $f_{HSCLK}$ (Clock frequency) (LVDS, LVPECL, HyperTransport technology) $f_{HSCLK} = f_{HSDR} / W$ | $W = 4$ to 30 (Serdes used) | 10 | | 210 | MHz |
| | $W = 2$ (Serdes bypass) | 50 | | 231 | MHz |
| | $W = 2$ (Serdes used) | 150 | | 420 | MHz |
| | $W = 1$ (Serdes bypass) | 100 | | 462 | MHz |
| | $W = 1$ (Serdes used) | 300 | | 717 | MHz |
| $f_{HSDR}$ Device operation (LVDS, LVPECL, HyperTransport technology) | $J = 10$ | 300 | | 840 | Mbps |
| | $J = 8$ | 300 | | 840 | Mbps |
| | $J = 7$ | 300 | | 840 | Mbps |
| | $J = 4$ | 300 | | 840 | Mbps |
| | $J = 2$ | 100 | | 462 | Mbps |
| | $J = 1$ (LVDS and LVPECL only) | 100 | | 462 | Mbps |
| $f_{HSCLK}$ (Clock frequency) (PCML) $f_{HSCLK} = f_{HSDR} / W$ | $W = 4$ to 30 (Serdes used) | 10 | | 100 | MHz |
| | $W = 2$ (Serdes bypass) | 50 | | 200 | MHz |
| | $W = 2$ (Serdes used) | 150 | | 200 | MHz |
| | $W = 1$ (Serdes bypass) | 100 | | 250 | MHz |
| | $W = 1$ (Serdes used) | 300 | | 400 | MHz |
| $f_{HSDR}$ Device operation (PCML) | $J = 10$ | 300 | | 400 | Mbps |
| | $J = 8$ | 300 | | 400 | Mbps |
| | $J = 7$ | 300 | | 400 | Mbps |
| | $J = 4$ | 300 | | 400 | Mbps |
| | $J = 2$ | 100 | | 400 | Mbps |
| | $J = 1$ | 100 | | 250 | Mbps |
| TCCS | All | | | 200 | ps |
| SW | PCML ($J = 4, 7, 8, 10$) | 750 | | | ps |
| | PCML ($J = 2$) | 900 | | | ps |
| | PCML ($J = 1$) | 1,500 | | | ps |
| | LVDS and LVPECL ($J = 1$) | 500 | | | ps |
| | LVDS, LVPECL, HyperTransport technology ($J = 2$ through 10) | 440 | | | ps |

*Table 4–50. High-Speed I/O Specifications (Part 2 of 2) Notes (1), (2)*

| Symbol | Conditions | Performance | | | Unit |
|---|---|---|---|---|---|
| | | Min | Typ | Max | |
| Input jitter tolerance (peak-to-peak) | All | | | 250 | ps |
| Output jitter (peak-to-peak) | All | | | 160 | ps |
| Output $t_{RISE}$ | LVDS | 80 | 110 | 120 | ps |
| | HyperTransport technology | 110 | 170 | 200 | ps |
| | LVPECL | 90 | 130 | 150 | ps |
| | PCML | 80 | 110 | 135 | ps |
| Output $t_{FALL}$ | LVDS | 80 | 110 | 120 | ps |
| | HyperTransport technology | 110 | 170 | 200 | ps |
| | LVPECL | 90 | 130 | 160 | ps |
| | PCML | 105 | 140 | 175 | ps |
| $t_{DUTY}$ | LVDS ($J$ = 2 through 10) | 47.5 | 50 | 52.5 | % |
| | LVDS ($J$ =1) and LVPECL, PCML, HyperTransport technology | 45 | 50 | 55 | % |
| $t_{LOCK}$ | All | | | 100 | µs |

*Notes to Table 4–50:*
(1) When $J$ = 4, 7, 8, and 10, the SERDES block is used.
(2) When $J$ = 2 or $J$ = 1, the SERDES is bypassed.

# PLL Specifications

Table 4–51 describes the HardCopy Stratix device enhanced PLL specifications.

*Table 4–51. Enhanced PLL Specifications (Part 1 of 3)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{IN}$ | Input clock frequency | 3 *(1)* | | 684 | MHz |
| $f_{INDUTY}$ | Input clock duty cycle | 40 | | 60 | % |
| $f_{EINDUTY}$ | External feedback clock input duty cycle | 40 | | 60 | % |
| $t_{INJITTER}$ | Input clock period jitter | | | ±200 *(2)* | ps |
| $t_{EINJITTER}$ | External feedback clock period jitter | | | ±200 *(2)* | ps |
| $t_{FCOMP}$ | External feedback clock compensation time *(3)* | | | 6 | ns |

*Table 4–51. Enhanced PLL Specifications (Part 2 of 3)*

| Symbol | Parameter | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| $f_{OUT}$ | Output frequency for internal global or regional clock | 0.3 | | 500 | MHz |
| $f_{OUT\_EXT}$ | Output frequency for external clock *(2)* | 0.3 | | 526 | MHz |
| $t_{OUTDUTY}$ | Duty cycle for external clock output (when set to 50%) | 45 | | 55 | % |
| $t_{JITTER}$ | Period jitter for external clock output *(5)* | | | ±100 ps for >200 MHz `outclk`<br>±20 mUI for <200 MHz `outclk` | ps or mUI |
| $t_{CONFIG5,6}$ | Time required to reconfigure the scan chains for PLLs 5 and 6 | | | $289/f_{SCANCLK}$ | |
| $t_{CONFIG11,12}$ | Time required to reconfigure the scan chains for PLLs 11 and 12 | | | $193/f_{SCANCLK}$ | |
| $t_{SCANCLK}$ | `scanclk` frequency *(4)* | | | 22 | MHz |
| $t_{DLOCK}$ | Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)* | *(8)* | | 100 | µs |
| $t_{LOCK}$ | Time required to lock from end of device configuration | 10 | | 400 | µs |
| $f_{VCO}$ | PLL internal VCO operating range | 300 | | 800 *(7)* | MHz |
| $t_{LSKEW}$ | Clock skew between two external clock outputs driven by the same counter | | ±50 | | ps |
| $t_{SKEW}$ | Clock skew between two external clock outputs driven by the different counters with the same settings | | ±75 | | ps |
| $f_{SS}$ | Spread spectrum modulation frequency | 30 | | 150 | kHz |
| % spread | Percentage spread for spread spectrum frequency *(9)* | 0.4 | 0.5 | 0.6 | % |

*Table 4–53. Document Revision History (Part 2 of 2)*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| December 2006 v3.2 | Updated chapter number and metadata. | — |
| March 2006 | Formerly chapter 8; no content change. | — |
| October 2005 v3.1 | • Minor edits<br>• Graphic updates | |
| May 2005 v3.0 | • Updated SSTL-2 and SSTL-3 specifications in Tables 8–19 through 8–22<br>• Updated CTT I/O specifications in Table 8–30<br>• Updated bus hold parameters in Table 8–31.<br>• Added the External Timing Parameters, HardCopy Stratix External I/O Timing, and Maximum Input and Output Clock Rates sections<br>• Added the High-Speed I/O Specification, and PLL Specifications sections | — |
| January 2005 v2.0 | Removed recommended maximum rise and fall times ($t_R$ and $t_F$) for input signals | — |
| June 2003 v1.0 | Initial release of Chapter 8, Operating Conditions, in the *HardCopy Device Handbook* | |

# 5. Quartus II Support for HardCopy Stratix Devices

H51014-3.4

## Introduction

Altera® HardCopy devices provide a comprehensive alternative to ASICs. HardCopy structured ASICs offer a complete solution from prototype to high-volume production, and maintain the powerful features and high-performance architecture of their equivalent FPGAs with the programmability removed. You can use the Quartus II design software to design HardCopy devices in a manner similar to the traditional ASIC design flow and you can prototype with Altera's high density Stratix, APEX 20KC, and APEX 20KE FPGAs before seamlessly migrating to the corresponding HardCopy device for high-volume production.

HardCopy structured ASICs provide the following key benefits:

- Improves performance, on the average, by 40% over the corresponding -6 speed grade FPGA device
- Lowers power consumption, on the average, by 40% over the corresponding FPGA
- Preserves the FPGA architecture and features and minimizes risk
- Guarantees first-silicon success through a proven, seamless migration process from the FPGA to the equivalent HardCopy device
- Offers a quick turnaround of the FPGA design to a structured ASIC device—samples are available in about eight weeks

Altera's Quartus II software has built-in support for HardCopy Stratix devices. The HardCopy design flow in Quartus II software offers the following advantages:

- Unified design flow from prototype to production
- Performance estimation of the HardCopy Stratix device allows you to design systems for maximum throughput
- Easy-to-use and inexpensive design tools from a single vendor
- An integrated design methodology that enables system-on-a-chip designs

This section discusses the following areas:

- How to design HardCopy Stratix and HardCopy APEX structured ASICs using the Quartus II software
- An explanation of what the HARDCOPY_FPGA_PROTOTYPE devices are and how to target designs to these devices
- Performance and power estimation of HardCopy Stratix devices
- How to generate the HardCopy design database for submitting HardCopy Stratix and HardCopy APEX designs to the HardCopy Design Center

## Features

Beginning with version 4.2, the Quartus II software contains several powerful features that facilitate design of HardCopy Stratix and HardCopy APEX devices:

- **HARDCOPY_FPGA_PROTOTYPE Devices**
  These are virtual Stratix FPGA devices with features identical to HardCopy Stratix devices. You must use these FPGA devices to prototype your designs and verify the functionality in silicon.

- **HardCopy Timing Optimization Wizard**
  Using this feature, you can target your design to HardCopy Stratix devices, providing an estimate of the design's performance in a HardCopy Stratix device.

- **HardCopy Stratix Floorplans and Timing Models**
  The Quartus II software supports post-migration HardCopy Stratix device floorplans and timing models and facilitates design optimization for design performance.

- **Placement Constraints**
  Location and LogicLock constraints are supported at the HardCopy Stratix floorplan level to improve overall performance.

- **Improved Timing Estimation**
  Beginning with version 4.2, the Quartus II software determines routing and associated buffer insertion for HardCopy Stratix designs, and provides the Timing Analyzer with more accurate information about the delays than was possible in previous versions of the Quartus II software. The Quartus II Archive File automatically receives buffer insertion information, which greatly enhances the timing closure process in the back-end migration of your HardCopy Stratix device.

Stratix FPGA for your design. The three devices are tied together with the same netlist, thus a single SRAM Object File (**.sof**) can be used to achieve the various goals at each stage. The same SRAM Object File is generated in the HARDCOPY_FPGA_PROTOTYPE design, and is used to program the Stratix FPGA device, the same way that it is used to generate the HardCopy Stratix device, guaranteeing a seamless migration.

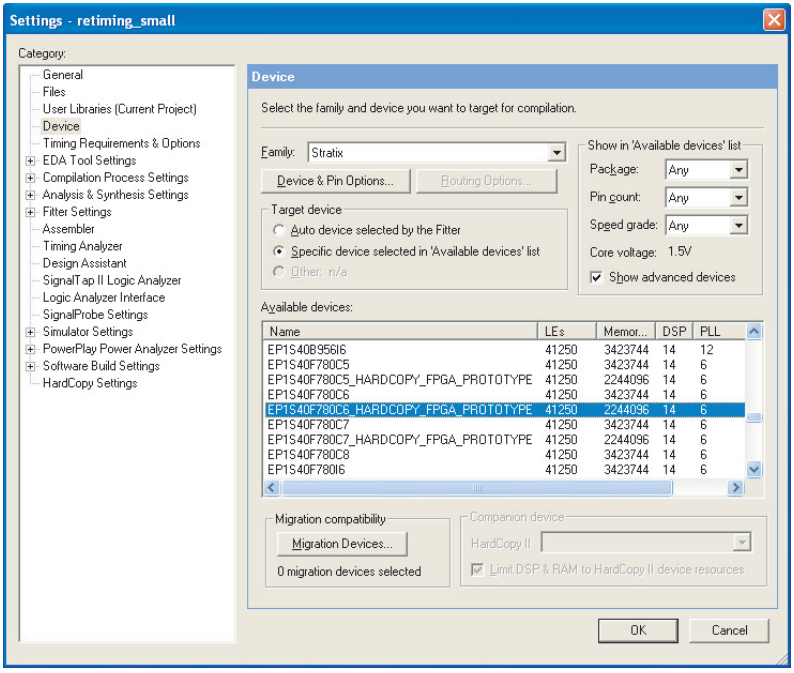
For more information about the SRAM Object File and programming Stratix FPGA devices, refer to the *Programming and Configuration* chapter of the *Introduction to Quartus II Manual*.

## HardCopy Design Flow

Figure 5–1 shows a HardCopy design flow diagram. The design steps are explained in detail in the following sections of this chapter. The HardCopy Stratix design flow utilizes the HardCopy Timing Optimization Wizard to automate the migration process into a one-step process. The remainder of this section explains the tasks performed by this automated process.

For a detailed description of the HardCopy Timing Optimization Wizard and HardCopy Files Wizard, refer to "HardCopy Timing Optimization Wizard Summary" and "Generating the HardCopy Design Database".

*Figure 5–2. Selecting a HARDCOPY_FPGA_PROTOTYPE Device*

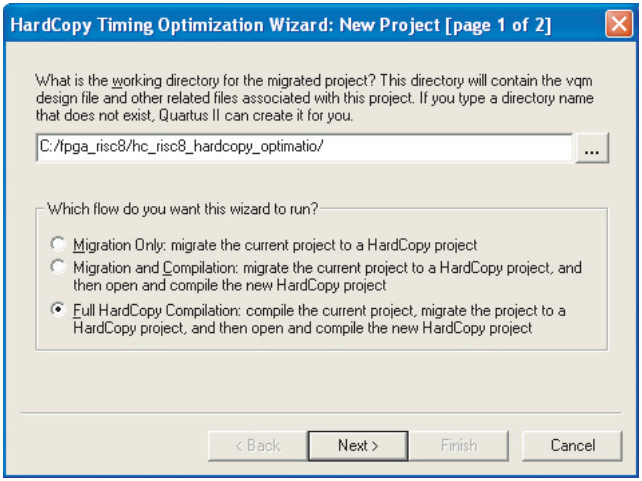



By choosing the HARDCOPY_FPGA_PROTOTYPE device, all the design information, available resources, package option, and pin assignments are constrained to guarantee a seamless migration of your project to the HardCopy Stratix device. The netlist resulting from the HARDCOPY_FPGA_PROTOTYPE device compilation contains information about the electrical connectivity, resources used, I/O placements, and the unused resources in the FPGA device.

4. On the Assignments menu, click **Settings**. In the **Category** list, select **HardCopy Settings** and specify the input transition timing to be modeled for both clock and data input pins. These transition times are used in static timing analysis during back-end timing closure of the HardCopy device.

5. Add constraints to your HARDCOPY_FPGA_PROTOTYPE device, and on the Processing menu, click **Start Compilation** to compile the design.

*Figure 5–3. HardCopy Timing Optimization Wizard Options*




The main benefit of the HardCopy Timing Wizard's three options is flexibility of the conversion process automation. The first time you migrate your HARDCOPY_FPGA_PROTOTYPE project to a HardCopy Stratix device, you may want to use Migration Only, and then work on the HardCopy Stratix project in the Quartus II software. As your prototype FPGA project and HardCopy Stratix project constraints stabilize and you have fewer changes, the Full HardCopy Compilation is ideal for one-click compiling of your HARDCOPY_FPGA_PROTOTYPE and HardCopy Stratix projects.

## Related Documents

For more information, refer to the following documentation:

- The *HardCopy Series Design Guidelines* chapter in volume 1 of the *HardCopy Series Handbook.*
- The *HardCopy Series Back-End Timing Closure* chapter in volume 1 of the *HardCopy Series Handbook.*

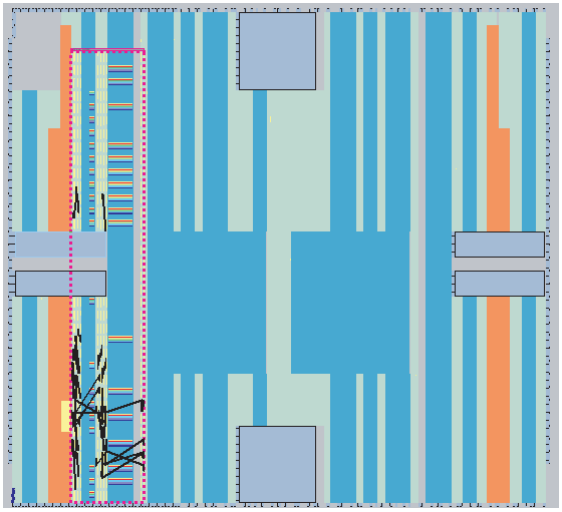
## Document Revision History

Table 5–6 shows the revision history for this chapter.

*Table 5–6. Document Revision History*

| Date and Document Version | Changes Made | Summary of Changes |
|---|---|---|
| September 2008 v3.4 | Updated chapter number and metadata. | — |
| June 2007 v3.3 | Updated with the current Quartus II software version 7.1 information. | — |
| December 2006 v3.2 | Updated revision history. | — |
| March 2006 | Formerly chapter 20; no content change. | — |
| October 2005 v3.1 | • Updated for technical contents for Quartus II 5.1 release<br>• Minor edits | Minor edits. |
| May 2005 v3.0 | Added PowerPlay early Power estimator information. | — |
| January 2005 v2.0 | This revision was previously the *Quartus® II Support for HardCopy Devices* chapter in the *Quartus II Development Software Handbook, v4.1.* | — |
| August 2003 v1.1 | Overall edit; added Tcl script appendix. | — |
| June 2003 v1.0 | Initial release of Chapter 20, Quartus II Support for HardCopy Stratix Devices. | — |

*Figure 6–4. HardCopy Stratix Device Floorplan with Soft Region Off*



## Using Analysis and Synthesis Settings for Performance Improvement

After establishing the baseline for improvement for this design of 65.30 MHz FPGA/88.14 MHz HardCopy, you can gain additional performance improvement in the Stratix FPGA and HardCopy Stratix devices using the available features in the Quartus II software.

Changing the **Analysis & Synthesis Effort** from **Balanced** to **Speed** yields additional benefit in performance, but at the cost of additional LE resources. The Tcl command for this assignment is as follows:

```
set_global_assignment -name
STRATIX_OPTIMIZATION_TECHNIQUE SPEED
```