Intel - HC1S60F1020CA Datasheet

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Details	
Product Status	Obsolete
Number of LABs/CLBs	5712
Number of Logic Elements/Cells	57120
Total RAM Bits	5215104
Number of I/O	782
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/hc1s60f1020ca

Table 2–1 illustrates the differences between HardCopy Stratix and Stratix devices.

Table 2–1. HardCopy Stratix and Stratix Device Comparison (Part 1 of 2)

HardCopy Stratix	Stratix
Customized device. All reprogrammability support is removed and no configuration is required.	Re-programmable with configuration is required upon power-up.
Average of 50% performance improvement over corresponding FPGA *(1)*.	High-performance FPGA.
Average of 40% less power consumption compared to corresponding FPGA *(1)*.	Standard FPGA power consumption.
Contact Altera for information regarding specific IP support.	IP support for all devices is available.
Double data rate (DDR) SDRAM maximum operating frequency is pending characterization.	DDR SDRAM can operate at 200 MHz for -5 speed grade devices.
All routing connections are direct and all unused routing is removed.	MultiTrack™ routing stitches together routing resources to provide a path.
HC1S30 and HC1S40 devices have two M-RAM blocks. HC1S80 devices have six M-RAM blocks.	EP1S30 and EP1S40 devices have four M-RAM blocks. EP1S80 devices have nine M-RAM blocks.
It is not possible to initialize M512 and M4K RAM contents during power-up.	The contents of M512 and M4K RAM blocks can be preloaded during configuration with data specified in a memory initialization file (**.mif**).
The contents of memory output registers are unknown after power-on reset (POR).	The contents of memory output registers are initialized to '0' after POR.
HC1S30 and HC1S40 devices have six PLLs.	HC1S30 devices have 10 PLLs. HC1S40 devices have 12 PLLs.
PLL dynamic reconfiguration uses ROM for information. This reconfiguration is performed in the back-end and does not affect the migration flow.	PLL dynamic reconfiguration uses a MIF to initialize a RAM resource with information.
The I/O elements (IOEs) are equivalent but not identical to FPGA IOEs due to slight design optimizations for HardCopy devices.	The IOEs are optimized for the FPGA architecture.

drive signals into the device before or during power up or power down without damaging the device. HardCopy Stratix devices do not drive out until they have attained proper operating conditions.

You can power up or power down the V_{CCIO} and V_{CCINT} pins in any sequence. The power supply ramp rates can range from 100 ns to 100 ms. During hot socketing, the I/O pin capacitance is less than 15 pF and the clock pin capacitance is less than 20 pF.

- The hot socketing DC specification is $| I_{IOPIN} | < 300$ µA.
- The hot socketing AC specification is $| I_{IOPIN} | < 8$ mA for 10 ns or less. This specification takes into account the pin capacitance only. Additional capacitance for trace, connector, and loading needs to be taken into consideration separately. I_{IOPIN} is the current at any user I/O pin on the device.

The DC specification applies when all V_{CC} supplies to the device are stable in the powered-up or powered-down conditions. For the AC specification, the peak current duration due to power-up transients is 10 ns or less.

HARDCOPY_ FPGA_ PROTOTYPE Devices

HARDCOPY_FPGA_PROTOTYPE devices are Stratix FPGAs available for designers to prototype their HardCopy Stratix designs and perform in-system verification before migration to a HardCopy Stratix device. The HARDCOPY_FPGA_PROTOTYPE devices have the same available resources as in the final HardCopy Stratix devices.

The Quartus II software version 4.1 and later contains the latest timing models. For designs with tight timing constraints, Altera strongly recommends compiling the design with the Quartus II software version 4.1 or later. To properly verify I/O features, it is important to design with the HARDCOPY_FPGA_PROTOTYPE device option prior to migrating to a HardCopy Stratix device.

Table 2–9. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
December 2006 v3.2	Updated revision history.	—
March 2006	Formerly chapter 6; no content change.	—
October 2005 v3.1	• Minor edits • Updated graphics	Minor edits.
May 2005 v3.0	• Added Table 6-1 • Added the Logic Elements section • Added the Embedded Memory section • Added the DSP Blocks section • Added the PLLs and Clock Networks section • Added the I/O Structure and Features section	Minor update.
January 2005 v2.0	• Added summary of I/O and timing differences between Stratix FPGAs and HardCopy Stratix devices • Removed section on Quartus II support of HardCopy Stratix devices • Added "Hot Socketing" section	Minor update.
August 2003 v1.1	Edited section headings' hierarchy.	Minor edits.
June 2003 v1.0	Initial release of Chapter 6, Description, Architecture and Features, in the *HardCopy Device Handbook*	—

Table 3–3. 32-Bit HardCopy Stratix Device IDCODE

Device	IDCODE (32 Bits) *(1)*			
	Version (4 Bits)	Part Number (16 Bits)	Manufacturer Identity (11 Bits)	LSB (1 Bit) *(2)*
HC1S25	0000	0010 0000 0000 0011	000 0110 1110	1
HC1S30	0000	0010 0000 0000 0100	000 0110 1110	1
HC1S40	0000	0010 0000 0000 0101	000 0110 1110	1
HC1S60	0000	0010 0000 0000 0110	000 0110 1110	1
HC1S80	0000	0010 0000 0000 0111	000 0110 1110	1

Notes to Table 3–3:
(1) The most significant bit (MSB) is on the left.
(2) The IDCODE's least significant bit (LSB) is always 1.

Figure 3–1 shows the timing requirements for the JTAG signals.

Figure 3–1. HardCopy Stratix JTAG Waveforms

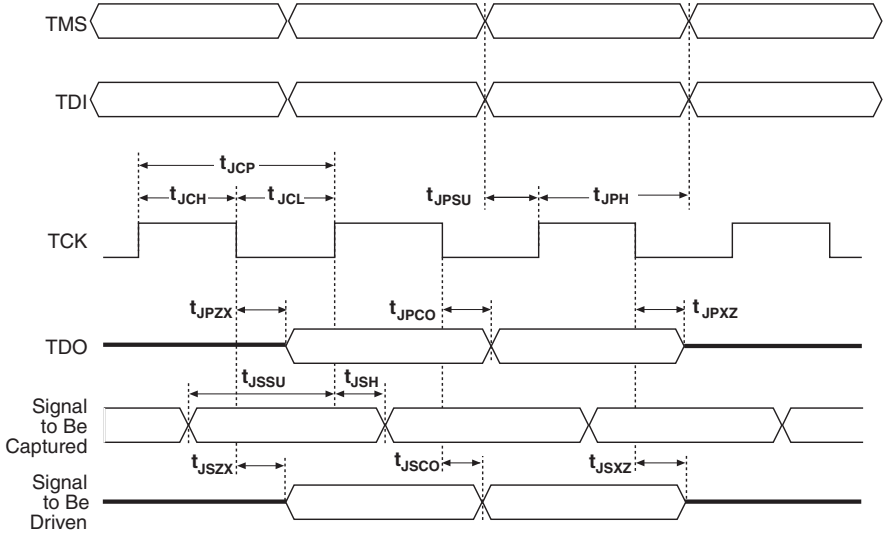


Table 3–5. Document Revision History (Part 2 of 2)

Date and Document Version	Changes Made	Summary of Changes
October 2005 v3.1	• Minor edits • Graphic updates	—
May 2005 v3.0	Updated "IEEE Std. 1149.1 (JTAG) Boundary-Scan Support" section	
January 2005 v2.0	Added information about `USERCODE` registers	
June 2003 v1.0	Initial release of Chapter 7, Boundary-Scan Support, in the *HardCopy Device Handbook*	

Table 4–7. 1.8-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.65	1.95	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	2.25	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 to –8 mA *(1)*	V_{CCIO} – 0.45		V
V_{OL}	Low-level output voltage	I_{OL} = 2 to 8 mA *(1)*		0.45	V

Table 4–8. 1.5-V I/O Specifications

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{CCIO}	Output supply voltage		1.4	1.6	V
V_{IH}	High-level input voltage		0.65 × V_{CCIO}	V_{CCIO} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.35 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OH} = –2 mA *(1)*	0.75 × V_{CCIO}		V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA *(1)*		0.25 × V_{CCIO}	V

Table 4–9. 3.3-V LVDS I/O Specifications (Part 1 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		3.135	3.3	3.465	V
V_{ID}	Input differential voltage swing	0.1 V < V_{CM} < 1.1 V *J* = 1 through 10	300		1,000	mV
		1.1 V ≤ V_{CM} ≤ 1.6 V J = 1	200		1,000	mV
		1.1 V ≤ V_{CM} ≤ 1.6 V *J* = 2 through10	100		1,000	mV
		1.6 V < V_{CM} < 1.8 V *J* = 1 through 10	300		1,000	mV

Table 4–22. SSTL-3 Class II Specifications (Part 2 of 2)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
$V_{IH(DC)}$	High-level DC input voltage		V_{REF} + 0.2		V_{CCIO} + 0.3	V
$V_{IL(DC)}$	Low-level DC input voltage		–0.3		V_{REF} – 0.2	V
$V_{IH(AC)}$	High-level AC input voltage		V_{REF} + 0.4			V
$V_{IL(AC)}$	Low-level AC input voltage				V_{REF} – 0.4	V
V_{OH}	High-level output voltage	I_{OH} = –16 mA *(1)*	V_{TT} + 0.8			V
V_{OL}	Low-level output voltage	I_{OL} = 16 mA *(1)*			V_{TT} – 0.8	V

Table 4–23. 3.3-V AGP 2× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{REF}	Reference voltage		0.39 × V_{CCIO}		0.41 × V_{CCIO}	V
V_{IH}	High-level input voltage *(4)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(4)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			0.1 × V_{CCIO}	V

Table 4–24. 3.3-V AGP 1× Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		3.15	3.3	3.45	V
V_{IH}	High-level input voltage *(4)*		0.5 × V_{CCIO}		V_{CCIO} + 0.5	V
V_{IL}	Low-level input voltage *(4)*				0.3 × V_{CCIO}	V
V_{OH}	High-level output voltage	I_{OUT} = –0.5 mA	0.9 × V_{CCIO}		3.6	V
V_{OL}	Low-level output voltage	I_{OUT} = 1.5 mA			0.1 × V_{CCIO}	V

Table 4–29. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 4–30. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.05	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		V_{REF} + 0.2			V
V_{IL}	Low-level input voltage				V_{REF} – 0.2	V
V_{OH}	High-level output voltage	I_{OH} = –8 mA	V_{REF} + 0.4			V
V_{OL}	Low-level output voltage	I_{OL} = 8 mA			V_{REF} – 0.4	V
I_O	Output leakage current (when output is high *Z*)	GND ≤ V_{OUT} ≤ V_{CCIO}	–10		10	µA

Table 4–31. Bus Hold Parameters

Parameter	Conditions	V_{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V_{IN} > V_{IL} (maximum)	25		30		50		70		µA
High sustaining current	V_{IN} < V_{IH} (minimum)	–25		–30		–50		–70		µA
Low overdrive current	0 V < V_{IN} < V_{CCIO}		160		200		300		500	µA
High overdrive current	0 V < V_{IN} < V_{CCIO}		–160		–200		–300		–500	µA
Bus hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

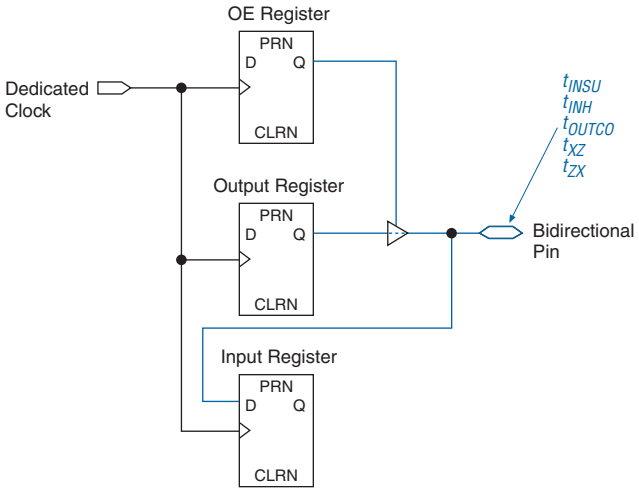
The final timing numbers and actual performance for each HardCopy Stratix design is available when the design migration is complete and are subject to verification and approval by Altera and the designer during the HardCopy Design review process.

For more information, refer to the *HardCopy Series Back-End Timing Closure* chapter in the *HardCopy Series Handbook*.

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–1 shows the pin-to-pin timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 4–1. External Timing in HardCopy Stratix Devices



All external timing parameters reported in this section are defined with respect to the dedicated clock pin as the starting point. All external I/O timing parameters shown are for 3.3-V LVTTL I/O standard with the 4-mA current strength and fast slew rate. For external I/O timing using standards other than LVTTL or for different current strengths, use the I/O standard input and output delay adders in the *Stratix Device Handbook*.

Table 4–33 shows the external I/O timing parameters when using global clock networks.

Table 4–33. HardCopy Stratix Global Clock External I/O Timing Parameters *Notes (1), (2)*

Symbol	Parameter
t_{INSU}	Setup time for input or bidirectional pin using IOE input register with global clock fed by CLK pin
t_{INH}	Hold time for input or bidirectional pin using IOE input register with global clock fed by CLK pin
t_{OUTCO}	Clock-to-output delay output or bidirectional pin using IOE output register with global clock fed by CLK pin
$t_{INSUPLL}$	Setup time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting
t_{INHPLL}	Hold time for input or bidirectional pin using IOE input register with global clock fed by Enhanced PLL with default phase setting
$t_{OUTCOPLL}$	Clock-to-output delay output or bidirectional pin using IOE output register with global clock Enhanced PLL with default phase setting
t_{XZPLL}	Synchronous IOE output enable register to output pin disable delay using global clock fed by Enhanced PLL with default phase setting
t_{ZXPLL}	Synchronous IOE output enable register to output pin enable delay using global clock fed by Enhanced PLL with default phase setting

Notes to Table 4–33:
(1) These timing parameters are sample-tested only.
(2) These timing parameters are for column and row IOE pins. Designers should use the Quartus II software to verify the external timing for any pin.

HardCopy Stratix External I/O Timing

These timing parameters are for both column IOE and row IOE pins. In HC1S30 devices and above, designers can decrease the t_{SU} time by using FPLLCLK, but may get positive hold time in HC1S60 and HC1S80 devices. Designers should use the Quartus II software to verify the external devices for any pin.

Tables 4–38 through 4–39 show the external timing parameters on column and row pins for HC1S40 devices.

Table 4–38. HC1S40 External I/O Timing on Column Pins Using Global Clock Networks

Parameter	Performance		Unit
	Min	Max	
t_{INSU}	2.126		ns
t_{INH}	0.000		ns
t_{OUTCO}	2.856	7.253	ns
t_{XZ}	2.796	7.138	ns
t_{ZX}	2.796	7.138	ns
$t_{INSUPLL}$	1.466		ns
t_{INHPLL}	0.000		ns
$t_{OUTCOPLL}$	1.092	2.473	ns
t_{XZPLL}	1.032	2.358	ns
t_{ZXPLL}	1.032	2.358	ns

Table 4–39. HC1S40 External I/O Timing on Row Pins Using Global Clock Networks

Parameter	Performance		Unit
	Min	Max	
t_{INSU}	2.020		ns
t_{INH}	0.000		ns
t_{OUTCO}	2.912	7.480	ns
t_{XZ}	2.939	7.562	ns
t_{ZX}	2.939	7.562	ns
$t_{INSUPLL}$	1.370		ns
t_{INHPLL}	0.000		ns
$t_{OUTCOPLL}$	1.144	2.693	ns
t_{XZPLL}	1.171	2.775	ns
t_{ZXPLL}	1.171	2.775	ns

Table 4–47. HardCopy Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 2 of 2)

I/O Standard	Performance	Unit
LVDS *(2)*	500	MHz
HyperTransport technology *(2)*	350	MHz

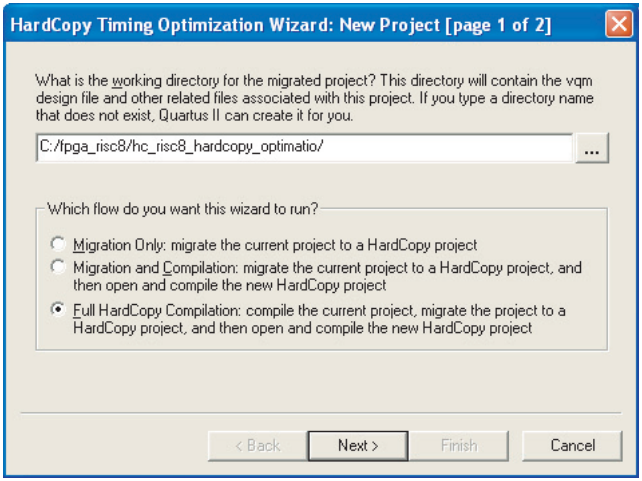
Table 4–48. HardCopy Stratix Maximum Output Clock Rate (Using I/O Pins) for PLL[1, 2, 3, 4] Pins (Part 1 of 2)

I/O Standard	Performance	Unit
LVTTL	400	MHz
2.5 V	400	MHz
1.8 V	400	MHz
1.5 V	350	MHz
LVCMOS	400	MHz
GTL	200	MHz
GTL+	200	MHz
SSTL-3 class I	167	MHz
SSTL-3 class II	167	MHz
SSTL-2 class I	150	MHz
SSTL-2 class II	150	MHz
SSTL-18 class I	150	MHz
SSTL-18 class II	150	MHz
1.5-V HSTL class I	250	MHz
1.5-V HSTL class II	225	MHz
1.8-V HSTL class I	250	MHz
1.8-V HSTL class II	225	MHz
3.3-V PCI	250	MHz
3.3-V PCI-X 1.0	225	MHz
Compact PCI	400	MHz
AGP 1×	400	MHz
AGP 2×	400	MHz
CTT	300	MHz
Differential HSTL	225	MHz
LVPECL *(2)*	717	MHz
PCML *(2)*	420	MHz

Table 4–51. Enhanced PLL Specifications (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{OUT}	Output frequency for internal global or regional clock	0.3		500	MHz
f_{OUT_EXT}	Output frequency for external clock *(2)*	0.3		526	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45		55	%
t_{JITTER}	Period jitter for external clock output *(5)*			±100 ps for >200 MHz `outclk` ±20 mUI for <200 MHz `outclk`	ps or mUI
$t_{CONFIG5,6}$	Time required to reconfigure the scan chains for PLLs 5 and 6			$289/f_{SCANCLK}$	
$t_{CONFIG11,12}$	Time required to reconfigure the scan chains for PLLs 11 and 12			$193/f_{SCANCLK}$	
$t_{SCANCLK}$	`scanclk` frequency *(4)*			22	MHz
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays) *(6)*	*(8)*		100	µs
t_{LOCK}	Time required to lock from end of device configuration	10		400	µs
f_{VCO}	PLL internal VCO operating range	300		800 *(7)*	MHz
t_{LSKEW}	Clock skew between two external clock outputs driven by the same counter		±50		ps
t_{SKEW}	Clock skew between two external clock outputs driven by the different counters with the same settings		±75		ps
f_{SS}	Spread spectrum modulation frequency	30		150	kHz
% spread	Percentage spread for spread spectrum frequency *(9)*	0.4	0.5	0.6	%

Figure 5–3. HardCopy Timing Optimization Wizard Options



The main benefit of the HardCopy Timing Wizard's three options is flexibility of the conversion process automation. The first time you migrate your HARDCOPY_FPGA_PROTOTYPE project to a HardCopy Stratix device, you may want to use Migration Only, and then work on the HardCopy Stratix project in the Quartus II software. As your prototype FPGA project and HardCopy Stratix project constraints stabilize and you have fewer changes, the Full HardCopy Compilation is ideal for one-click compiling of your HARDCOPY_FPGA_PROTOTYPE and HardCopy Stratix projects.

Planning Stratix FPGA Design for HardCopy Stratix Design Conversion

In order to achieve greater performance improvement in your HardCopy Stratix device, additional Quartus II software constraints and placement techniques in the HARDCOPY_FPGA_PROTOTYPE design project may be necessary. This does not mean changing the source hardware description language (HDL) code or functionality, but providing additional constraints in the Quartus II software that specifically impact HardCopy Stratix timing optimization.

Planning ahead for migration to the HardCopy design, while still modifying the HARDCOPY_FPGA_PROTOTYPE design, can improve design performance results. You must anticipate how portions of your FPGA design are placed and connected in the HardCopy device floorplan. The HardCopy device floorplan is smaller than the FPGA device floorplan, allowing use of the customized metal routing in HardCopy Stratix devices.

Partitioning Your Design

Partitioning your design into functional blocks is essential in multi-million gate designs. With a HardCopy Stratix device, you can implement approximately one million ASIC gates of logic. Therefore, Altera recommends hierarchical-design partitioning based on system functions.

When using a hierarchical- or incremental-design methodology, you must consider how your design is partitioned to achieve good results. Altera recommends the following practices for partitioning designs as documented in the *Design Recommendations for Altera Devices* chapter in volume 1 of the *Quartus II Development Software Handbook*:

- Partition your design at functional boundaries.
- Minimize the I/O connections between different partitions.
- Register all inputs and outputs of each block. This makes logic synchronous and avoids glitches and any delay penalty on signals that cross between partitions. Registering I/O pins typically eliminates the need to specify timing requirements for signals that connect between different blocks.
- Do not use glue logic or connection logic between hierarchical blocks. When you preserve hierarchy boundaries, glue logic is not merged with hierarchical blocks. Your synthesis software may optimize glue logic separately, which can degrade synthesis results and is not efficient when used with the LogicLock design methodology.
- Logic is not synthesized or optimized across partition boundaries. Any constant values (for example, signals set to GND), are not propagated across partitions.

turned on by default in the HardCopy Stratix design. While this does allow the Fitter to place all logic in your design with fewer restrictions, it is not optimal for performance improvement in the HardCopy Stratix design.

Recommended LogicLock Settings for HardCopy Stratix Designs

Altera recommends the following LogicLock region settings for the HARDCOPY_FPGA_PROTOTYPE:

- Turn on **Reserve Unused Logic**
- Turn off **Soft Region**
- Select either **Auto** or **Fixed** as the **Size** (design-dependent)
- Select either **Floating** or **Locked** as the **Location** (design-dependent)

When using the **Reserve Unused Logic** setting in a design with high resource utilization (> 95% LE utilization), and a large number of LogicLock regions, the design may not fit in the device. Turning off **Reserve Unused Logic** in less critical LogicLock regions can help Fitter placement. The LEs allowed to float in placement and be packed into unused LEs of LogicLock regions may not be placed optimally after migration to the HardCopy Stratix device since they are merged with other LogicLock regions.

After running the HardCopy Timing Optimization Wizard, the LogicLock region properties are reset to their default conditions. This allows a successful and immediate placement of your design in the Quartus II software. You can further refine the LogicLock region properties for additional benefits.

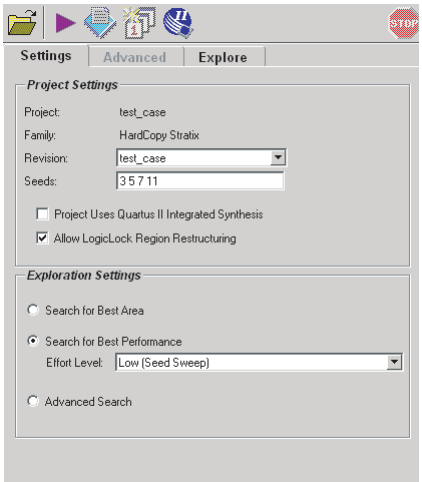
Altera recommends using the following properties for LogicLock regions in the HardCopy design project:

- Turn off **Soft Region**
- Select either **Auto** or **Fixed** as the **Size** after you are satisfied with the placement and timing result of a LogicLock region in a successful HardCopy Stratix compilation
- Select either **Floating** or **Locked** as the **Location** after you are satisfied with the placement and timing results
- **Reserve Unused Logic** is not applicable in the HardCopy Stratix device placement because logic array block (LAB) contents can not be changed after the HardCopy Timing Optimization Wizard is run

An example of a well partitioned design using LogicLock regions effectively for some portions of the design is shown in Figure 6–1. Only the most critical logic functions required are placed in LogicLock regions in order to achieve the desired performance in the HardCopy Stratix

in your open project in the Quartus II software, select **Launch Design Space Explorer** (Tools menu). An example of the DSE GUI and DSE Settings window for the HardCopy Stratix device is shown in Figure 6–2.

Figure 6–2. DSE Settings Window in the DSE GUI



Recommended DSE Settings for HardCopy Stratix Designs

The HardCopy Stratix design does not require all advanced settings or effort-level settings in DSE. Altera recommends using the following settings in DSE for HardCopy Stratix designs:

- In the **Settings** tab (Figure 6–2), make the following selections:
  - Under **Project Settings**, enter several seed numbers in the **Seeds** box. Each seed number requires one full compile of the HardCopy Stratix project.
  - Under **Project Settings**, select **Allow LogicLock Region Restructuring.**
  - Under **Exploration Settings**, select **Search for Best Performance,** and select **Low (Seed Sweep)** from the **Effort Level** menu.
- Turn on **Archive all Compilations** (Options menu).

After running DSE with the seed sweep setting, view the results and identify which seed settings produced the best compilation results. Use the archive of the identified seed, or merge the compilation settings and seed number from the DSE archived project into your primary HardCopy Stratix project.

Performance Improvement Example

With the design used for the performance improvement example in this section, the designer was seeking performance improvement on an HC1S30F780 design for an intellectual property (IP) core consisting of approximately 5200 LEs, 75,000 bits of memory, and two digital signal processing (DSP) multiplier accumulators (MACs). The final application needed to fit in a reserved portion of the HC1S30 device floorplan, so the entire block of IP was initially bounded in a single LogicLock region. The IP block was evaluated as a stand-alone block.

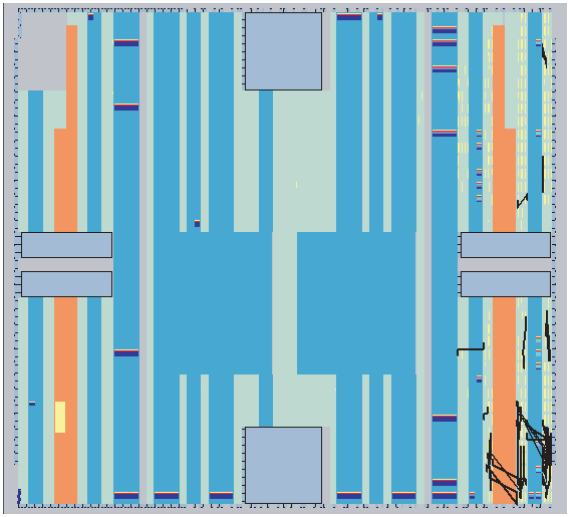
Initial Design Example Settings

The default settings in the Quartus II software version 4.2 were used, with the following initial constraints added:

- The device was set to the target Stratix FPGA device which is the prototype for the HC1S30F780 device:
  ```
  set_global_assignment -name DEVICE
  EP1S30F780C6_HARDCOPY_FPGA_PROTOTYPE
  ```
- A LogicLock region was created for the block to bound it in the reserved region.
- The LogicLock region properties were set to **Auto Size** and **Floating Location**, and **Reserve Unused Logic** was turned on:
  ```
  set_global_assignment -name LL_STATE FLOATING
  set_global_assignment -name LL_AUTO_SIZE ON
  set_global_assignment -name LL_RESERVED OFF
  set_global_assignment -name LL_SOFT OFF
  ```
- Virtual I/O pins were used for the ports of the core since this core does not interface to pins in the parent design, and the I/O pins were placed outside the LogicLock region and are represented as registers in LEs.

The initial compilation results yielded 65.30-MHz f_{MAX} in the FPGA. The block was constrained through virtual I/O pins and a LogicLock region to keep the logic from spreading throughout the floorplan.

Figure 6–3. HardCopy Stratix Device Floorplan with Soft Region On



To keep the LogicLock region contents bounded in the final placement in the HardCopy Stratix device floorplan, turn off the **Soft Region** option. After turning off the **Soft Region** option and compiling the HardCopy Stratix design, the result is an f_{MAX} of 88.14 MHz—a gain of 33% over the Stratix FPGA device performance. The bounded placement in the LogicLock region helps to achieve performance improvement in well-partitioned design blocks by taking advantage of the smaller die size and custom metal routing interconnect of the HardCopy Stratix device. The floorplan of the bounded LogicLock region is visible in Figure 6–4. In this figure, you can see the difference in disabling the Soft Region setting in the HardCopy Stratix design.