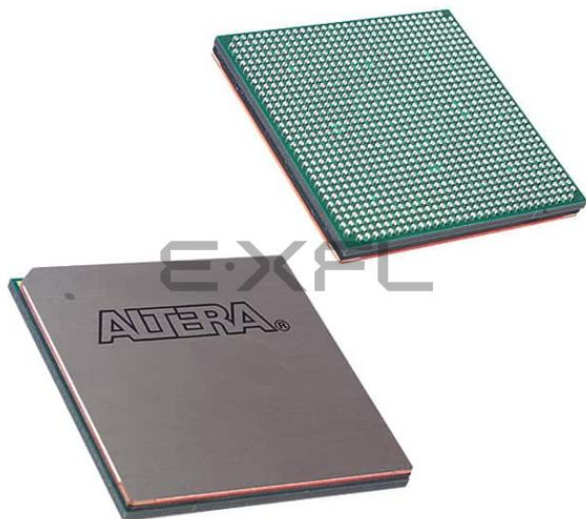




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### Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

|                                |                                                                                                                                   |
|--------------------------------|-----------------------------------------------------------------------------------------------------------------------------------|
| Product Status                 | Obsolete                                                                                                                          |
| Number of LABs/CLBs            | 5712                                                                                                                              |
| Number of Logic Elements/Cells | 57120                                                                                                                             |
| Total RAM Bits                 | 5215104                                                                                                                           |
| Number of I/O                  | 782                                                                                                                               |
| Number of Gates                | -                                                                                                                                 |
| Voltage - Supply               | 1.425V ~ 1.575V                                                                                                                   |
| Mounting Type                  | Surface Mount                                                                                                                     |
| Operating Temperature          | -                                                                                                                                 |
| Package / Case                 | 1020-BBGA                                                                                                                         |
| Supplier Device Package        | 1020-FBGA (33x33)                                                                                                                 |
| Purchase URL                   | <a href="https://www.e-xfl.com/product-detail/intel/hc1s60f1020nam">https://www.e-xfl.com/product-detail/intel/hc1s60f1020nam</a> |

The HardCopy Stratix family consists of base arrays that are common to all designs for a particular device density. Design-specific customization is done within the top two metal layers. The base arrays use an area-efficient sea-of-logic-elements (SOLE) core and extend the flexibility of high-density Stratix FPGAs to a cost-effective, high-volume production solution. With a seamless migration process employed in numerous successful designs, functionality-verified Stratix FPGA designs can be migrated to fixed-function HardCopy Stratix devices with minimal risk and guaranteed first-time success.

The SRAM configuration cells of the original Stratix devices are replaced in HardCopy Stratix devices by metal connects, which define the function of each logic element (LE), digital signal processing (DSP) block, phase-locked loop (PLL), embedded memory, and I/O cell in the device. These resources are interconnected using metallization layers. Once a HardCopy Stratix device has been manufactured, the functionality of the device is fixed and no re-programming is possible. However, as is the case with Stratix FPGAs, the PLLs can be dynamically configured in HardCopy Stratix devices.

## HardCopy Stratix and Stratix FPGA Differences

To ensure HardCopy Stratix device functionality and performance, designers should thoroughly test the original Stratix FPGA-based design for satisfactory results before committing the design for migration to a HardCopy Stratix device. Unlike Stratix FPGAs, HardCopy Stratix devices are customized at the time of manufacturing and therefore do not have programmability support.

Since HardCopy Stratix devices are customized within the top two metal layers, no configuration circuitry is required. Refer to [“Power-Up Modes in HardCopy Stratix Devices” on page 2–7](#) for more information.

Depending on the design, HardCopy Stratix devices can provide, on average, a 50% performance improvement over equivalent Stratix FPGAs. The performance improvement is achieved by die size reduction, metal interconnect optimization, and customized signal buffering. HardCopy Stratix devices consume, on average, 40% less power than their equivalent Stratix FPGAs.



Designers can use the Quartus II software to design HardCopy Stratix devices, estimate performance and power consumption, and maximize system throughput.



Some HARDCOPY\_FPGA\_PROTOTYPE devices, as indicated in [Table 2–8](#), have fewer M-RAM blocks compared to the equivalent Stratix FPGAs. The selective removal of these resources provides a significant price benefit to designers using HardCopy Stratix devices.

**Table 2–8. M-RAM Block Comparison Between Various Devices**

| Number of LEs | HARDCOPY_FPGA_PROTOTYPE Devices |              | HardCopy Stratix Devices |              | Stratix Devices |              |
|---------------|---------------------------------|--------------|--------------------------|--------------|-----------------|--------------|
|               | Device                          | M-RAM Blocks | Device                   | M-RAM Blocks | Device          | M-RAM Blocks |
| 25,660        | EP1S25                          | 2            | HC1S25                   | 2            | EP1S25          | 2            |
| 32,470        | EP1S30                          | 2            | HC1S30                   | 2            | EP1S30          | 4            |
| 41,250        | EP1S40                          | 2            | HC1S40                   | 2            | EP1S40          | 4            |
| 57,120        | EP1S60                          | 6            | HC1S60                   | 6            | EP1S60          | 6            |
| 79,040        | EP1S830                         | 6            | HC1S830                  | 6            | EP1S830         | 9            |



For more information about how the various features in the Quartus II software can be used for designing HardCopy Stratix devices, refer to the *Quartus II Support for HardCopy Stratix Devices* chapter of the *HardCopy Series Handbook*.

HARDCOPY\_FPGA\_PROTOTYPE FPGA devices have the identical speed grade as the equivalent Stratix FPGAs. However, HardCopy Stratix devices are customized and do not have any speed grading. HardCopy Stratix devices, on an average, can be 50% faster than their equivalent HARDCOPY\_FPGA\_PROTOTYPE devices. The actual improvement is design-dependent.

## Document Revision History

[Table 2–9](#) shows the revision history for this chapter.

**Table 2–9. Document Revision History (Part 1 of 2)**

| Date and Document Version | Changes Made                                                                                                                                                                                                             | Summary of Changes |
|---------------------------|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| September 2008 v3.4       | Revised chapter number and metadata.                                                                                                                                                                                     | —                  |
| June 2007 v3.3            | <ul style="list-style-type: none"> <li>Updated <a href="#">Table 2–1</a>.</li> <li>Added note to the “<a href="#">Embedded Memory</a>” section.</li> <li>Updated the “<a href="#">Hot Socketing</a>” section.</li> </ul> | —                  |

**Table 2–9. Document Revision History (Part 2 of 2)**

| Date and Document Version | Changes Made                                                                                                                                                                                                                                                                                                      | Summary of Changes |
|---------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|
| December 2006<br>v3.2     | Updated revision history.                                                                                                                                                                                                                                                                                         | —                  |
| March 2006                | Formerly chapter 6; no content change.                                                                                                                                                                                                                                                                            | —                  |
| October 2005 v3.1         | <ul style="list-style-type: none"> <li>• Minor edits</li> <li>• Updated graphics</li> </ul>                                                                                                                                                                                                                       | Minor edits.       |
| May 2005<br>v3.0          | <ul style="list-style-type: none"> <li>• Added Table 6-1</li> <li>• Added the Logic Elements section</li> <li>• Added the Embedded Memory section</li> <li>• Added the DSP Blocks section</li> <li>• Added the PLLs and Clock Networks section</li> <li>• Added the I/O Structure and Features section</li> </ul> | Minor update.      |
| January 2005<br>v2.0      | <ul style="list-style-type: none"> <li>• Added summary of I/O and timing differences between Stratix FPGAs and HardCopy Stratix devices</li> <li>• Removed section on Quartus II support of HardCopy Stratix devices</li> <li>• Added “Hot Socketing” section</li> </ul>                                          | Minor update.      |
| August 2003<br>v1.1       | Edited section headings’ hierarchy.                                                                                                                                                                                                                                                                               | Minor edits.       |
| June 2003<br>v1.0         | Initial release of Chapter 6, Description, Architecture and Features, in the <i>HardCopy Device Handbook</i>                                                                                                                                                                                                      | —                  |

**Table 3–1. HardCopy Stratix JTAG Instructions (Part 2 of 2)**

| JTAG Instruction | Instruction Code | Description                                                                                                                                                                                                                                                                     |
|------------------|------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| CLAMP (1)        | 00 0000 1010     | Places the 1-bit bypass register between the TDI and TDO pins, which allows the BST data to pass synchronously through selected devices to adjacent devices during normal device operation while holding I/O pins to a state defined by the data in the boundary-scan register. |

Note to Table 3–1:

- (1) Bus hold and weak pull-up resistor features override the high-impedance state of HIGHZ, CLAMP, and EXTEST.



The boundary-scan description language (BSDL) files for HardCopy Stratix devices are different from the corresponding Stratix FPGAs. The BSDL files for HardCopy Stratix devices are available for download from the Altera website at [www.altera.com](http://www.altera.com).

The HardCopy Stratix device instruction register length is 10 bits; the USERCODE register length is 32 bits. The USERCODE registers are mask-programmed, so they are not re-programmable. The designer can choose an appropriate 32-bit sequence to program into the USERCODE registers.

Tables 3–2 and 3–3 show the boundary-scan register length and device IDCODE information for HardCopy Stratix devices.

**Table 3–2. HardCopy Stratix Boundary-Scan Register Length**

| Device                        | Maximum Boundary-Scan Register Length |
|-------------------------------|---------------------------------------|
| HC1S25 672-pin FineLine BGA   | 1,458                                 |
| HC1S30 780-pin FineLine BGA   | 1,878                                 |
| HC1S40 780-pin FineLine BGA   | 1,878                                 |
| HC1S60 1,020-pin FineLine BGA | 2,382                                 |
| HC1S80 1,020-pin FineLine BGA | 2,382                                 |

## Recommended Operating Conditions

Tables 4–1 through 4–3 provide information on absolute maximum ratings, recommended operating conditions, DC operating conditions, and capacitance for 1.5-V HardCopy® Stratix® devices.

**Table 4–1. HardCopy Stratix Device Absolute Maximum Ratings** *Notes (1), (2)*

| Symbol             | Parameter                  | Conditions              | Minimum | Maximum | Unit |
|--------------------|----------------------------|-------------------------|---------|---------|------|
| V <sub>CCINT</sub> | Supply voltage             | With respect to ground  | –0.5    | 2.4     | V    |
| V <sub>CCIO</sub>  |                            |                         | –0.5    | 4.6     | V    |
| V <sub>I</sub>     | DC input voltage (3)       |                         | –0.5    | 4.6     | V    |
| I <sub>OUT</sub>   | DC output current, per pin |                         | –25     | 40      | mA   |
| T <sub>STG</sub>   | Storage temperature        | No bias                 | –65     | 150     | °C   |
| T <sub>J</sub>     | Junction temperature       | BGA packages under bias |         | 135     | °C   |

**Table 4–2. HardCopy Stratix Device Recommended Operating Conditions**

| Symbol             | Parameter                                           | Conditions         | Minimum      | Maximum           | Unit |
|--------------------|-----------------------------------------------------|--------------------|--------------|-------------------|------|
| V <sub>CCINT</sub> | Supply voltage for internal logic and input buffers | (4)                | 1.425        | 1.575             | V    |
| V <sub>CCIO</sub>  | Supply voltage for output buffers, 3.3-V operation  | (4), (5)           | 3.00 (3.135) | 3.60 (3.465)      | V    |
|                    | Supply voltage for output buffers, 2.5-V operation  | (4)                | 2.375        | 2.625             | V    |
|                    | Supply voltage for output buffers, 1.8-V operation  | (4)                | 1.71         | 1.89              | V    |
|                    | Supply voltage for output buffers, 1.5-V operation  | (4)                | 1.4          | 1.6               | V    |
| V <sub>I</sub>     | Input voltage                                       | (3), (6)           | –0.5         | 4.1               | V    |
| V <sub>O</sub>     | Output voltage                                      |                    | 0            | V <sub>CCIO</sub> | V    |
| T <sub>J</sub>     | Operating junction temperature                      | For commercial use | 0            | 85                | °C   |
|                    |                                                     | For industrial use | –40          | 100               | °C   |

**Table 4–12. HyperTransport Technology Specifications**

| Symbol           | Parameter                                | Conditions          | Minimum | Typical | Maximum | Unit     |
|------------------|------------------------------------------|---------------------|---------|---------|---------|----------|
| $V_{CCIO}$       | I/O supply voltage                       |                     | 2.375   | 2.5     | 2.625   | V        |
| $V_{ID}$         | Input differential voltage swing         |                     | 300     |         | 900     | mV       |
| $V_{ICM}$        | Input common mode voltage                |                     | 300     |         | 900     | mV       |
| $V_{OD}$         | Output differential voltage              | $R_L = 100\ \Omega$ | 380     | 485     | 820     | mV       |
| $\Delta V_{OD}$  | Change in $V_{OD}$ between high and low  | $R_L = 100\ \Omega$ |         |         | 50      | mV       |
| $V_{OCM}$        | Output common mode voltage               | $R_L = 100\ \Omega$ | 440     | 650     | 780     | mV       |
| $\Delta V_{OCM}$ | Change in $V_{OCM}$ between high and low | $R_L = 100\ \Omega$ |         |         | 50      | mV       |
| $R_L$            | Receiver differential input resistor     |                     | 90      | 100     | 110     | $\Omega$ |

**Table 4–13. 3.3-V PCI Specifications**

| Symbol     | Parameter                 | Conditions               | Minimum               | Typical | Maximum               | Unit |
|------------|---------------------------|--------------------------|-----------------------|---------|-----------------------|------|
| $V_{CCIO}$ | Output supply voltage     |                          | 3.0                   | 3.3     | 3.6                   | V    |
| $V_{IH}$   | High-level input voltage  |                          | $0.5 \times V_{CCIO}$ |         | $V_{CCIO} + 0.5$      | V    |
| $V_{IL}$   | Low-level input voltage   |                          | –0.5                  |         | $0.3 \times V_{CCIO}$ | V    |
| $V_{OH}$   | High-level output voltage | $I_{OUT} = -500\ \mu A$  | $0.9 \times V_{CCIO}$ |         |                       | V    |
| $V_{OL}$   | Low-level output voltage  | $I_{OUT} = 1,500\ \mu A$ |                       |         | $0.1 \times V_{CCIO}$ | V    |

**Table 4–14. PCI-X 1.0 Specifications**

| Symbol     | Parameter                 | Conditions               | Minimum               | Typical | Maximum                | Unit |
|------------|---------------------------|--------------------------|-----------------------|---------|------------------------|------|
| $V_{CCIO}$ | Output supply voltage     |                          | 3.0                   |         | 3.6                    | V    |
| $V_{IH}$   | High-level input voltage  |                          | $0.5 \times V_{CCIO}$ |         | $V_{CCIO} + 0.5$       | V    |
| $V_{IL}$   | Low-level input voltage   |                          | –0.5                  |         | $0.35 \times V_{CCIO}$ | V    |
| $V_{IPU}$  | Input pull-up voltage     |                          | $0.7 \times V_{CCIO}$ |         |                        | V    |
| $V_{OH}$   | High-level output voltage | $I_{OUT} = -500\ \mu A$  | $0.9 \times V_{CCIO}$ |         |                        | V    |
| $V_{OL}$   | Low-level output voltage  | $I_{OUT} = 1,500\ \mu A$ |                       |         | $0.1 \times V_{CCIO}$  | V    |

**Table 4–15. GTL+ I/O Specifications**

| Symbol    | Parameter                | Conditions                   | Minimum         | Typical | Maximum         | Unit |
|-----------|--------------------------|------------------------------|-----------------|---------|-----------------|------|
| $V_{TT}$  | Termination voltage      |                              | 1.35            | 1.5     | 1.65            | V    |
| $V_{REF}$ | Reference voltage        |                              | 0.88            | 1.0     | 1.12            | V    |
| $V_{IH}$  | High-level input voltage |                              | $V_{REF} + 0.1$ |         |                 | V    |
| $V_{IL}$  | Low-level input voltage  |                              |                 |         | $V_{REF} - 0.1$ | V    |
| $V_{OL}$  | Low-level output voltage | $I_{OL} = 34 \text{ mA}$ (1) |                 |         | 0.65            | V    |

**Table 4–16. GTL I/O Specifications**

| Symbol    | Parameter                | Conditions                   | Minimum          | Typical | Maximum          | Unit |
|-----------|--------------------------|------------------------------|------------------|---------|------------------|------|
| $V_{TT}$  | Termination voltage      |                              | 1.14             | 1.2     | 1.26             | V    |
| $V_{REF}$ | Reference voltage        |                              | 0.74             | 0.8     | 0.86             | V    |
| $V_{IH}$  | High-level input voltage |                              | $V_{REF} + 0.05$ |         |                  | V    |
| $V_{IL}$  | Low-level input voltage  |                              |                  |         | $V_{REF} - 0.05$ | V    |
| $V_{OL}$  | Low-level output voltage | $I_{OL} = 40 \text{ mA}$ (1) |                  |         | 0.4              | V    |

**Table 4–17. SSTL-18 Class I Specifications**

| Symbol       | Parameter                   | Conditions                     | Minimum           | Typical   | Maximum           | Unit |
|--------------|-----------------------------|--------------------------------|-------------------|-----------|-------------------|------|
| $V_{CCIO}$   | Output supply voltage       |                                | 1.65              | 1.8       | 1.95              | V    |
| $V_{REF}$    | Reference voltage           |                                | 0.8               | 0.9       | 1.0               | V    |
| $V_{TT}$     | Termination voltage         |                                | $V_{REF} - 0.04$  | $V_{REF}$ | $V_{REF} + 0.04$  | V    |
| $V_{IH(DC)}$ | High-level DC input voltage |                                | $V_{REF} + 0.125$ |           |                   | V    |
| $V_{IL(DC)}$ | Low-level DC input voltage  |                                |                   |           | $V_{REF} - 0.125$ | V    |
| $V_{IH(AC)}$ | High-level AC input voltage |                                | $V_{REF} + 0.275$ |           |                   | V    |
| $V_{IL(AC)}$ | Low-level AC input voltage  |                                |                   |           | $V_{REF} - 0.275$ | V    |
| $V_{OH}$     | High-level output voltage   | $I_{OH} = -6.7 \text{ mA}$ (1) | $V_{TT} + 0.475$  |           |                   | V    |
| $V_{OL}$     | Low-level output voltage    | $I_{OL} = 6.7 \text{ mA}$ (1)  |                   |           | $V_{TT} - 0.475$  | V    |



**Table 4–25. 1.5-V HSTL Class I Specifications**

| Symbol        | Parameter                   | Conditions                   | Minimum          | Typical | Maximum         | Unit |
|---------------|-----------------------------|------------------------------|------------------|---------|-----------------|------|
| $V_{CCIO}$    | Output supply voltage       |                              | 1.4              | 1.5     | 1.6             | V    |
| $V_{REF}$     | Input reference voltage     |                              | 0.68             | 0.75    | 0.9             | V    |
| $V_{TT}$      | Termination voltage         |                              | 0.7              | 0.75    | 0.8             | V    |
| $V_{IH}$ (DC) | DC high-level input voltage |                              | $V_{REF} + 0.1$  |         |                 | V    |
| $V_{IL}$ (DC) | DC low-level input voltage  |                              | –0.3             |         | $V_{REF} - 0.1$ | V    |
| $V_{IH}$ (AC) | AC high-level input voltage |                              | $V_{REF} + 0.2$  |         |                 | V    |
| $V_{IL}$ (AC) | AC low-level input voltage  |                              |                  |         | $V_{REF} - 0.2$ | V    |
| $V_{OH}$      | High-level output voltage   | $I_{OH} = 8 \text{ mA}$ (1)  | $V_{CCIO} - 0.4$ |         |                 | V    |
| $V_{OL}$      | Low-level output voltage    | $I_{OH} = -8 \text{ mA}$ (1) |                  |         | 0.4             | V    |

**Table 4–26. 1.5-V HSTL Class II Specifications**

| Symbol        | Parameter                   | Conditions                    | Minimum          | Typical | Maximum         | Unit |
|---------------|-----------------------------|-------------------------------|------------------|---------|-----------------|------|
| $V_{CCIO}$    | Output supply voltage       |                               | 1.4              | 1.5     | 1.6             | V    |
| $V_{REF}$     | Input reference voltage     |                               | 0.68             | 0.75    | 0.9             | V    |
| $V_{TT}$      | Termination voltage         |                               | 0.7              | 0.75    | 0.8             | V    |
| $V_{IH}$ (DC) | DC high-level input voltage |                               | $V_{REF} + 0.1$  |         |                 | V    |
| $V_{IL}$ (DC) | DC low-level input voltage  |                               | –0.3             |         | $V_{REF} - 0.1$ | V    |
| $V_{IH}$ (AC) | AC high-level input voltage |                               | $V_{REF} + 0.2$  |         |                 | V    |
| $V_{IL}$ (AC) | AC low-level input voltage  |                               |                  |         | $V_{REF} - 0.2$ | V    |
| $V_{OH}$      | High-level output voltage   | $I_{OH} = 16 \text{ mA}$ (1)  | $V_{CCIO} - 0.4$ |         |                 | V    |
| $V_{OL}$      | Low-level output voltage    | $I_{OH} = -16 \text{ mA}$ (1) |                  |         | 0.4             | V    |

This section discusses the following areas:

- How to design HardCopy Stratix and HardCopy APEX structured ASICs using the Quartus II software
- An explanation of what the `HARDCOPY_FPGA_PROTOTYPE` devices are and how to target designs to these devices
- Performance and power estimation of HardCopy Stratix devices
- How to generate the HardCopy design database for submitting HardCopy Stratix and HardCopy APEX designs to the HardCopy Design Center

## Features

Beginning with version 4.2, the Quartus II software contains several powerful features that facilitate design of HardCopy Stratix and HardCopy APEX devices:

- **HARDCOPY\_FPGA\_PROTOTYPE Devices**  
These are virtual Stratix FPGA devices with features identical to HardCopy Stratix devices. You must use these FPGA devices to prototype your designs and verify the functionality in silicon.
- **HardCopy Timing Optimization Wizard**  
Using this feature, you can target your design to HardCopy Stratix devices, providing an estimate of the design's performance in a HardCopy Stratix device.
- **HardCopy Stratix Floorplans and Timing Models**  
The Quartus II software supports post-migration HardCopy Stratix device floorplans and timing models and facilitates design optimization for design performance.
- **Placement Constraints**  
Location and LogicLock constraints are supported at the HardCopy Stratix floorplan level to improve overall performance.
- **Improved Timing Estimation**  
Beginning with version 4.2, the Quartus II software determines routing and associated buffer insertion for HardCopy Stratix designs, and provides the Timing Analyzer with more accurate information about the delays than was possible in previous versions of the Quartus II software. The Quartus II Archive File automatically receives buffer insertion information, which greatly enhances the timing closure process in the back-end migration of your HardCopy Stratix device.

Stratix FPGA for your design. The three devices are tied together with the same netlist, thus a single SRAM Object File (.sof) can be used to achieve the various goals at each stage. The same SRAM Object File is generated in the HARDCOPY\_FPGA\_PROTOTYPE design, and is used to program the Stratix FPGA device, the same way that it is used to generate the HardCopy Stratix device, guaranteeing a seamless migration.



For more information about the SRAM Object File and programming Stratix FPGA devices, refer to the *Programming and Configuration* chapter of the *Introduction to Quartus II Manual*.

## HardCopy Design Flow

Figure 5–1 shows a HardCopy design flow diagram. The design steps are explained in detail in the following sections of this chapter. The HardCopy Stratix design flow utilizes the HardCopy Timing Optimization Wizard to automate the migration process into a one-step process. The remainder of this section explains the tasks performed by this automated process.



For a detailed description of the HardCopy Timing Optimization Wizard and HardCopy Files Wizard, refer to “HardCopy Timing Optimization Wizard Summary” and “Generating the HardCopy Design Database”.

### *Migrate the Compiled Project*

This step generates the Quartus II Project File (.qpf) and the other files required for HardCopy implementation. The Quartus II software also assigns the appropriate HardCopy Stratix device for the design migration.

### *Close the Quartus FPGA Project*

Because you must compile the project for a HardCopy Stratix device, you must close the existing project which you have targeted your design to a HARDCOPY\_FPGA\_PROTOTYPE device.

### *Open the Quartus HardCopy Project*

Open the Quartus II project that you created in the “[Migrate the Compiled Project](#)” step. The selected device is one of the devices from the HardCopy Stratix family that was assigned during that step.

### *Compile for HardCopy Stratix Device*

Compile the design for a HardCopy Stratix device. After successful compilation, the Timing Analysis section of the compilation report shows the performance of the design implemented in the HardCopy device.

## How to Design HardCopy Stratix Devices

This section describes the process for designing for a HardCopy Stratix device using the HARDCOPY\_FPGA\_PROTOTYPE as your initial selected device. In order to use the HardCopy Timing Optimization Wizard, you must first design with the HARDCOPY\_FPGA\_PROTOTYPE in order for the design to migrate to a HardCopy Stratix device.

To target a design to a HardCopy Stratix device in the Quartus II software, follow these steps:

1. If you have not yet done so, create a new project or open an existing project.
2. On the Assignments menu, click **Settings**. In the **Category** list, select **Device**.
3. On the **Device** page, in the **Family** list, select **Stratix**. Select the desired HARDCOPY\_FPGA\_PROTOTYPE device in the **Available Devices** list ([Figure 5–2](#)).

```
■ quartus_sh --flow hardcopy_full_compile <project_name>  
  [-c <revision>] ←
```

This command performs the following tasks:

- Compiles the existing project for a `HARDCOPY_FPGA_PROTOTYPE` device.
- Migrates the project to a HardCopy Stratix project.
- Opens the migrated HardCopy Stratix project and compiles it for a HardCopy Stratix device.

## Design Optimization and Performance Estimation

The HardCopy Timing Optimization Wizard creates the HardCopy Stratix project in the Quartus II software, where you can perform design optimization and performance estimation of your HardCopy Stratix device.

### Design Optimization

Beginning with version 4.2, the Quartus II software supports HardCopy Stratix design optimization by providing floorplans for placement optimization and HardCopy Stratix timing models. These features allow you to refine placement of logic array blocks (LAB) and optimize the HardCopy design further than the FPGA performance. Customized routing and buffer insertion done in the Quartus II software are then used to estimate the design's performance in the migrated device. The HardCopy device floorplan, routing, and timing estimates in the Quartus II software reflect the actual placement of the design in the HardCopy Stratix device, and can be used to see the available resources, and the location of the resources in the actual device.

### Performance Estimation

**Figure 5–5** illustrates the design flow for estimating performance and optimizing your design. You can target your designs to `HARDCOPY_FPGA_PROTOTYPE` devices, migrate the design to the HardCopy Stratix device, and get placement optimization and timing estimation of your HardCopy Stratix device.

In the event that the required performance is not met, you can:

- Work to improve LAB placement in the HardCopy Stratix project.

*or*



Performance estimation is not supported for HardCopy APEX devices in the Quartus II software. Your design can be optimized by modifying the RTL code or the FPGA design and the constraints. You should contact Altera to discuss any desired performance improvements with HardCopy APEX devices.

## Buffer Insertion

Beginning with version 4.2, the Quartus II software provides improved HardCopy Stratix device timing closure and estimation, to more accurately reflect the results expected after back-end migration. The Quartus II software performs the necessary buffer insertion in your HardCopy Stratix device during the Fitter process, and stores the location of these buffers and necessary routing information in the Quartus II Archive File. This buffer insertion improves the estimation of the Quartus II Timing Analyzer for the HardCopy Stratix device.

## Placement Constraints

Beginning with version 4.2, the Quartus II software supports placement constraints and LogicLock regions for HardCopy Stratix devices. [Figure 5–6](#) shows an iterative process to modify the placement constraints until the best placement for the HardCopy Stratix device is achieved.

### *Design Assistant Settings*

You must select the design rules in the **Design Assistant** page prior to running the design. On the Assignments menu, click **Settings**. In the **Settings** dialog box, in the Category list, select **Design Assistant** and turn on **Run Design Assistant during compilation**. Altera recommends enabling this feature to run the Design Assistant automatically during compilation of your design.

### *Running Design Assistant*

To run Design Assistant independently of other Quartus II features, on the Processing menu, point to Start and click **Start Design Assistant**.

The Design Assistant automatically runs in the background of the Quartus II software when the HardCopy Timing Optimization Wizard is launched, and does not display the Design Assistant results immediately to the display. The design is checked before the Quartus II software migrates the design and creates a new project directory for performing timing analysis.

Also, the Design Assistant runs automatically whenever you generate the HardCopy design database with the HardCopy Files Wizard. The Design Assistant report generated is used by the Altera HardCopy Design Center to review your design.

## **Reports and Summary**

The results of running the Design Assistant on your design are available in the Design Assistant Results section of the Compilation Report. The Design Assistant also generates the summary report in the *<project name>\hardcopy* subdirectory of the project directory. This report file is titled *<project name>\_violations.datasheet*. Reports include the settings, run summary, results summary, and details of the results and messages. The Design Assistant report indicates the rule name, severity of the violation, and the circuit path where any violation occurred.



To learn about the design rules and standard design practices to comply with HardCopy design rules, refer to the Quartus II Help and the *HardCopy Series Design Guidelines* chapter in volume 1 of the *HardCopy Series Handbook*.

## Related Documents

For more information, refer to the following documentation:

- The *HardCopy Series Design Guidelines* chapter in volume 1 of the *HardCopy Series Handbook*.
- The *HardCopy Series Back-End Timing Closure* chapter in volume 1 of the *HardCopy Series Handbook*.

## Document Revision History

Table 5–6 shows the revision history for this chapter.

| <b>Table 5–6. Document Revision History</b> |                                                                                                                                                         |                           |
|---------------------------------------------|---------------------------------------------------------------------------------------------------------------------------------------------------------|---------------------------|
| <b>Date and Document Version</b>            | <b>Changes Made</b>                                                                                                                                     | <b>Summary of Changes</b> |
| September 2008 v3.4                         | Updated chapter number and metadata.                                                                                                                    | —                         |
| June 2007 v3.3                              | Updated with the current Quartus II software version 7.1 information.                                                                                   | —                         |
| December 2006 v3.2                          | Updated revision history.                                                                                                                               | —                         |
| March 2006                                  | Formerly chapter 20; no content change.                                                                                                                 | —                         |
| October 2005 v3.1                           | <ul style="list-style-type: none"> <li>● Updated for technical contents for Quartus II 5.1 release</li> <li>● Minor edits</li> </ul>                    | Minor edits.              |
| May 2005 v3.0                               | Added PowerPlay early Power estimator information.                                                                                                      | —                         |
| January 2005 v2.0                           | This revision was previously the <i>Quartus® II Support for HardCopy Devices</i> chapter in the <i>Quartus II Development Software Handbook, v4.1</i> . | —                         |
| August 2003 v1.1                            | Overall edit; added Tcl script appendix.                                                                                                                | —                         |
| June 2003 v1.0                              | Initial release of Chapter 20, Quartus II Support for HardCopy Stratix Devices.                                                                         | —                         |



Altera recommends physical synthesis optimizations for the `HARDCOPY_FPGA_PROTOTYPE`. The work done in the prototype enhances performance in the HardCopy Stratix device after migration. Duplicating combinational logic and registers can increase area utilization, which limits placement flexibility when designs exceed 95% logic element (LE) utilization. However, duplicating combinational logic and registers can help with performance by allowing critical paths to be duplicated when their endpoints must reach different areas of the device floorplan.



For more information on netlist and design optimization, refer to *Area Optimization and Timing Closure* in volume 2 of the *Quartus II Development Software Handbook*.

## Using LogicLock Regions in HardCopy Stratix Designs

Create LogicLock regions in the `HARDCOPY_FPGA_PROTOTYPE` project and migrate the regions into the HardCopy Stratix optimization project using the Quartus II software. LogicLock regions can provide significant benefits in design performance by carefully isolating critical blocks of logic, including:

- MegaCore® IP functions
- I/O interfaces
- Reset or other critical logic feeding global clock lines
- Partitioned function blocks

You must compile your design initially without LogicLock regions present and review the timing analysis reports to determine if additional constraints or LogicLock regions are necessary. This process allows you to determine which function blocks or data paths require LogicLock regions.

Create LogicLock regions in the `HARDCOPY_FPGA_PROTOTYPE` design project in the Quartus II software. This transfers the LogicLock regions to the HardCopy design project after the HardCopy Timing Optimization Wizard is run. Although the Quartus II software transfers the contents of the LogicLock region, the area, location, and soft boundary settings revert to their default settings in the HardCopy project immediately after the HardCopy Timing Optimization Wizard is run.

If you are using LogicLock regions, Altera recommends you use the **Migration Only** setting in the HardCopy Timing Optimization Wizard to create the HardCopy design project. You should not compile your design automatically using the **Full Compilation** or **Migrate and Compile** options in the wizard. Open the HardCopy design project and verify that the LogicLock region properties meet your desired settings before compiling the HardCopy optimization project. LogicLock soft regions are

## Performance Improvement Example

With the design used for the performance improvement example in this section, the designer was seeking performance improvement on an HC1S30F780 design for an intellectual property (IP) core consisting of approximately 5200 LEs, 75,000 bits of memory, and two digital signal processing (DSP) multiplier accumulators (MACs). The final application needed to fit in a reserved portion of the HC1S30 device floorplan, so the entire block of IP was initially bounded in a single LogicLock region. The IP block was evaluated as a stand-alone block.

### Initial Design Example Settings

The default settings in the Quartus II software version 4.2 were used, with the following initial constraints added:

- The device was set to the target Stratix FPGA device which is the prototype for the HC1S30F780 device:  

```
set_global_assignment -name DEVICE  
EP1S30F780C6_HARDCOPY_FPGA_PROTOTYPE
```
- A LogicLock region was created for the block to bound it in the reserved region.
- The LogicLock region properties were set to **Auto Size** and **Floating Location**, and **Reserve Unused Logic** was turned on:  

```
set_global_assignment -name LL_STATE FLOATING  
set_global_assignment -name LL_AUTO_SIZE ON  
set_global_assignment -name LL_RESERVED OFF  
set_global_assignment -name LL_SOFT OFF
```
- Virtual I/O pins were used for the ports of the core since this core does not interface to pins in the parent design, and the I/O pins were placed outside the LogicLock region and are represented as registers in LEs.

The initial compilation results yielded 65.30-MHz  $f_{MAX}$  in the FPGA. The block was constrained through virtual I/O pins and a LogicLock region to keep the logic from spreading throughout the floorplan.

The initial compile-relevant statistics for this example are provided in [Table 6–1](#).

| <i><b>Table 6–1. Initial Compilation Statistics</b></i> |                       |
|---------------------------------------------------------|-----------------------|
| <b>Result Type</b>                                      | <b>Results</b>        |
| $f_{\text{MAX}}$                                        | 65.30 MHz             |
| Total logic elements (LEs)                              | 5,187/32,470 (15%)    |
| Total LABs                                              | 564/3,247 (17%)       |
| M512 blocks                                             | 20/295 (6%)           |
| M4K blocks                                              | 16/171 (9%)           |
| M-RAM blocks                                            | 0/2 (0%)              |
| Total memory bits                                       | 74,752/2,137,536 (3%) |
| Total RAM block bits                                    | 85,248/2,137,536 (3%) |
| DSP block 9-bit elements                                | 2/96 (2%)             |

The design project was migrated to the HardCopy device using the HardCopy Timing Optimization wizard and was compiled. The default settings of the LogicLock region in a HardCopy Stratix project in the Quartus II software have the **Soft Region** option turned on. With this setting, the HardCopy Stratix compilation yields an  $f_{\text{MAX}}$  of 66.48 MHz, mainly due to the Fitter placement being scattered in an open design ([Figure 6–3](#)). Because the **Soft Region** is set to on, the LogicLock region is not bounded. This is not an optimal placement in the HardCopy Stratix design and is not the best possible performance.

The relevant compilation results of the FPGA are provided in [Table 6–2](#).

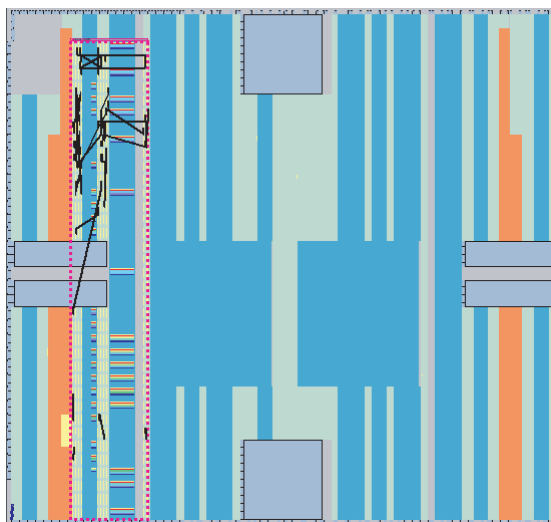
| <b>Table 6–2. Relevant Compile Results</b> |                       |
|--------------------------------------------|-----------------------|
| <b>Result Type</b>                         | <b>Results</b>        |
| $f_{\text{MAX}}$                           | 68.88 MHz             |
| Total logic elements                       | 5,508/32,470 (16%)    |
| Total LABs                                 | 598/3,247 (18%)       |
| M512 blocks                                | 20/295 (6%)           |
| M4K blocks                                 | 16/171 (9%)           |
| M-RAM blocks                               | 0/2 (0%)              |
| Total memory bits                          | 74,752/2,137,536 (3%) |
| Total RAM block bits                       | 85,248/2,137,536 (3%) |
| DSP block 9-bit elements                   | 2/96 (2%)             |

Increasing the LE resources by 6% only yielded an additional 3 MHz in performance in the FPGA, without using additional settings. However, after migrating this design to the HardCopy Stratix design and compiling it, the performance did not improve over the previous HardCopy Stratix design compile, and was slightly worse in performance at 87.34 MHz. This shows that the Quartus II software synthesis was very effective with the **Synthesis Effort Level** set to **Balanced**, and there was only marginal improvement in the FPGA when this option was set to **Speed**.

The next settings activated in this example were the **Synthesis Netlist Optimizations** shown below in Tcl format for WYSIWYG synthesis remapping and gate-level retiming after synthesis mapping:

```
set_global_assignment -name
ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP ON

set_global_assignment -name
ADV_NETLIST_OPT_SYNTH_GATE_RETIME ON
```

**Figure 6–6. Vertically Stretched LogicLock Region**

This floorplan would be better optimized if the LogicLock region had a more square shape, helping the paths that go from memory-to-memory, by containing the M4K and M512 memory blocks in a smaller space, and allowing LAB placement to be adjusted by the Fitter. In the HardCopy Stratix device, signals are routed between LABs, DSP blocks, and memory blocks using the customized metal layers. The reconfigurable routing tracks in the Stratix FPGA device limit the routing paths and delays between elements in the HardCopy Stratix device. This flexibility allows for aspect ratio changes in LogicLock regions, so the raw distance between points becomes the critical factor, and not the usage of available routing resources in the FPGA.

For the final placement optimization in this example, the LogicLock region was fixed in a square region that encompassed two columns of M4K blocks, four columns of M512 blocks, two columns of DSP blocks, and enough LABs to fit the remaining resources required. After compiling the design with these new LogicLock assignments, the performance increased to 93.46 MHz in the HardCopy Stratix device. The critical path and LogicLock region location can be seen in the zoomed-in area of the floorplan (Figure 6–7).

You can see in Figure 6–7 that the critical path shown is from an M4K block to an M512 block through several levels of logic. The placement of the memory blocks can be optimized manually, since the LogicLock region contains more memory blocks than necessary.