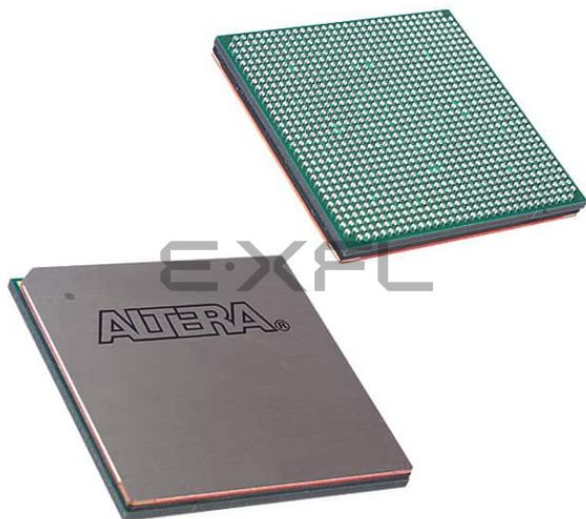




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	7904
Number of Logic Elements/Cells	79040
Total RAM Bits	5658048
Number of I/O	782
Number of Gates	-
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-
Package / Case	1020-BBGA
Supplier Device Package	1020-FBGA (33x33)
Purchase URL	https://www.e-xfl.com/product-detail/intel/hc1s80f1020n



1. Introduction to HardCopy Stratix Devices

H51001-2.4

Introduction

HardCopy® Stratix® structured ASICs, Altera's second-generation HardCopy structured ASICs, are low-cost, high-performance devices with the same architecture as the high-density Stratix FPGAs. The combination of Stratix FPGAs for prototyping and design verification, HardCopy Stratix devices for high-volume production, and the Quartus® II design software beginning with version 3.0, provide a complete and powerful alternative to ASIC design and development.

HardCopy Stratix devices are architecturally equivalent and have the same features as the corresponding Stratix FPGA. They offer pin-to-pin compatibility using the same package as the corresponding Stratix FPGA prototype. Designers can prototype their design to verify functionality with Stratix FPGAs before seamlessly migrating the proven design to a HardCopy Stratix structured ASIC.

The Quartus II software provides a complete set of inexpensive and easy-to-use tools for designing HardCopy Stratix devices. Using the successful and proven methodology from HardCopy APEX™ devices, Stratix FPGA designs can be seamlessly and quickly migrated to a low-cost ASIC alternative. Designers can use the Quartus II software to design HardCopy Stratix devices to obtain an average of 50% higher performance and up to 40% lower power consumption than can be achieved in the corresponding Stratix FPGAs. The migration process is fully automated, requires minimal customer involvement, and takes approximately eight weeks to deliver fully tested HardCopy Stratix prototypes.

The HardCopy Stratix devices use the same base arrays across multiple designs for a given device density and are customized using the top two metal layers. The HardCopy Stratix family consists of the HC1S25, HC1S30, HC1S40, HC1S60, and HC1S80 devices. [Table 1-1](#) provides the details of the HardCopy Stratix devices.

The HardCopy Stratix family consists of base arrays that are common to all designs for a particular device density. Design-specific customization is done within the top two metal layers. The base arrays use an area-efficient sea-of-logic-elements (SOLE) core and extend the flexibility of high-density Stratix FPGAs to a cost-effective, high-volume production solution. With a seamless migration process employed in numerous successful designs, functionality-verified Stratix FPGA designs can be migrated to fixed-function HardCopy Stratix devices with minimal risk and guaranteed first-time success.

The SRAM configuration cells of the original Stratix devices are replaced in HardCopy Stratix devices by metal connects, which define the function of each logic element (LE), digital signal processing (DSP) block, phase-locked loop (PLL), embedded memory, and I/O cell in the device. These resources are interconnected using metallization layers. Once a HardCopy Stratix device has been manufactured, the functionality of the device is fixed and no re-programming is possible. However, as is the case with Stratix FPGAs, the PLLs can be dynamically configured in HardCopy Stratix devices.

HardCopy Stratix and Stratix FPGA Differences

To ensure HardCopy Stratix device functionality and performance, designers should thoroughly test the original Stratix FPGA-based design for satisfactory results before committing the design for migration to a HardCopy Stratix device. Unlike Stratix FPGAs, HardCopy Stratix devices are customized at the time of manufacturing and therefore do not have programmability support.

Since HardCopy Stratix devices are customized within the top two metal layers, no configuration circuitry is required. Refer to [“Power-Up Modes in HardCopy Stratix Devices” on page 2–7](#) for more information.

Depending on the design, HardCopy Stratix devices can provide, on average, a 50% performance improvement over equivalent Stratix FPGAs. The performance improvement is achieved by die size reduction, metal interconnect optimization, and customized signal buffering. HardCopy Stratix devices consume, on average, 40% less power than their equivalent Stratix FPGAs.



Designers can use the Quartus II software to design HardCopy Stratix devices, estimate performance and power consumption, and maximize system throughput.

Although memory resource implementation is equivalent, the number of specific M-RAM blocks are not necessarily the same between corresponding Stratix and HardCopy Stratix devices. Table 2–3 shows the number of M-RAM blocks available in each device.

Table 2–3. HardCopy Stratix and Stratix M-RAM Block Comparison

HardCopy Stratix		Stratix	
Device	M-RAM Blocks	Device	M-RAM Blocks
HC1S25	2	EP1S25	2
HC1S30	2	EP1S30	4
HC1S40	2	EP1S40	4
HC1S60	6	EP1S60	6
HC1S830	6	EP1S830	9

In HardCopy Stratix devices, it is not possible to preload RAM contents using a MIF after powering up; the output registers of memory blocks will have unknown values. This occurs because there is no configuration process that is executed.



Violating the setup or hold time requirements on address registers could corrupt the memory contents. This requirement applies to both read and write operations.

Table 2–4 illustrates the differences between HardCopy Stratix and Stratix memory.

Table 2–4. HardCopy Stratix and Stratix Memory Comparison

HardCopy Stratix	Stratix
HC1S30 and HC1S40 devices have two M-RAM blocks. HC1S80 devices have six M-RAM blocks.	EP1S30 and EP1S40 devices have four M-RAM blocks. EP1S80 devices have nine M-RAM blocks.
It is not possible to initialize M512 and M4k RAM contents during power-up.	The contents of M512 and M4K RAM blocks can be preloaded during configuration with data specified in a MIF.
The contents of memory output registers are unknown after POR.	The contents of memory output registers are initialized to '0' after POR.

When designing with very tight timing constraints (for example, DDR or quad data rate [QDR]), or if using the programmable drive strength option, Altera recommends verifying final drive strength using updated IBIS models located on the Altera website at www.altera.com. Differential I/O standards are unaffected.

I/O pin placement and V_{REF} pin placement rules are identical between HardCopy Stratix and Stratix devices. Unused pin settings will carry over from Stratix device settings and are implemented as tri-stated outputs driving ground or outputs driving V_{CC} .

In Stratix EP1S40 780-pin FineLine BGA FPGAs, the I/O pins U12 and U18 are available as general-purpose I/O pins. In the FPGA prototype, EP1S40F780_HARDCOPY_FPGA_PROTOTYPE, and in the Hardcopy Stratix HC1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 must be connected to ground. HC1S40 780-pin FineLine BGA and EP1S40F780_HARDCOPY_FPGA_PROTOTYPE pin-outs are identical.

Table 2–7 illustrates the differences between HardCopy Stratix and Stratix I/O pins.

Table 2–7. HardCopy Stratix and Stratix I/O Pin Comparison	
HardCopy Stratix	Stratix
The IOEs are equivalent, but not identical to, the FPGA IOEs due to slight design optimizations for HardCopy devices.	IOEs are optimized for the FPGA architecture.
The I/O drive strength for single-ended I/O pins are slightly different and are found in the HardCopy Stratix IBIS models.	The I/O drive strength for single-ended I/O pins are found in Stratix IBIS models.
In the HC1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 must be connected to ground.	In the EP1S40 780-pin FineLine BGA device, the I/O pins U12 and U18 are available as general-purpose I/O pins.

Power-Up Modes in HardCopy Stratix Devices

Designers do not need to configure HardCopy Stratix devices, unlike their FPGA counterparts. However, to facilitate seamless migration, configuration can be emulated in HardCopy Stratix devices.

The modes in which a HardCopy Stratix device can be made ready for operation after power-up are: instant on, instant on after 50 ms, and configuration emulation. These modes are briefly described below.

Table 4–3. HardCopy Stratix Device DC Operating Conditions *Note (7)*

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_I	Input pin leakage current	$V_I = V_{CCIOmax}$ to 0 V (8)	–10		10	μA
I_{OZ}	Tri-stated I/O pin leakage current	$V_O = V_{CCIOmax}$ to 0 V (8)	–10		10	μA
I_{CC0}	V_{CC} supply current (standby) (All memory blocks in power-down mode)	V_I = ground, no load, no toggling inputs				mA
R_{CONF}	Value of I/O pin pull-up resistor before and during configuration	$V_i=0$; $V_{CCIO} = 3.3$ V (9)	15	25	50	$k\Omega$
		$V_i=0$; $V_{CCIO} = 2.5$ V (9)	20	45	70	$k\Omega$
		$V_i=0$; $V_{CCIO} = 1.8$ V (9)	30	65	100	$k\Omega$
		$V_i=0$; $V_{CCIO} = 1.5$ V (9)	50	100	150	$k\Omega$
	Recommended value of I/O pin external pull-down resistor before and during configuration			1	2	$k\Omega$

Notes to Tables 4–1 through 4–3:

- Refer to the *Operating Requirements for Altera Devices* Data Sheet.
- Conditions beyond those listed in Table 4–1 may cause permanent damage to a device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.
- Minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2 V or overshoot to 4.6 V for input currents less than 100 mA and periods shorter than 20 ns.
- Maximum V_{CC} rise time is 100 ms, and V_{CC} must rise monotonically.
- V_{CCIO} maximum and minimum conditions for LVPECL, LVDS, and 3.3-V PCML are shown in parentheses.
- All pins, including dedicated inputs, clock, I/O, and JTAG pins, may be driven before V_{CCINT} and V_{CCIO} are powered.
- Typical values are for $T_A = 25$ °C, $V_{CCINT} = 1.5$ V, and $V_{CCIO} = 1.5$ V, 1.8 V, 2.5 V, and 3.3 V.
- This value is specified for normal device operation. The value may vary during power up. This applies for all V_{CCIO} settings (3.3, 2.5, 1.8, and 1.5 V).
- Pin pull-up resistance values will be lower if an external source drives the pin higher than V_{CCIO} .

Table 4–29. 1.5-V Differential HSTL Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O supply voltage		1.4	1.5	1.6	V
V_{DIF} (DC)	DC input differential voltage		0.2			V
V_{CM} (DC)	DC common mode input voltage		0.68		0.9	V
V_{DIF} (AC)	AC differential input voltage		0.4			V

Table 4–30. CTT I/O Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{CCIO}	Output supply voltage		2.05	3.3	3.6	V
V_{TT}/V_{REF}	Termination and input reference voltage		1.35	1.5	1.65	V
V_{IH}	High-level input voltage		$V_{REF} + 0.2$			V
V_{IL}	Low-level input voltage				$V_{REF} - 0.2$	V
V_{OH}	High-level output voltage	$I_{OH} = -8$ mA	$V_{REF} + 0.4$			V
V_{OL}	Low-level output voltage	$I_{OL} = 8$ mA			$V_{REF} - 0.4$	V
I_O	Output leakage current (when output is high Z)	$GND \leq V_{OUT} \leq V_{CCIO}$	-10		10	μ A

Table 4–31. Bus Hold Parameters

Parameter	Conditions	V _{CCIO} Level								Unit
		1.5 V		1.8 V		2.5 V		3.3 V		
		Min	Max	Min	Max	Min	Max	Min	Max	
Low sustaining current	V _{IN} > V _{IL} (maximum)	25		30		50		70		μA
High sustaining current	V _{IN} < V _{IH} (minimum)	−25		−30		−50		−70		μA
Low overdrive current	0 V < V _{IN} < V _{CCIO}		160		200		300		500	μA
High overdrive current	0 V < V _{IN} < V _{CCIO}		−160		−200		−300		−500	μA
Bus hold trip point		0.5	1.0	0.68	1.07	0.7	1.7	0.8	2.0	V

The final timing numbers and actual performance for each HardCopy Stratix design is available when the design migration is complete and are subject to verification and approval by Altera and the designer during the HardCopy Design review process.

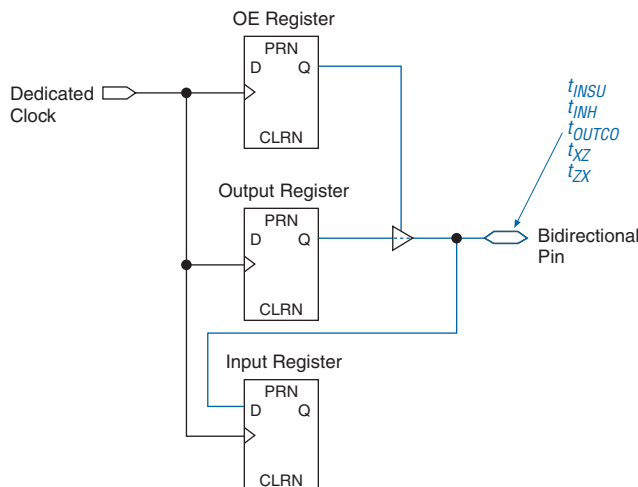


For more information, refer to the *HardCopy Series Back-End Timing Closure* chapter in the *HardCopy Series Handbook*.

External Timing Parameters

External timing parameters are specified by device density and speed grade. Figure 4–1 shows the pin-to-pin timing model for bidirectional IOE pin timing. All registers are within the IOE.

Figure 4–1. External Timing in HardCopy Stratix Devices



All external timing parameters reported in this section are defined with respect to the dedicated clock pin as the starting point. All external I/O timing parameters shown are for 3.3-V LVTTTL I/O standard with the 4-mA current strength and fast slew rate. For external I/O timing using standards other than LVTTTL or for different current strengths, use the I/O standard input and output delay adders in the *Stratix Device Handbook*.

Table 4–45. HardCopy Stratix Maximum Input Clock Rate for CLK[0, 2, 9, 11] Pins and FPLL[10..7]CLK Pins

I/O Standard	Performance	Unit
LVTTL	422	MHz
2.5 V	422	MHz
1.8 V	422	MHz
1.5 V	422	MHz
LVC MOS	422	MHz
GTL	300	MHz
GTL+	300	MHz
SSTL-3 class I	400	MHz
SSTL-3 class II	400	MHz
SSTL-2 class I	400	MHz
SSTL-2 class II	400	MHz
SSTL-18 class I	400	MHz
SSTL-18 class II	400	MHz
1.5-V HSTL class I	400	MHz
1.5-V HSTL class II	400	MHz
1.8-V HSTL class I	400	MHz
1.8-V HSTL class II	400	MHz
3.3-V PCI	422	MHz
3.3-V PCI-X 1.0	422	MHz
Compact PCI	422	MHz
AGP 1×	422	MHz
AGP 2×	422	MHz
CTT	300	MHz
Differential HSTL	400	MHz
LVPECL (1)	717	MHz
PCML (1)	400	MHz
LVDS (1)	717	MHz
HyperTransport technology (1)	717	MHz

Tables 4–47 through 4–48 show the maximum output clock rate for column and row pins in HardCopy Stratix devices.

Table 4–47. HardCopy Stratix Maximum Output Clock Rate for PLL[5, 6, 11, 12] Pins (Part 1 of 2)

I/O Standard	Performance	Unit
LVTTTL	350	MHz
2.5 V	350	MHz
1.8 V	250	MHz
1.5 V	225	MHz
LVC MOS	350	MHz
GTL	200	MHz
GTL+	200	MHz
SSTL-3 class I	200	MHz
SSTL-3 class II	200	MHz
SSTL-2 class I (3)	200	MHz
SSTL-2 class I (4)	200	MHz
SSTL-2 class I (5)	150	MHz
SSTL-2 class II (3)	200	MHz
SSTL-2 class II (4)	200	MHz
SSTL-2 class II (5)	150	MHz
SSTL-18 class I	150	MHz
SSTL-18 class II	150	MHz
1.5-V HSTL class I	250	MHz
1.5-V HSTL class II	225	MHz
1.8-V HSTL class I	250	MHz
1.8-V HSTL class II	225	MHz
3.3-V PCI	350	MHz
3.3-V PCI-X 1.0	350	MHz
Compact PCI	350	MHz
AGP 1×	350	MHz
AGP 2×	350	MHz
CTT	200	MHz
Differential HSTL	225	MHz
Differential SSTL-2 (6)	200	MHz
LVPECL (2)	500	MHz
PCML (2)	350	MHz

Table 4–50. High-Speed I/O Specifications (Part 2 of 2) Notes (1), (2)

Symbol	Conditions	Performance			Unit
		Min	Typ	Max	
Input jitter tolerance (peak-to-peak)	All			250	ps
Output jitter (peak-to-peak)	All			160	ps
Output t_{RISE}	LVDS	80	110	120	ps
	HyperTransport technology	110	170	200	ps
	LVPECL	90	130	150	ps
	PCML	80	110	135	ps
Output t_{FALL}	LVDS	80	110	120	ps
	HyperTransport technology	110	170	200	ps
	LVPECL	90	130	160	ps
	PCML	105	140	175	ps
t_{DUTY}	LVDS ($J = 2$ through 10)	47.5	50	52.5	%
	LVDS ($J = 1$) and LVPECL, PCML, HyperTransport technology	45	50	55	%
t_{LOCK}	All			100	μ s

Notes to Table 4–50:

- (1) When $J = 4, 7, 8$, and 10, the SERDES block is used.
- (2) When $J = 2$ or $J = 1$, the SERDES is bypassed.

PLL Specifications

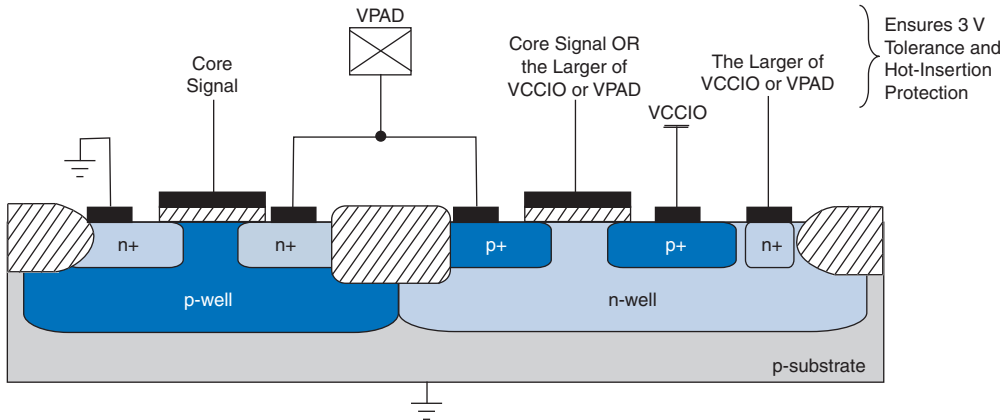
Table 4–51 describes the HardCopy Stratix device enhanced PLL specifications.

Table 4–51. Enhanced PLL Specifications (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency	3 (1)		684	MHz
f_{INDUTY}	Input clock duty cycle	40		60	%
$f_{EINDUTY}$	External feedback clock input duty cycle	40		60	%
$t_{INJITTER}$	Input clock period jitter			± 200 (2)	ps
$t_{EINJITTER}$	External feedback clock period jitter			± 200 (2)	ps
t_{FCOMP}	External feedback clock compensation time (3)			6	ns

Figure 4–2 shows a transistor level cross section of the HardCopy Stratix CMOS I/O buffer structure which will be used to explain ESD protection.

Figure 4–2. Transistor-Level Cross Section of the HardCopy Stratix Device I/O Buffers



The CMOS output drivers in the I/O pins intrinsically provide electrostatic discharge protection. There are two cases to consider for ESD voltage strikes: positive voltage zap and negative voltage zap.

Positive Voltage Zap

A positive ESD voltage zap occurs when a positive voltage is present on an I/O pin due to an ESD charge event. This can cause the N+ (Drain)/P-Substrate) junction of the N-channel drain to break down and the N+ (Drain)/P-Substrate/N+ (Source) intrinsic bipolar transistor turns ON to discharge ESD current from I/O pin to GND.

Table 5–1. Qualitative Comparison of *HARDCOPY_FPGA_PROTOTYPE* to Stratix and HardCopy Stratix Devices (Part 2 of 2)

Stratix Device	<i>HARDCOPY_FPGA_PROTOTYPE</i> Device	HardCopy Stratix Device
FPGA	Resources identical to HardCopy Stratix device	M-RAM resources different than Stratix FPGA in some devices
Ordered through Altera part number	Cannot be ordered, use the Altera Stratix FPGA part number	Ordered by Altera part number

Table 5–2 lists the resources available in each of the HardCopy Stratix devices.

Table 5–2. HardCopy Stratix Device Physical Resources

Device	LEs	ASIC Equivalent Gates (K) ⁽¹⁾	M512 Blocks	M4K Blocks	M-RAM Blocks	DSP Blocks	PLLs	Maximum User I/O Pins
HC1S25F672	25,660	250	224	138	2	10	6	473
HC1S30F780	32,470	325	295	171	2 ⁽²⁾	12	6	597
HC1S40F780	41,250	410	384	183	2 ⁽²⁾	14	6	615
HC1S60F1020	57,120	570	574	292	6	18	12	773
HC1S80F1020	79,040	800	767	364	6 ⁽²⁾	22	12	773

Notes to Table 5–2:

- (1) Combinational and registered logic do not include digital signal processing (DSP) blocks, on-chip RAM, or phase-locked loops (PLLs).
- (2) The M-RAM resources for these HardCopy devices differ from the corresponding Stratix FPGA.

For a given device, the number of available M-RAM blocks in HardCopy Stratix devices is identical with the corresponding *HARDCOPY_FPGA_PROTOTYPE* devices, but may be different from the corresponding Stratix devices. Maintaining the identical resources between *HARDCOPY_FPGA_PROTOTYPE* and HardCopy Stratix devices facilitates seamless migration from the FPGA to the structured ASIC device.



For more information about HardCopy Stratix devices, refer to the *HardCopy Stratix Device Family Data Sheet* section in volume 1 of the *HardCopy Series Handbook*.

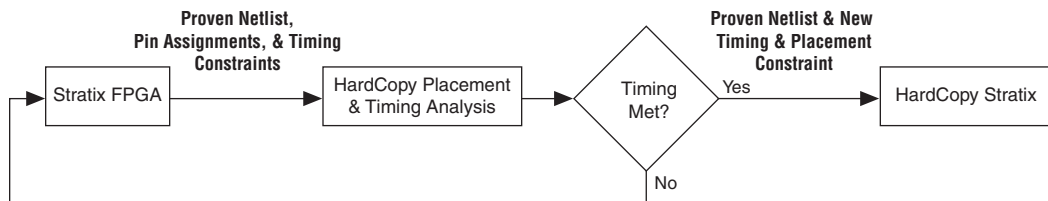
The three devices, Stratix FPGA, *HARDCOPY_FPGA_PROTOTYPE*, and HardCopy device, are distinct devices in the Quartus II software. The *HARDCOPY_FPGA_PROTOTYPE* programming files are used in the

- Go back to the `HARDCOPY_FPGA_PROTOTYPE` project and optimize that design, modify your RTL source code, repeat the migration to the HardCopy Stratix device, and perform the optimization and timing estimation steps.



On average, HardCopy Stratix devices are 40% faster than the equivalent -6 speed grade Stratix FPGA device. These performance numbers are highly design dependent, and you must obtain final performance numbers from Altera.

Figure 5–5. Obtaining a HardCopy Performance Estimation



To perform Timing Analysis for a HardCopy Stratix device, follow these steps:

1. Open an existing project compiled for a `HARDCOPY_FPGA_PROTOTYPE` device.
2. On the Project menu, point to HardCopy Utilities and click **HardCopy Timing Optimization Wizard**.
3. Select a destination directory for the migrated project and complete the HardCopy Timing Optimization Wizard process.

On completion of the HardCopy Timing Optimization Wizard, the destination directory created contains the Quartus II project file, and all files required for HardCopy Stratix implementation. At this stage, the design is copied from the `HARDCOPY_FPGA_PROTOTYPE` project directory to a new directory to perform the timing analysis. This two-project directory structure enables you to move back and forth between the `HARDCOPY_FPGA_PROTOTYPE` design database and the HardCopy Stratix design database. The Quartus II software creates the `<project name>_hardcopy_optimization` directory.

You do not have to select the HardCopy Stratix device while performing performance estimation. When you run the HardCopy Timing Optimization Wizard, the Quartus II software selects the



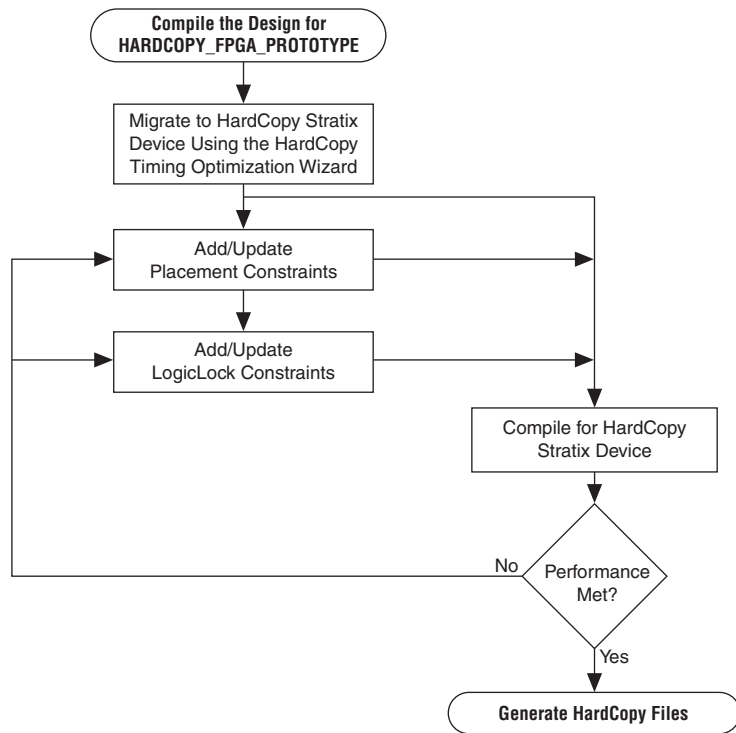
Performance estimation is not supported for HardCopy APEX devices in the Quartus II software. Your design can be optimized by modifying the RTL code or the FPGA design and the constraints. You should contact Altera to discuss any desired performance improvements with HardCopy APEX devices.

Buffer Insertion

Beginning with version 4.2, the Quartus II software provides improved HardCopy Stratix device timing closure and estimation, to more accurately reflect the results expected after back-end migration. The Quartus II software performs the necessary buffer insertion in your HardCopy Stratix device during the Fitter process, and stores the location of these buffers and necessary routing information in the Quartus II Archive File. This buffer insertion improves the estimation of the Quartus II Timing Analyzer for the HardCopy Stratix device.

Placement Constraints

Beginning with version 4.2, the Quartus II software supports placement constraints and LogicLock regions for HardCopy Stratix devices. [Figure 5–6](#) shows an iterative process to modify the placement constraints until the best placement for the HardCopy Stratix device is achieved.

Figure 5–6. Placement Constraints Flow for HardCopy Stratix Devices

Location Constraints

This section provides information about HardCopy Stratix logic location constraints.

LAB Assignments

Logic placement in HardCopy Stratix is limited to LAB placement and optimization of the interconnecting signals between them. In a Stratix FPGA, individual logic elements (LE) are placed by the Quartus II Fitter into LABs. The HardCopy Stratix migration process requires that LAB contents cannot change after the Timing Optimization Wizard task is done. Therefore, you can only make LAB-level placement optimization and location assignments after migrating the `HARDCOPY_FPGA_PROTOTYPE` project to the HardCopy Stratix device.

turned on by default in the HardCopy Stratix design. While this does allow the Fitter to place all logic in your design with fewer restrictions, it is not optimal for performance improvement in the HardCopy Stratix design.

Recommended LogicLock Settings for HardCopy Stratix Designs

Altera recommends the following LogicLock region settings for the `HARDCOPY_FPGA_PROTOTYPE`:

- Turn on **Reserve Unused Logic**
- Turn off **Soft Region**
- Select either **Auto** or **Fixed** as the **Size** (design-dependent)
- Select either **Floating** or **Locked** as the **Location** (design-dependent)

When using the **Reserve Unused Logic** setting in a design with high resource utilization (> 95% LE utilization), and a large number of LogicLock regions, the design may not fit in the device. Turning off **Reserve Unused Logic** in less critical LogicLock regions can help Fitter placement. The LEs allowed to float in placement and be packed into unused LEs of LogicLock regions may not be placed optimally after migration to the HardCopy Stratix device since they are merged with other LogicLock regions.

After running the HardCopy Timing Optimization Wizard, the LogicLock region properties are reset to their default conditions. This allows a successful and immediate placement of your design in the Quartus II software. You can further refine the LogicLock region properties for additional benefits.

Altera recommends using the following properties for LogicLock regions in the HardCopy design project:

- Turn off **Soft Region**
- Select either **Auto** or **Fixed** as the **Size** after you are satisfied with the placement and timing result of a LogicLock region in a successful HardCopy Stratix compilation
- Select either **Floating** or **Locked** as the **Location** after you are satisfied with the placement and timing results
- **Reserve Unused Logic** is not applicable in the HardCopy Stratix device placement because logic array block (LAB) contents can not be changed after the HardCopy Timing Optimization Wizard is run

An example of a well partitioned design using LogicLock regions effectively for some portions of the design is shown in [Figure 6–1](#). Only the most critical logic functions required are placed in LogicLock regions in order to achieve the desired performance in the HardCopy Stratix

Performance Improvement Example

With the design used for the performance improvement example in this section, the designer was seeking performance improvement on an HC1S30F780 design for an intellectual property (IP) core consisting of approximately 5200 LEs, 75,000 bits of memory, and two digital signal processing (DSP) multiplier accumulators (MACs). The final application needed to fit in a reserved portion of the HC1S30 device floorplan, so the entire block of IP was initially bounded in a single LogicLock region. The IP block was evaluated as a stand-alone block.

Initial Design Example Settings

The default settings in the Quartus II software version 4.2 were used, with the following initial constraints added:

- The device was set to the target Stratix FPGA device which is the prototype for the HC1S30F780 device:

```
set_global_assignment -name DEVICE  
EP1S30F780C6_HARDCOPY_FPGA_PROTOTYPE
```
- A LogicLock region was created for the block to bound it in the reserved region.
- The LogicLock region properties were set to **Auto Size** and **Floating Location**, and **Reserve Unused Logic** was turned on:

```
set_global_assignment -name LL_STATE FLOATING  
set_global_assignment -name LL_AUTO_SIZE ON  
set_global_assignment -name LL_RESERVED OFF  
set_global_assignment -name LL_SOFT OFF
```
- Virtual I/O pins were used for the ports of the core since this core does not interface to pins in the parent design, and the I/O pins were placed outside the LogicLock region and are represented as registers in LEs.

The initial compilation results yielded 65.30-MHz f_{MAX} in the FPGA. The block was constrained through virtual I/O pins and a LogicLock region to keep the logic from spreading throughout the floorplan.

The relevant compilation results of the FPGA are provided in [Table 6–2](#).

Table 6–2. Relevant Compile Results	
Result Type	Results
f_{MAX}	68.88 MHz
Total logic elements	5,508/32,470 (16%)
Total LABs	598/3,247 (18%)
M512 blocks	20/295 (6%)
M4K blocks	16/171 (9%)
M-RAM blocks	0/2 (0%)
Total memory bits	74,752/2,137,536 (3%)
Total RAM block bits	85,248/2,137,536 (3%)
DSP block 9-bit elements	2/96 (2%)

Increasing the LE resources by 6% only yielded an additional 3 MHz in performance in the FPGA, without using additional settings. However, after migrating this design to the HardCopy Stratix design and compiling it, the performance did not improve over the previous HardCopy Stratix design compile, and was slightly worse in performance at 87.34 MHz. This shows that the Quartus II software synthesis was very effective with the **Synthesis Effort Level** set to **Balanced**, and there was only marginal improvement in the FPGA when this option was set to **Speed**.

The next settings activated in this example were the **Synthesis Netlist Optimizations** shown below in Tcl format for WYSIWYG synthesis remapping and gate-level retiming after synthesis mapping:

```
set_global_assignment -name
ADV_NETLIST_OPT_SYNTH_WYSIWYG_REMAP ON

set_global_assignment -name
ADV_NETLIST_OPT_SYNTH_GATE_RETIME ON
```