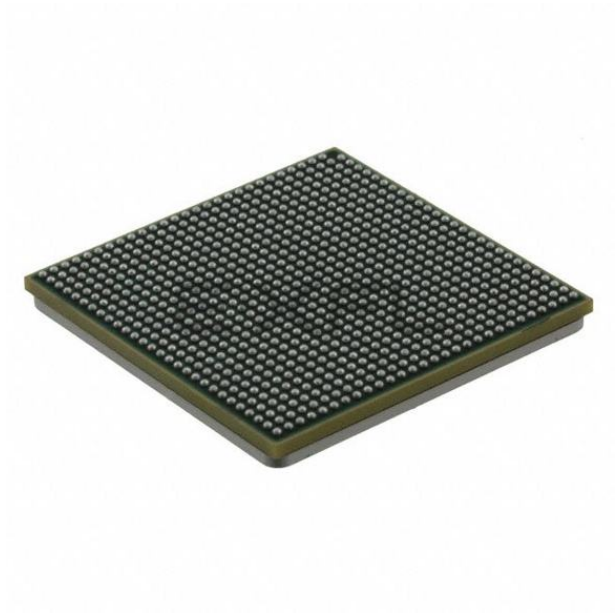

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## Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

## Applications of Embedded - DSP (Digital Signal Processors)

| Details | |
|---|---|
| Product Status | Obsolete |
| Type | SC3850 Dual Core |
| Interface | Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART |
| Clock Rate | 1GHz |
| Non-Volatile Memory | ROM (96kB) |
| On-Chip RAM | 576kB |
| Voltage - I/O | 2.50V |
| Voltage - Core | 1.00V |
| Operating Temperature | 0°C ~ 105°C (TJ) |
| Mounting Type | Surface Mount |
| Package / Case | 783-BBGA, FCBGA |
| Supplier Device Package | 783-FCPBGA (29x29) |
| Purchase URL | https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8252sag1000b |

# Table of Contents



## List of Figures

# 1 Pin Assignment

This section includes diagrams of the MSC8252 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

## 1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

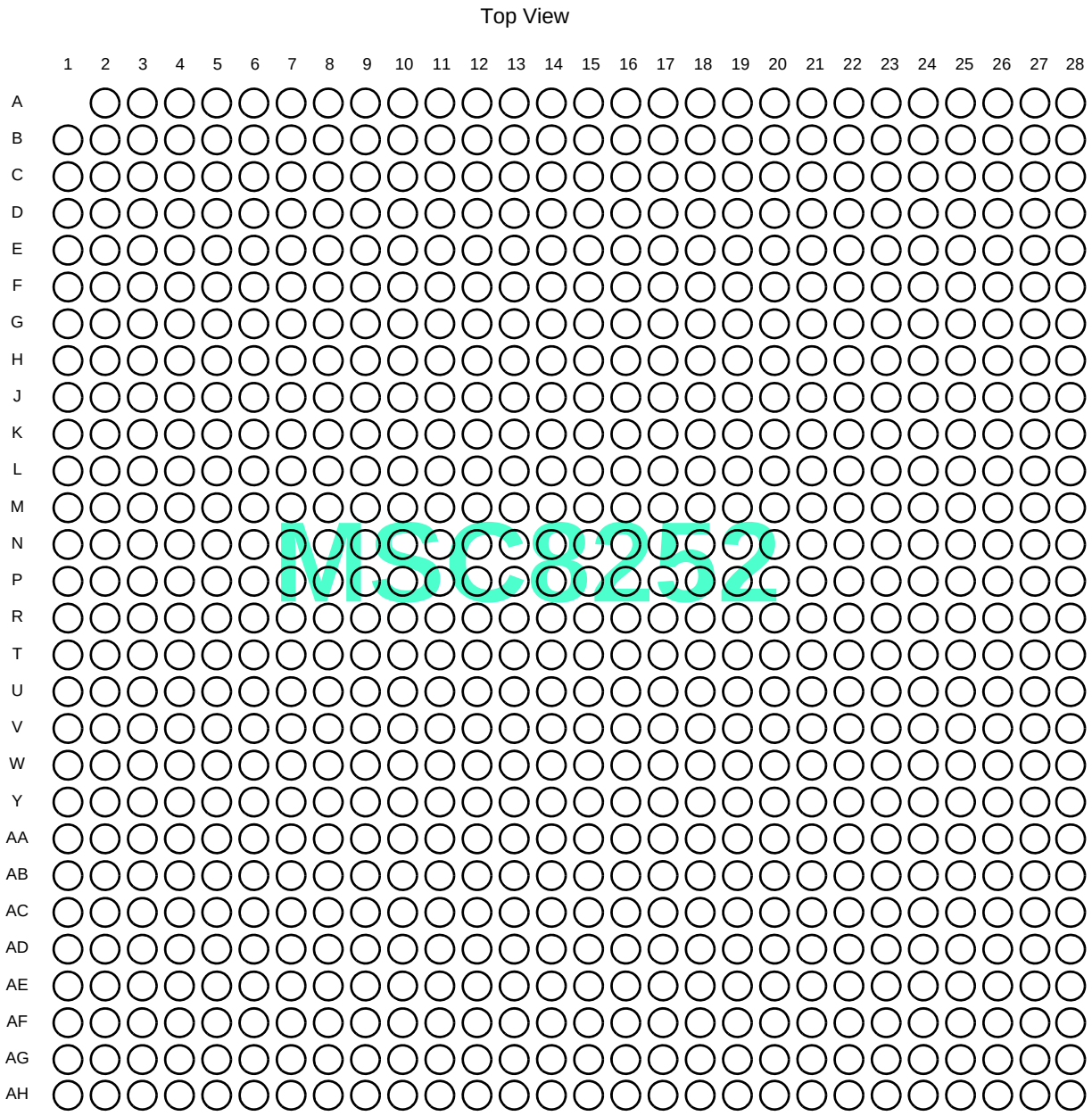


**Figure 3. MSC8252 FC-PBGA Package, Top View**

## Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name[1,2] | Pin Type[10] | Power Rail Name |
|---|---|---|---|
| N23 | SR2_TXD2/PE_TXD2/SG1_TX[4] | O | SXPVDD2 |
| N24 | $\overline{\text{SR2\_TXD2}}$/PE_TXD2/$\overline{\text{SG1\_TX}}$[4] | O | SXPVDD2 |
| N25 | SXCVDD2 | Power | N/A |
| N26 | SXCVSS2 | Ground | N/A |
| N27 | $\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4] | I | SXCVDD2 |
| N28 | SR2_RXD2/PE_RXD2/SG1_RX[4] | I | SXCVDD2 |
| P1 | CLKIN | I | QVDD |
| P2 | EE0 | I | QVDD |
| P3 | QVDD | Power | N/A |
| P4 | VSS | Ground | N/A |
| P5 | STOP_BS | I | QVDD |
| P6 | QVDD | Power | N/A |
| P7 | VSS | Ground | N/A |
| P8 | PLL0_AVDD[9] | Power | VDD |
| P9 | PLL2_AVDD[9] | Power | VDD |
| P10 | VSS | Ground | N/A |
| P11 | VDD | Power | N/A |
| P12 | VSS | Ground | N/A |
| P13 | VDD | Power | N/A |
| P14 | VSS | Ground | N/A |
| P15 | VSS | Ground | N/A |
| P16 | VSS | Ground | N/A |
| P17 | VSS | Ground | N/A |
| P18 | VSS | Ground | N/A |
| P19 | VDD | Power | N/A |
| P20 | Reserved | NC | — |
| P21 | Reserved | NC | — |
| P22 | Reserved | NC | — |
| P23 | SXPVDD2 | Power | N/A |
| P24 | SXPVSS2 | Ground | N/A |
| P25 | SR2_PLL_AGND[9] | Ground | SXCVSS2 |
| P26 | SR2_PLL_AVDD[9] | Power | SXCVDD2 |
| P27 | SXCVSS2 | Ground | N/A |
| P28 | SXCVDD2 | Power | N/A |
| R1 | VSS | Ground | N/A |
| R2 | $\overline{\text{NMI}}$ | I | QVDD |
| R3 | $\overline{\text{NMI\_OUT}}$[6] | O | QVDD |
| R4 | $\overline{\text{HRESET}}$[6,7] | I/O | QVDD |
| R5 | $\overline{\text{INT\_OUT}}$[6] | O | QVDD |
| R6 | EE1 | O | QVDD |
| R7 | VSS | Ground | N/A |
| R8 | PLL1_AVDD[9] | Power | VDD |
| R9 | VSS | Ground | N/A |
| R10 | VDD | Power | N/A |
| R11 | VSS | Non-user | N/A |
| R12 | VDD | Power | N/A |

## Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name[1,2] | Pin Type[10] | Power Rail Name |
|---|---|---|---|
| U3 | GVDD1 | Power | N/A |
| U4 | M1DQ15 | I/O | GVDD1 |
| U5 | M1DQ1 | I/O | GVDD1 |
| U6 | VSS | Ground | N/A |
| U7 | GVDD1 | Power | N/A |
| U8 | M1DQ7 | I/O | GVDD1 |
| U9 | M1DQ6 | I/O | GVDD1 |
| U10 | VDD | Power | N/A |
| U11 | VSS | Ground | N/A |
| U12 | M3VDD | Power | N/A |
| U13 | VSS | Ground | N/A |
| U14 | VDD | Power | N/A |
| U15 | VSS | Ground | N/A |
| U16 | VDD | Power | N/A |
| U17 | VSS | Ground | N/A |
| U18 | VDD | Power | N/A |
| U19 | VSS | Ground | N/A |
| U20 | VSS | Ground | N/A |
| U21 | VSS | Ground | N/A |
| U22 | VSS | Non-user | N/A |
| U23 | SR2_TXD0/PE_TXD0[4] | O | SXPVDD2 |
| U24 | $\overline{\text{SR2\_TXD0}}/\overline{\text{PE\_TXD0}}$[4] | O | SXPVDD2 |
| U25 | SXCVDD2 | Power | N/A |
| U26 | SXCVSS2 | Ground | N/A |
| U27 | $\overline{\text{SR2\_RXD0}}/\overline{\text{PE\_RXD0}}$[4] | I | SXCVDD2 |
| U28 | SR2_RXD0/PE_RXD0[4] | I | SXCVDD2 |
| V1 | M1DQ9 | I/O | GVDD1 |
| V2 | M1DQ12 | I/O | GVDD1 |
| V3 | M1DQ13 | I/O | GVDD1 |
| V4 | $\overline{\text{M1DQS0}}$ | I/O | GVDD1 |
| V5 | M1DQS0 | I/O | GVDD1 |
| V6 | M1DM0 | O | GVDD1 |
| V7 | M1DQ3 | I/O | GVDD1 |
| V8 | M1DQ2 | I/O | GVDD1 |
| V9 | M1DQ4 | I/O | GVDD1 |
| V10 | VSS | Ground | N/A |
| V11 | VDD | Power | N/A |
| V12 | VSS | Ground | N/A |
| V13 | VDD | Power | N/A |
| V14 | VSS | Ground | N/A |
| V15 | VDD | Power | N/A |
| V16 | VSS | Ground | N/A |
| V17 | VDD | Power | N/A |
| V18 | VSS | Ground | N/A |
| V19 | VDD | Power | N/A |
| V20 | NVDD | Power | N/A |

## Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name[1,2] | Pin Type[10] | Power Rail Name |
|---|---|---|---|
| Y11 | GVDD1 | Power | N/A |
| Y12 | VSS | Ground | N/A |
| Y13 | GVDD1 | Power | N/A |
| Y14 | VSS | Ground | N/A |
| Y15 | GVDD1 | Power | N/A |
| Y16 | VSS | Ground | N/A |
| Y17 | GVDD1 | Power | N/A |
| Y18 | VSS | Ground | N/A |
| Y19 | GVDD1 | Power | N/A |
| Y20 | VSS | Ground | N/A |
| Y21 | NVDD | Power | N/A |
| Y22 | GPIO20/$\overline{\text{SPI\_SL}}$[5,8] | I/O | NVDD |
| Y23 | GPIO17/SPI_SCK[5,8] | I/O | NVDD |
| Y24 | GPIO14/DRQ0/$\overline{\text{IRQ14}}$/RC14[5,8] | I/O | NVDD |
| Y25 | GPIO12/$\overline{\text{IRQ12}}$/RC12[5,8] | I/O | NVDD |
| Y26 | GPIO8/$\overline{\text{IRQ8}}$/RC8[5,8] | I/O | NVDD |
| Y27 | NVDD | Power | N/A |
| Y28 | VSS | Ground | N/A |
| AA1 | GVDD1 | Power | N/A |
| AA2 | VSS | Ground | N/A |
| AA3 | M1DQ18 | I/O | GVDD1 |
| AA4 | GVDD1 | Power | N/A |
| AA5 | VSS | Ground | N/A |
| AA6 | M1DQ20 | I/O | GVDD1 |
| AA7 | GVDD1 | Power | N/A |
| AA8 | VSS | Ground | N/A |
| AA9 | M1A15 | O | GVDD1 |
| AA10 | M1CK2 | O | GVDD1 |
| AA11 | M1MDIC0 | I/O | GVDD1 |
| AA12 | M1VREF | I | GVDD1 |
| AA13 | M1MDIC1 | I/O | GVDD1 |
| AA14 | M1DQ46 | I/O | GVDD1 |
| AA15 | M1DQ47 | I/O | GVDD1 |
| AA16 | M1DQ45 | I/O | GVDD1 |
| AA17 | M1DQ41 | I/O | GVDD1 |
| AA18 | M1DQ62 | I/O | GVDD1 |
| AA19 | M1DQ63 | I/O | GVDD1 |
| AA20 | M1DQ61 | I/O | GVDD1 |
| AA21 | VSS | Ground | N/A |
| AA22 | GPIO21[5,8] | I/O | NVDD |
| AA23 | GPIO18/SPI_MOSI[5,8] | I/O | NVDD |
| AA24 | GPIO16/RC16[5,8] | I/O | NVDD |
| AA25 | GPIO4/DDN1/$\overline{\text{IRQ4}}$/RC4[5,8] | I/O | NVDD |
| AA26 | GPIO9/$\overline{\text{IRQ9}}$/RC9[5,8] | I/O | NVDD |
| AA27 | GPIO6/$\overline{\text{IRQ6}}$/RC6[5,8] | I/O | NVDD |
| AA28 | GPIO1/$\overline{\text{IRQ1}}$/RC1[5,8] | I/O | NVDD |

## Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name[1,2] | Pin Type[10] | Power Rail Name |
|---|---|---|---|
| AE9 | M1A8 | O | GVDD1 |
| AE10 | GVDD1 | Power | N/A |
| AE11 | VSS | Ground | N/A |
| AE12 | M1A0 | O | GVDD1 |
| AE13 | GVDD1 | Power | N/A |
| AE14 | VSS | Ground | N/A |
| AE15 | M1DQ39 | I/O | GVDD1 |
| AE16 | GVDD1 | Power | N/A |
| AE17 | VSS | Ground | N/A |
| AE18 | M1DQ54 | I/O | GVDD1 |
| AE19 | GVDD1 | Power | N/A |
| AE20 | VSS | Ground | N/A |
| AE21 | GPIO29/UART_TXD[5,8] | I/O | NVDD |
| AE22 | TDM1TCK/GE2_RX_CLK[3] | I | NVDD |
| AE23 | TDM1RSN/GE2_RX_CTL[3] | I/O | NVDD |
| AE24 | VSS | Ground | N/A |
| AE25 | TDM3RCK/GE1_GTX_CLK[3] | I/O | NVDD |
| AE26 | TDM3TSN/GE1_RX_CLK[3] | I/O | NVDD |
| AE27 | TDM2RSN/GE1_TD2[3] | I/O | NVDD |
| AE28 | TDM2RDT/GE1_TD1[3] | I/O | NVDD |
| AF1 | M1DQ28 | I/O | GVDD1 |
| AF2 | M1DM3 | O | GVDD1 |
| AF3 | M1DQ26 | I/O | GVDD1 |
| AF4 | M1ECC4 | I/O | GVDD1 |
| AF5 | M1DM8 | O | GVDD1 |
| AF6 | M1ECC2 | I/O | GVDD1 |
| AF7 | M1CKE1 | O | GVDD1 |
| AF8 | M1CK0 | O | GVDD1 |
| AF9 | $\overline{\text{M1CK0}}$ | O | GVDD1 |
| AF10 | M1BA1 | O | GVDD1 |
| AF11 | M1A1 | O | GVDD1 |
| AF12 | $\overline{\text{M1WE}}$ | O | GVDD1 |
| AF13 | M1DQ37 | I/O | GVDD1 |
| AF14 | M1DM4 | O | GVDD1 |
| AF15 | M1DQ36 | I/O | GVDD1 |
| AF16 | M1DQ32 | I/O | GVDD1 |
| AF17 | M1DQ55 | I/O | GVDD1 |
| AF18 | M1DM6 | O | GVDD1 |
| AF19 | M1DQ53 | I/O | GVDD1 |
| AF20 | M1DQ52 | I/O | GVDD1 |
| AF21 | GPIO28/UART_RXD[5,8] | I/O | NVDD |
| AF22 | TDM0RSN/GE2_TD2[3] | I/O | NVDD |
| AF23 | TDM0TDT/GE2_TD3[3] | I/O | NVDD |
| AF24 | NVDD | Power | N/A |
| AF25 | TDM2TSN/GE1_TX_CTL[3] | I/O | NVDD |
| AF26 | GE1_RX_CTL | I | NVDD |

## Table 1. Signal List by Ball Number (continued)

| Ball Number | Signal Name[1,2] | Pin Type[10] | Power Rail Name |
|---|---|---|---|
| AH17 | $\overline{\text{M1DQS6}}$ | I/O | GVDD1 |
| AH18 | M1DQS6 | I/O | GVDD1 |
| AH19 | M1DQ48 | I/O | GVDD1 |
| AH20 | M1DQ49 | I/O | GVDD1 |
| AH21 | VSS | Ground | N/A |
| AH22 | TDM0RCK/GE2_RD2[3] | I/O | NVDD |
| AH23 | TDM0RDT/GE2_RD3[3] | I/O | NVDD |
| AH24 | TDM0TSN/GE2_RD0[3] | I/O | NVDD |
| AH25 | TDM1RCK/GE2_RD1[3] | I/O | NVDD |
| AH26 | TDM3TDT/GE1_RD3[3] | I/O | NVDD |
| AH27 | TDM3TCK/GE1_RD2[3] | I | NVDD |
| AH28 | VSS | Ground | N/A |

**Notes:**
1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD).
2. Signal function during power-on reset is determined by the RCW source type.
3. Selection of TDM versus RGMII functionality is determined by the RCW bit values.
4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values.
5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the *GPIO* chapter in the *MSC8252 Reference Manual*.
6. Open-drain signal.
7. Internal 20 KΩ pull-up resistor.
8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See the *GPIO* chapter of the *MSC8252 Reference Manual* for configuration details.
9. Connect to power supply via external filter. See **Section 3.2**, *PLL Power Supply Design Considerations* for details.
10. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected.

# 2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8252 Reference Manual*.

## 2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8252.

**Table 2. Absolute Maximum Ratings**

| Rating | Power Rail Name | Symbol | Value | Unit |
|---|---|---|---|---|
| Core supply voltage<br>• Cores 0–3 | VDD | $V_{DD}$ | –0.3 to 1.1 | V |
| PLL supply voltage[3] | | $V_{DDPLL0}$<br>$V_{DDPLL1}$<br>$V_{DDPLL2}$ | –0.3 to 1.1<br>–0.3 to 1.1<br>–0.3 to 1.1 | V<br>V<br>V |
| M3 memory supply voltage | M3VDD | $V_{DDM3}$ | –0.3 to 1.1 | V |
| DDR memory supply voltage<br>• DDR2 mode<br>• DDR3 mode | GVDD1, GVDD2 | $V_{DDDDR}$ | <br>–0.3 to 1.98<br>–0.3 to 1.65 | <br>V<br>V |
| DDR reference voltage | MVREF | $MV_{REF}$ | –0.3 to 0.51 × $V_{DDDDR}$ | V |
| Input DDR voltage | | $V_{INDDR}$ | –0.3 to $V_{DDDDR}$ + 0.3 | V |
| I/O voltage excluding DDR and RapidIO lines | NVDD, QVDD | $V_{DDIO}$ | –0.3 to 2.625 | V |
| Input I/O voltage | | $V_{INIO}$ | –0.3 to $V_{DDIO}$ + 0.3 | V |
| RapidIO pad voltage | SXPVDD1, SXPVDD2 | $V_{DDSXP}$ | –0.3 to 1.26 | V |
| Rapid I/O core voltage | SXCVDD1, SXCVDD2 | $V_{DDSXC}$ | –0.3 to 1.21 | V |
| Rapid I/O PLL voltage[3] | | $V_{DDRIOPLL}$ | –0.3 to 1.21 | V |
| Input RapidIO I/O voltage | | $V_{INRIO}$ | –0.3 to $V_{DDSXC}$ + 0.3 | V |
| Operating temperature | | $T_J$ | –40 to 105 | °C |
| Storage temperature range | | $T_{STG}$ | –55 to +150 | °C |

**Notes:**
1. Functional operating conditions are given in Table 3.
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8252 (see Figure 37 and Figure 38)

## 2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

**Table 3. Recommended Operating Conditions**

| Rating | Symbol | Min | Nominal | Max | Unit |
|---|---|---|---|---|---|
| Core supply voltage | $V_{DD}$ | 0.97 | 1.0 | 1.05 | V |
| M3 memory supply voltage | $V_{DDM3}$ | 0.97 | 1.0 | 1.05 | V |
| DDR memory supply voltage<br>• DDR2 mode<br>• DDR3 mode<br>DDR reference voltage | $V_{DDDDR}$<br><br><br>$MV_{REF}$ | <br>1.7<br>1.425<br>$0.49 \times V_{DDDDR}$ | <br>1.8<br>1.5<br>$0.5 \times V_{DDDDR}$ | <br>1.9<br>1.575<br>$0.51 \times V_{DDDDR}$ | <br>V<br>V<br>V |
| I/O voltage excluding DDR and RapidIO lines | $V_{DDIO}$ | 2.375 | 2.5 | 2.625 | V |
| Rapid I/O pad voltage | $V_{DDSXP}$ | 0.97 | 1.0 | 1.05 | V |
| Rapid I/O core voltage | $V_{DDSXC}$ | 0.97 | 1.0 | 1.05 | V |
| Operating temperature range:<br>• Standard<br>• Higher<br>• Extended | <br>$T_J$<br>$T_J$<br>$T_A$<br>$T_J$ | <br>0<br>0<br>–40<br>— | | <br>90<br>105<br>—<br>105 | <br>°C<br>°C<br>°C |
| Typical power: 1 GHz at 1.0 V[1] | P | — | 3.54 | — | W |

**Notes:** **1.** The typical power values are derived for a device running under the following conditions.
- Two cores running at 1 GHz, Core voltage at 1V, 75% utilization (50% control/50% DSP).
- A single 64 bit DDR3 running at 800 MHz, 50% utilization (50% reads/50% writes).
- M3 Memory 50% utilized, PCI Express controller disabled, TDM enabled 20% loading, Serial RapidIO controller disabled, 1 RGMII at 1 Gbps 50% loading.
- A junction temperature of 60°C.

## 2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8252 for the FC-PBGA packages.

**Table 4. Thermal Characteristics for the MSC8252**

| Characteristic | Symbol | FC-PBGA 29 × 29 mm² | | Unit |
|---|---|---|---|---|
| | | Natural Convection | 200 ft/min (1 m/s) airflow | |
| Junction-to-ambient[1, 2] | $R_{\theta JA}$ | 18 | 12 | °C/W |
| Junction-to-ambient, four-layer board[1, 2] | $R_{\theta JA}$ | 13 | 9 | °C/W |
| Junction-to-board (bottom)[3] | $R_{\theta JB}$ | 5 | | °C/W |
| Junction-to-case[4] | $R_{\theta JC}$ | 0.6 | | °C/W |

**Notes:**
**1.** Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
**2.** Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESDC51-6. Thermal test board meets JEDEC specification for the specified package.
**3.** Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package.
**4.** Junction-to-case at the top of the package determined using MIL- STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer

### 2.5.1.2 DDR3 (1.5V) SDRAM DC Electrical Characteristics

Table 7 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR3 SDRAM.

**Note:** At recommended operating conditions (see Table 3) with $V_{DDDDR}$ = 1.5 V.

**Table 7. DDR3 SDRAM Interface DC Electrical Characteristics**

| Parameter/Condition | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| I/O reference voltage | $MV_{REF}$ | 0.49 × $V_{DDDDR}$ | 0.51 × $V_{DDDDR}$ | V | 2,3,4 |
| Input high voltage | $V_{IH}$ | $MV_{REF}$ + 0.100 | $V_{DDDDR}$ | V | 5 |
| Input low voltage | $V_{IL}$ | GND | $MV_{REF}$ – 0.100 | V | 5 |
| I/O leakage current | $I_{OZ}$ | –50 | 50 | μA | 6 |

**Notes:**
1. $V_{DDDDR}$ is expected to be within 50 mV of the DRAM $V_{DD}$ at all times. The DRAM and memory controller can use the same or different sources.
2. $MV_{REF}$ is expected to be equal to 0.5 × $V_{DDDDR}$ and to track $V_{DDDDR}$ DC variations as measured at the receiver. Peak-to-peak noise on $MV_{REF}$ may not exceed ±1% of the DC value.
3. $V_{TT}$ is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to $MV_{REF}$ with a minimum value of $MV_{REF}$ – 0.4 and a maximum value of $MV_{REF}$ + 0.04 V. $V_{TT}$ should track variations in the DC-level of $MV_{REF}$.
4. The voltage regulator for $MV_{REF}$ must be able to supply up to 250 μA.
5. Input capacitance load for DQ, DQS, and $\overline{DQS}$ signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, 0 V ≤ $V_{OUT}$ ≤ $V_{DDDDR}$.

### 2.5.1.3 DDR2/DDR3 SDRAM Capacitance

Table 8 provides the DDR controller interface capacitance for DDR2 and DDR3 memory.

**Note:** At recommended operating conditions (see Table 3) with $V_{DDDDR}$ = 1.8 V for DDR2 memory or $V_{DDDDR}$ = 1.5 V for DDR3 memory.

**Table 8. DDR2/DDR3 SDRAM Capacitance**

| Parameter | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| I/O capacitance: DQ, DQS, $\overline{DQS}$ | $C_{IO}$ | 6 | 8 | pF |
| Delta I/O capacitance: DQ, DQS, $\overline{DQS}$ | $C_{DIO}$ | — | 0.5 | pF |

**Note:** Guaranteed by FAB process and micro-construction.

### 2.5.1.4 DDR Reference Current Draw

Table 9 lists the current draw characteristics for $MV_{REF}$.

**Note:** Values when used at recommended operating conditions (see Table 3).

**Table 9. Current Draw Characteristics for $MV_{REF}$**

| Parameter / Condition | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Current draw for $MV_{REFn}$<br>• DDR2 SDRAM<br>• DDR3 SDRAM | $I_{MVREFn}$ | — | <br>300<br>250 | <br>µA<br>µA |

## 2.5.2 High-Speed Serial Interface (HSSI) DC Electrical Characteristics

The MSC8252 features an HSSI that includes two 4-channel SerDes ports used for high-speed serial interface applications (PCI Express, Serial RapidIO interfaces, and SGMII). This section and its subsections describe the common portion of the SerDes DC, including the DC requirements for the SerDes reference clocks and the SerDes data lane transmitter (Tx) and receiver (Rx) reference circuits. The data lane circuit specifications are specific for each supported interface, and they have individual subsections by protocol. The selection of individual data channel functionality is done via the Reset Configuration Word High Register (RCWHR) SerDes Protocol selection fields (S1P and S2P). Specific AC electrical characteristics are defined in Section 2.6.2, "HSSI AC Timing Specifications."

### 2.5.2.1 Signal Term Definitions

The SerDes interface uses differential signalling to transfer data across the serial link. This section defines terms used in the description and specification of differential signals. Figure 4 shows how the signals are defined. For illustration purposes only, one SerDes lane is used in the description. Figure 4 shows the waveform for either a transmitter output (SR[1–2]_TX and $\overline{\text{SR[1–2]\_TX}}$) or a receiver input (SR[1–2]_RX and $\overline{\text{SR[1–2]\_RX}}$). Each signal swings between A volts and B volts where A > B.

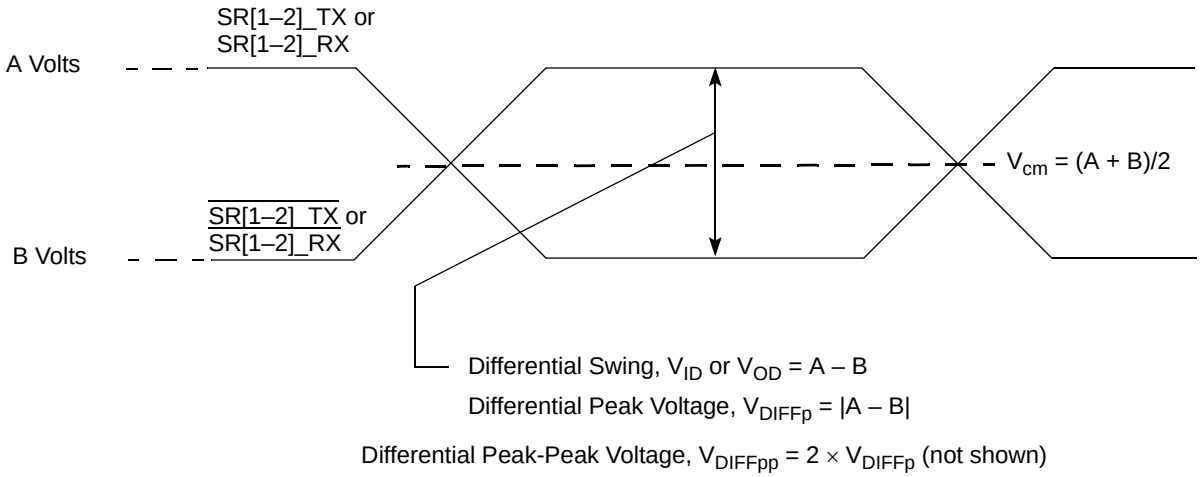


**Figure 4. Differential Voltage Definitions for Transmitter or Receiver**

### 2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SR1_REF_CLK/$\overline{\text{SR1\_REF\_CLK}}$ or SR2_REF_CLK/$\overline{\text{SR2\_REF\_CLK}}$. Figure 5 shows a receiver reference diagram of the SerDes reference clocks.

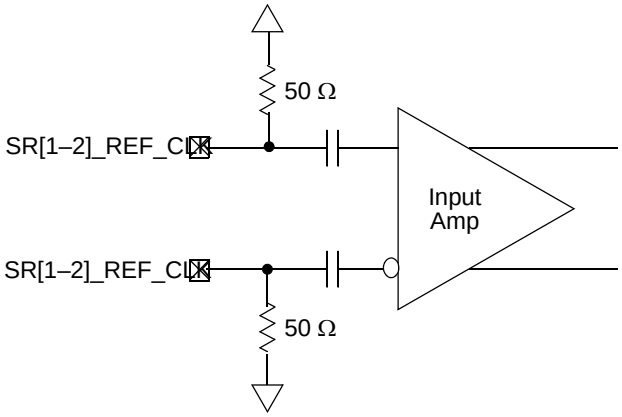


**Figure 5. Receiver of SerDes Reference Clocks**

The characteristics of the clock signals are as follows:

- The supply voltage requirements for $V_{DDSXC}$ are as specified in **Table 3.**
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 5. Each differential clock input (SR[1–2]_REF_CLK or $\overline{\text{SR[1–2]\_REF\_CLK}}$) has on-chip 50-Ω termination to $GND_{SXC}$ followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA) while the minimum common mode input level is 0.1 V above $GND_{SXC}$. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ inputs cannot drive 50 Ω to $GND_{SXC}$ DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

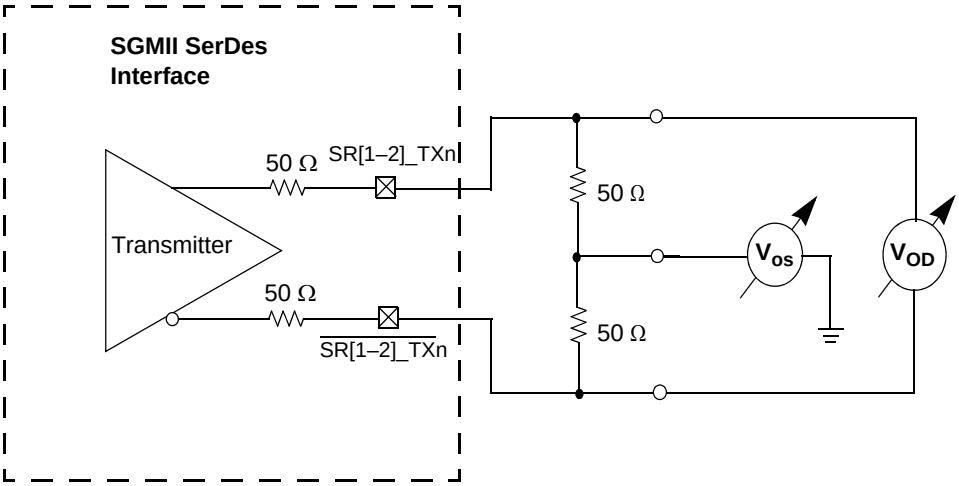


**Figure 10. SGMII Transmitter DC Measurement Circuit**

Table 16 describes the SGMII SerDes receiver AC-coupled DC electrical characteristics.

**Table 16. SGMII DC Receiver Electrical Characteristics[5]**

| Parameter | | Symbol | Min | Typ | Max | Unit | Notes |
|---|---|---|---|---|---|---|---|
| DC Input voltage range | | — | | N/A | | — | 1 |
| Input differential voltage | SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1<br>SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2 | $V_{RX\_DIFFp\text{-}p}$ | 100 | — | 1200 | mV | 2, 4 |
| | SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1<br>SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2 | | 175 | — | | | |
| Loss of signal threshold | SRDSnCR4[EICE{12:10}] = 0b001 for SGMII1<br>SRDSnCR4[EICF{4:2}] = 0b001 for SGMII2 | VLOS | 30 | — | 100 | mV | 3, 4 |
| | SRDSnCR4[EICE{12:10}] = 0b100 for SGMII1<br>SRDSnCR4[EICF{4:2}] = 0b100 for SGMII2 | | 65 | — | 175 | | |
| Receiver differential input impedance | | $Z_{RX\_DIFF}$ | 80 | — | 120 | W | — |

**Notes:**
1. Input must be externally AC-coupled.
2. $V_{RX\_DIFFp\text{-}p}$ is also referred to as peak-to-peak input differential voltage.
3. The concept of this parameter is equivalent to the Electrical Idle Detect Threshold parameter in the PCI Express interface. Refer to the PCI Express Differential Receiver (RX) Input Specifications section of the *PCI Express Specification* document. for details.
4. The values for SGMII1 and SGMII2 are selected in the SRDS control registers.
5. The supply voltage is 1.0 V.

## 2.5.4 RGMII and Other Interface DC Electrical Characteristics

Table 17 describes the DC electrical characteristics for the following interfaces:

- RGMII Ethernet
- SPI
- TDM
- GPIO
- UART
- TIMER
- EE
- $I^2C$
- Interrupts ($\overline{\text{IRQn}}$, $\overline{\text{NMI\_OUT}}$, $\overline{\text{INT\_OUT}}$)
- Clock and resets (CLKIN, $\overline{\text{PORESET}}$, $\overline{\text{HRESET}}$, $\overline{\text{SRESET}}$)
- DMA External Request
- JTAG signals

**Table 17. 2.5 V I/O DC Electrical Characteristics**

| Characteristic | Symbol | Min | Max | Unit | Notes |
|---|---|---|---|---|---|
| Input high voltage | $V_{IH}$ | 1.7 | — | V | 1 |
| Input low voltage | $V_{IL}$ | — | 0.7 | V | 1 |
| Input high current ($V_{IN} = V_{DDIO}$) | $I_{IN}$ | — | 30 | μA | 2 |
| Output high voltage ($V_{DDIO}$ = min, $I_{OH}$ = –1.0 mA) | $V_{OH}$ | 2.0 | VDDIO + 0.3 | V | 1 |
| Output low voltage ($V_{DDIO}$ = min, $I_{OL}$= 1.0 mA) | $V_{OL}$ | GND – 0.3 | 0.40 | V | 1 |

**Notes:** **1.** The min $V_{IL}$ and max $V_{IH}$ values are based on the respective min and max $V_{IN}$ values listed in Table 3.
**2.** The symbol $V_{IN}$ represents the input voltage of the supply. It is referenced in Table 3.

**Table 21. DDR SDRAM Output AC Timing Specifications (continued)**

| Parameter | Symbol [1] | Min | Max | Unit | Notes |
|---|---|---|---|---|---|

**Notes:**

1. The symbols used for timing specifications follow the pattern of $t_{\text{(first two letters of functional block)(signal)(state) (reference)(state)}}$ for inputs and $t_{\text{(first two letters of functional block)(reference)(state)(signal)(state)}}$ for outputs. Output hold time can be read as DDR timing (DD) from the rising or falling edge of the reference clock (KH or KL) until the output went invalid (AX or DX). For example, $t_{DDKHAS}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes from the high (H) state until outputs (A) are setup (S) or output valid time. Also, $t_{DDKLDX}$ symbolizes DDR timing (DD) for the time $t_{MCK}$ memory clock reference (K) goes low (L) until data outputs (D) are invalid (X) or data output hold time.
2. All MCK/$\overline{\text{MCK}}$ referenced measurements are made from the crossing of the two signals.
3. ADDR/CMD includes all DDR SDRAM output signals except MCK/$\overline{\text{MCK}}$, $\overline{\text{MCS}}$, and MDQ/MECC/MDM/MDQS.
4. Note that $t_{DDKHMH}$ follows the symbol conventions described in note 1. For example, $t_{DDKHMH}$ describes the DDR timing (DD) from the rising edge of the MCK(n) clock (KH) until the MDQS signal is valid (MH). $t_{DDKHMH}$ can be modified through control of the DQSS override bits in the TIMING_CFG_2 register. This will typically be set to the same delay as the clock adjust in the CLK_CNTL register. The timing parameters listed in the table assume that these two parameters have been set to the same adjustment value. See the *MSC8252 Reference Manual* for a description and understanding of the timing modifications enabled by use of these bits.
5. Determined by maximum possible skew between a data strobe (MDQS) and any corresponding bit of data (MDQ), ECC (MECC), or data mask (MDM). The data strobe should be centered inside of the data eye at the pins of the MSC8252.
6. At recommended operating conditions with $V_{DDDDR}$ (1.5 V or 1,8 V) ± 5%.

**Note:** For the ADDR/CMD setup and hold specifications in Table 21, it is assumed that the clock control register is set to adjust the memory clocks by ½ applied cycle.

Figure 12 shows the DDR SDRAM output timing for the MCK to MDQS skew measurement ($t_{DDKHMH}$).

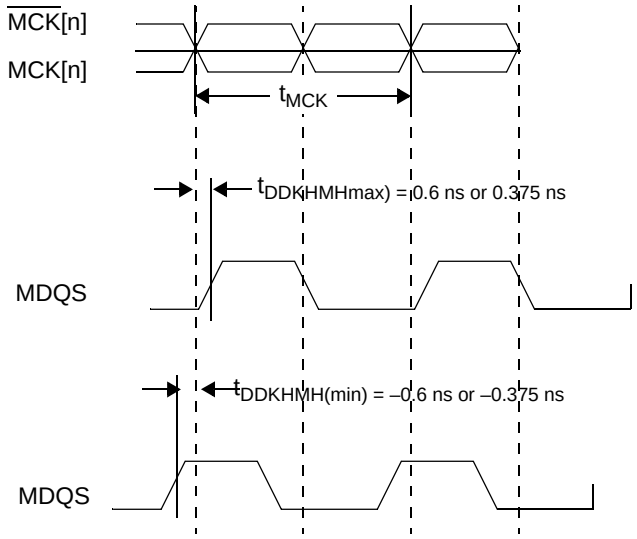


**Figure 12. MCK to MDQS Timing**

### 2.6.5.2 RGMII AC Timing Specifications

Table 34 presents the RGMII AC timing specifications for applications requiring an on-board delayed clock.

**Table 34. RGMII at 1 Gbps[2] with On-Board Delay[3] AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter)[4] | $t_{SKEWT}$ | –-0.5 | — | 0.5 | ns |
| Data to clock input skew (at receiver) [4] | $t_{SKEWR}$ | 1 | — | 2.6 | ns |

**Notes:**
1. At recommended operating conditions with $V_{DDIO}$ of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. Program GCR4 as 0x00000000.
4. This implies that PC board design requires clocks to be routed such that an additional trace delay of greater than 1.5 ns and less than 2.0 ns is added to the associated clock signal.

Table 35 presents the RGMII AC timing specification for applications required non-delayed clock on board.

**Table 35. RGMII at 1 Gbps[2] with No On-Board Delay[3] AC Timing Specifications**

| Parameter/Condition | Symbol | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| Data to clock output skew (at transmitter)[4] | $t_{SKEWT}$ | –2.6 | — | –1.0 | ns |
| Data to clock input skew (at receiver)[4] | $t_{SKEWR}$ | –0.5 | — | 0.5 | ns |

**Notes:**
1. At recommended operating conditions with $V_{DDIO}$ of 2.5 V ± 5%.
2. RGMII at 100 Mbps support is guaranteed by design.
3. GCR4 should be programmed as 0x000CC330.
4. This implies that PC board design requires clocks to be routed with no additional trace delay

Figure 25 shows the RGMII AC timing and multiplexing diagrams.

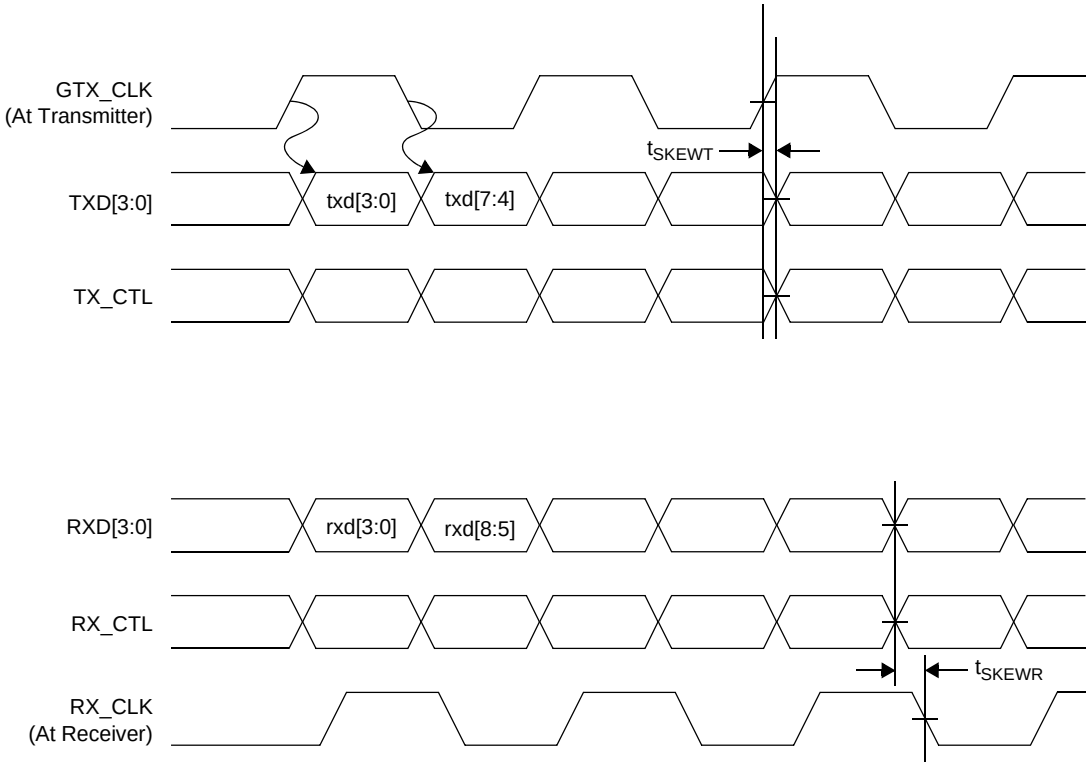


**Figure 25. RGMII AC Timing and Multiplexing**

Figure 30 shows the boundary scan (JTAG) timing diagram.

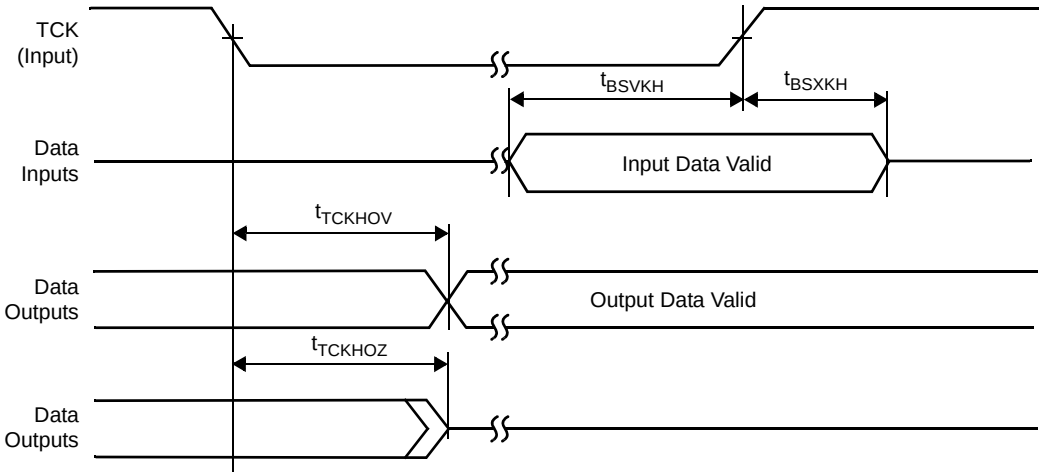


**Figure 30. Boundary Scan (JTAG) Timing**

Figure 31 shows the test access port timing diagram.

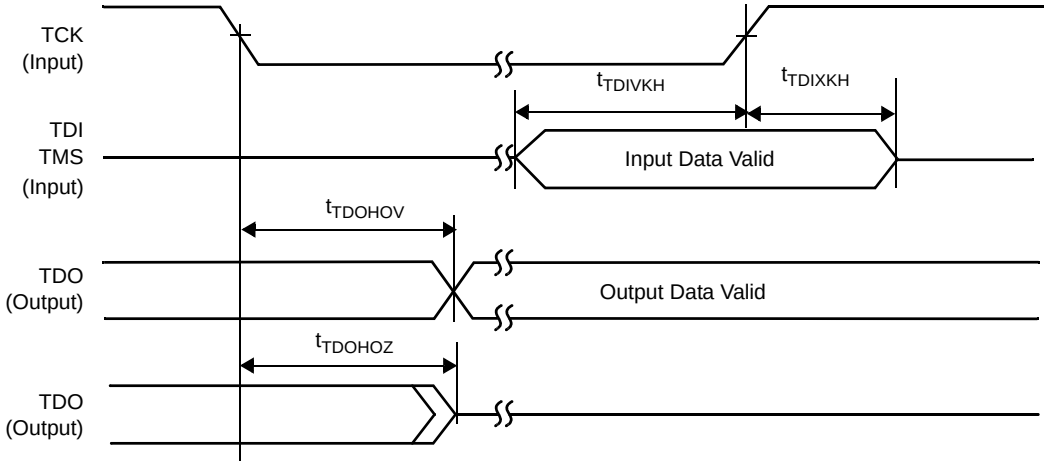


**Figure 31. Test Access Port Timing**

Figure 32 shows the $\overline{\text{TRST}}$ timing diagram.


**Figure 32. $\overline{\text{TRST}}$ Timing**

2. After the above rails rise to 90% of their nominal voltage, the following I/O power rails may rise in any sequence (see Figure 34): QVDD, NVDD, GVDD1, and GVDD2.

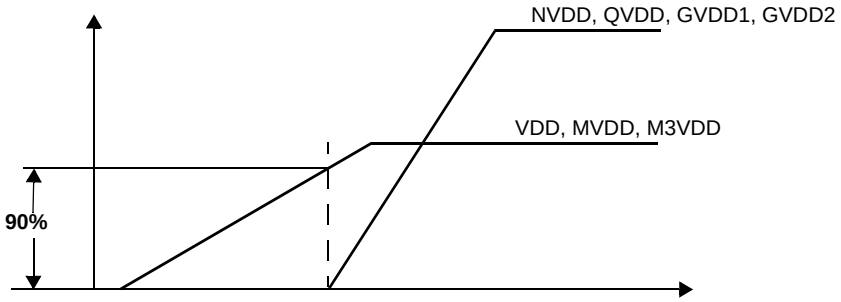


**Figure 34. Supply Ramp-Up Sequence**

**Notes:**
1. If the M3 memory is not used, M3VDD can be tied to GND.
2. If the HSSI port1 is not used, SXCVDD1and SXPVDD1 must be connected to the designated power supplies.
3. If the HSSI port2 is not used, SXCVDD2 and SXPVDD2 must be connected to the designated power supplies.
4. If the DDR port 1 interface is not used, it is recommended that GVDD1 be left unconnected.
5. If the DDR port 2 interface is not used, it is recommended that GVDD2 be left unconnected.

## 3.1.4 Reset Guidelines

When a debugger is not used, implement the connection scheme shown in Figure 35.

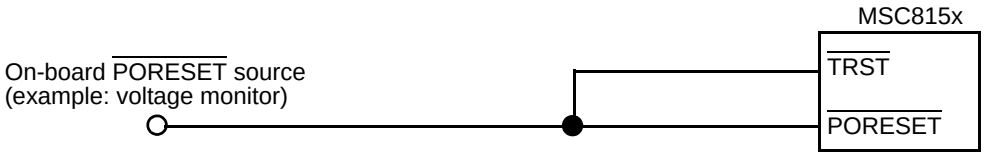


**Figure 35. Reset Connection in Functional Application**

When a debugger is used, implement the connection scheme shown in Figure 36.

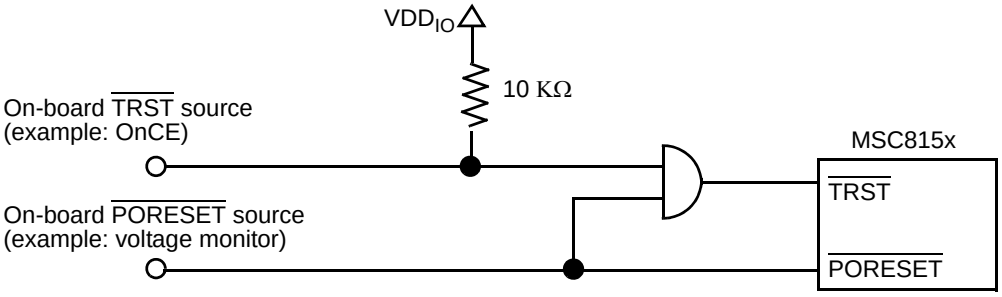


**Figure 36. Reset Connection in Debugger Application**

#### 3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

**Table 43. Connectivity of MAPAR Pins for DDR2**

| Signal Name | Pin connection |
|---|---|
| MAPAR_OUT | NC |
| $\overline{\text{MAPAR\_IN}}$ | NC |

**Notes:** 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8252 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

### 3.5.2 HSSI-Related Pins

#### 3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

**Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used**

| Signal Name | Pin Connection |
|---|---|
| SR_IMP_CAL_RX | NC |
| SR_IMP_CAL_TX | NC |
| $\overline{\text{SR[1–2]\_REF\_CLK}}$ | SXCVSS |
| SR[1–2]_REF_CLK | SXCVSS |
| SR[1–2]_RXD[3–0] | SXCVSS |
| $\overline{\text{SR[1–2]\_RXD[3–0]}}$ | SXCVSS |
| $\overline{\text{SR[1–2]\_TXD[3–0]}}$ | NC |
| SR[1–2]_TXD[3–0] | NC |
| SR[1–2]_PLL_AVDD | In use |
| SR[1–2]_PLL_AGND | In use |
| SXPVSS | In use |
| SXCVSS | In use |
| SXPVDD | In use |
| SXCVDD | In use |

**Note:** All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8252 Reference Manual* for details.

#### 3.5.2.2 HSSI Specific Lane Is Not Used

**Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used**

| Signal Name | Pin Connection |
|---|---|
| SR_IMP_CAL_RX | In use |
| SR_IMP_CAL_TX | In use |
| $\overline{\text{SR[1–2]\_REF\_CLK}}$ | In use |
| SR[1–2]_REF_CLK | In use |

**Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used (continued)**

| Signal Name | Pin Connection |
|---|---|
| SR[1–2]_RXD***n*** | SXCVSS |
| $\overline{\text{SR[1–2]\_RXD}\textit{n}}$ | SXCVSS |
| $\overline{\text{SR[1–2]\_TXD}\textit{n}}$ | NC |
| SR[1–2]_TXD***n*** | NC |
| SR[1–2]_PLL_AVDD | in use |
| SR[1–2]_PLL_AGND | in use |
| SXPVSS | in use |
| SXCVSS | in use |
| SXPVDD | in use |
| SXCVDD | in use |
| **Note:** The ***n*** indicates the lane number {0,1,2,3} for all unused lanes. | |

## 3.5.3 RGMII Ethernet Related Pins

**Note:** Table 46 and Table 47 assume that the alternate function of the specified pin is not used. If the alternate function is used, connect the pin as required to support that function.

**Table 46. Connectivity of RGMII Related Pins When the RGMII Interface Is Not Used**

| Signal Name | Pin Connection |
|---|---|
| GE1_RX_CTL | GND |
| GE2_TX_CTL | NC |
| **Note:** Assuming GE1 and GE2 are disabled in the reset configuration word. | |

GE_MDC and GE_MDIO pins should be connected as required by the specified protocol. If neither GE1 nor GE2 is used, Table 47 lists the recommended management pin connections.

**Table 47. Connectivity of GE Management Pins When GE1 and GE2 Are Not Used**

| Signal Name | Pin Connection |
|---|---|
| GE_MDC | NC |
| GE_MDIO | NC |

## 3.5.4 TDM Interface Related Pins

Table 48 lists the board connections of the TDM pins when an entire specific TDM is not used. For multiplexing options that select a subset of a TDM interface, use the connections described in Table 48 for those signals that are not selected. Table 48 assumes that the alternate function of the specified pin is not used. If the alternate function is used, connect that pin as required to support the selected function.

**Table 48. Connectivity of TDM Related Pins When TDM Interface Is Not Used**

| Signal Name | Pin Connection |
|---|---|
| TDM***n***RCLK | GND |
| TDM***n***RDAT | GND |
| TDM***n***RSYN | GND |