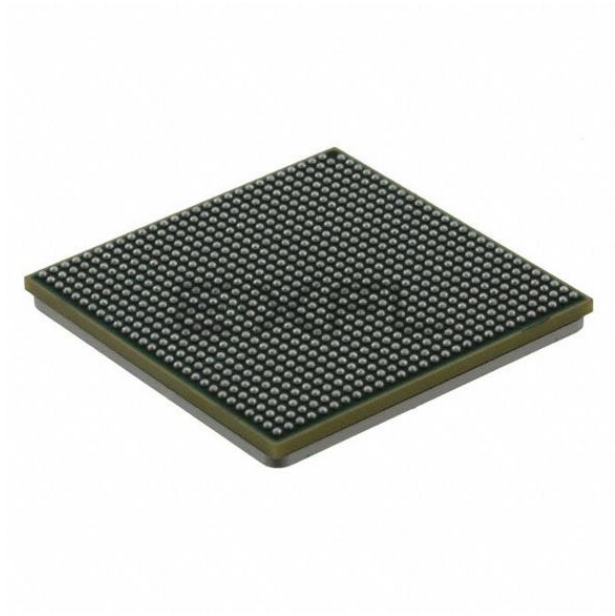

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Dual Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8252tag1000b

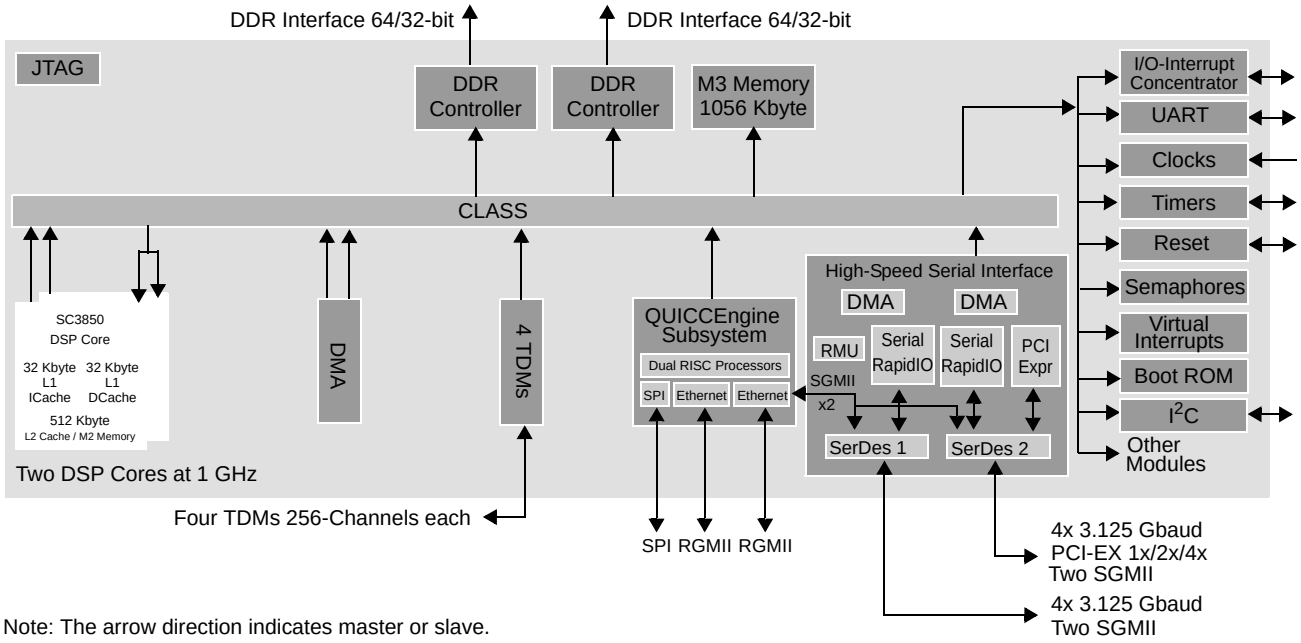


Figure 1. MSC8252 Block Diagram

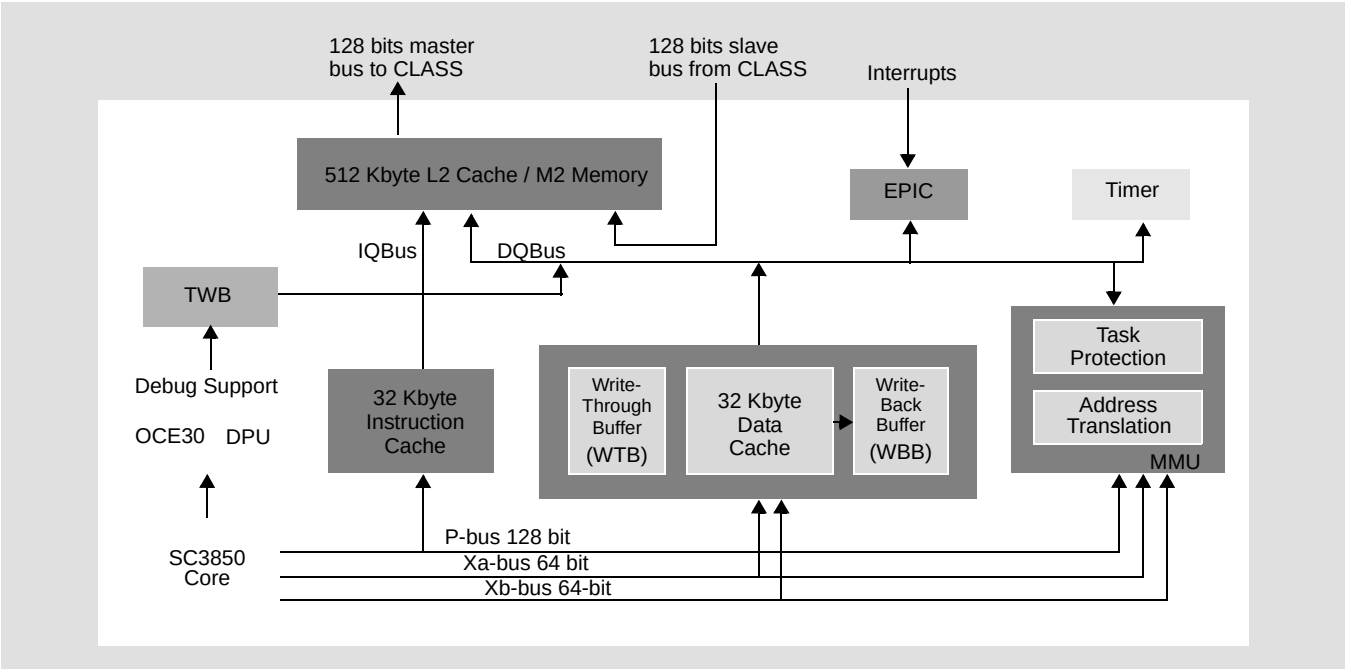


Figure 2. StarCore SC3850 DSP Subsystem Block Diagram

1.2 Signal List By Ball Location

Table 1 presents the signal list sorted by ball number. When designing a board, make sure that the power rail for each signal is appropriately considered. The specified power rail must be tied to the voltage level specified in this document if any of the related signal functions are used (active)

Note: The information in Table 1 and Table 2 distinguishes among three concepts. First, the power pins are the balls of the device package used to supply specific power levels for different device subsystems (as opposed to signals). Second, the power rails are the electrical lines on the board that transfer power from the voltage regulators to the device. They are indicated here as the reference power rails for signal lines; therefore, the actual power inputs are listed as N/A with regard to the power rails. Third, symbols used in these tables are the names for the voltage levels (absolute, recommended, and so on) and not the power supplies themselves.

Table 1. Signal List by Ball Number

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
A2	$\overline{\text{M2DQS3}}$	I/O	GVDD2
A3	M2DQS3	I/O	GVDD2
A4	M2ECC0	I/O	GVDD2
A5	$\overline{\text{M2DQS8}}$	I/O	GVDD2
A6	M2DQS8	I/O	GVDD2
A7	M2A5	O	GVDD2
A8	$\overline{\text{M2CK1}}$	O	GVDD2
A9	M2CK1	O	GVDD2
A10	$\overline{\text{M2CS0}}$	O	GVDD2
A11	M2BA0	O	GVDD2
A12	$\overline{\text{M2CAS}}$	O	GVDD2
A13	M2DQ34	I/O	GVDD2
A14	$\overline{\text{M2DQS4}}$	I/O	GVDD2
A15	M2DQS4	I/O	GVDD2
A16	M2DQ50	I/O	GVDD2
A17	$\overline{\text{M2DQS6}}$	I/O	GVDD2
A18	M2DQS6	I/O	GVDD2
A19	M2DQ48	I/O	GVDD2
A20	M2DQ49	I/O	GVDD2
A21	VSS	Ground	N/A
A22	Reserved	NC	—
A23	SXPVDD1	Power	N/A
A24	SXPVSS1	Ground	N/A
A25	Reserved	NC	—
A26	Reserved	NC	—
A27	SXCVDD1	Power	N/A
A28	SXCVSS1	Ground	N/A
B1	M2DQ24	I/O	GVDD2
B2	GVDD2	Power	N/A
B3	M2DQ25	I/O	GVDD2
B4	VSS	Ground	N/A
B5	GVDD2	Power	N/A
B6	M2ECC1	I/O	GVDD2
B7	VSS	Ground	N/A
B8	GVDD2	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
B9	M2A13	O	GVDD2
B10	VSS	Ground	N/A
B11	GVDD2	Power	N/A
B12	$\overline{\text{M2CS1}}$	O	GVDD2
B13	VSS	Ground	N/A
B14	GVDD2	Power	N/A
B15	M2DQ35	I/O	GVDD2
B16	VSS	Ground	N/A
B17	GVDD2	Power	N/A
B18	M2DQ51	I/O	GVDD2
B19	VSS	Ground	N/A
B20	GVDD2	Power	N/A
B21	Reserved	NC	—
B22	Reserved	NC	—
B23	SR1_TXD0	O	SXPVDD1
B24	$\overline{\text{SR1\_TXD0}}$	O	SXPVDD1
B25	SXCVDD1	Power	N/A
B26	SXCVSS1	Ground	N/A
B27	$\overline{\text{SR1\_RXD0}}$	I	SXCVDD1
B28	SR1_RXD0	I	SXCVDD1
C1	M2DQ28	I/O	GVDD2
C2	M2DM3	O	GVDD2
C3	M2DQ26	I/O	GVDD2
C4	M2ECC4	I/O	GVDD2
C5	M2DM8	O	GVDD2
C6	M2ECC2	I/O	GVDD2
C7	M2CKE1	O	GVDD2
C8	M2CK0	O	GVDD2
C9	$\overline{\text{M2CK0}}$	O	GVDD2
C10	M2BA1	O	GVDD2
C11	M2A1	O	GVDD2
C12	$\overline{\text{M2WE}}$	O	GVDD2
C13	M2DQ37	I/O	GVDD2
C14	M2DM4	O	GVDD2
C15	M2DQ36	I/O	GVDD2
C16	M2DQ32	I/O	GVDD2
C17	M2DQ55	I/O	GVDD2
C18	M2DM6	O	GVDD2
C19	M2DQ53	I/O	GVDD2
C20	M2DQ52	I/O	GVDD2
C21	Reserved	NC	—
C22	SR1_IMP_CAL_RX	I	SXCVDD1
C23	SXPVSS1	Ground	N/A
C24	SXPVDD1	Power	N/A
C25	SR1_REF_CLK	I	SXCVDD1
C26	$\overline{\text{SR1\_REF\_CLK}}$	I	SXCVDD1

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
E17	M2DQ56	I/O	GVDD2
E18	M2DQ57	I/O	GVDD2
E19	$\overline{\text{M2DQS7}}$	I/O	GVDD2
E20	Reserved	NC	—
E21	Reserved	NC	—
E22	Reserved	NC	—
E23	SXPVDD1	Power	N/A
E24	SXPVSS1	Ground	N/A
E25	SR1_PLL_AGND[9]	Ground	SXCVSS1
E26	SR1_PLL_AVDD[9]	Power	SXCVDD1
E27	SXCVSS1	Ground	N/A
E28	SXCVDD1	Power	N/A
F1	VSS	Ground	N/A
F2	GVDD2	Power	N/A
F3	M2DQ16	I/O	GVDD2
F4	VSS	Ground	N/A
F5	GVDD2	Power	N/A
F6	M2DQ17	I/O	GVDD2
F7	VSS	Ground	N/A
F8	GVDD2	Power	N/A
F9	M2BA2	O	GVDD2
F10	VSS	Ground	N/A
F11	GVDD2	Power	N/A
F12	M2A4	O	GVDD2
F13	VSS	Ground	N/A
F14	GVDD2	Power	N/A
F15	M2DQ42	I/O	GVDD2
F16	VSS	Ground	N/A
F17	GVDD2	Power	N/A
F18	M2DQ58	I/O	GVDD2
F19	M2DQS7	I/O	GVDD2
F20	GVDD2	Power	N/A
F21	SXPVDD1	Power	N/A
F22	SXPVSS1	Ground	N/A
F23	SR1_TXD2/SG1_TX[4]	O	SXPVDD1
F24	$\overline{\text{SR1\_TXD2}}$/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD1
F25	SXCVDD1	Power	N/A
F26	SXCVSS1	Ground	N/A
F27	$\overline{\text{SR1\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD1
F28	SR1_RXD2/SG1_RX[4]	I	SXCVDD1
G1	$\overline{\text{M2DQS2}}$	I/O	GVDD2
G2	M2DQS2	I/O	GVDD2
G3	M2DQ19	I/O	GVDD2
G4	M2DM2	O	GVDD2
G5	M2DQ21	I/O	GVDD2
G6	M2DQ22	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/PE_TXD2/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	VSS	Ground	N/A
P16	VSS	Ground	N/A
P17	VSS	Ground	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
V21	RCW_LSEL_3/RC20	I/O	NVDD
V22	RCW_LSEL_2/RC19	I/O	NVDD
V23	SXPVDD2	Power	N/A
V24	SXPVSS2	Ground	N/A
V25	RCW_LSEL_1/RC18	I/O	NVDD
V26	RC21	I	NVDD
V27	SXCVDD2	Power	N/A
V28	SXCVSS2	Ground	N/A
W1	VSS	Ground	N/A
W2	GVDD1	Power	N/A
W3	M1DM1	O	GVDD1
W4	VSS	Ground	N/A
W5	GVDD1	Power	N/A
W6	M1DQ0	I/O	GVDD1
W7	VSS	Ground	N/A
W8	GVDD1	Power	N/A
W9	M1DQ5	I/O	GVDD1
W10	VDD	Power	N/A
W11	VSS	Ground	N/A
W12	VDD	Power	N/A
W13	VSS	Ground	N/A
W14	VDD	Power	N/A
W15	VSS	Ground	N/A
W16	VDD	Power	N/A
W17	VSS	Ground	N/A
W18	VDD	Power	N/A
W19	VSS	Ground	N/A
W20	VSS	Ground	N/A
W21	RCW_LSEL0/RC17	I/O	NVDD
W22	GPIO19/SPI_MISO[5,8]	I/O	NVDD
W23	VSS	Ground	N/A
W24	NVDD	Power	N/A
W25	GPIO11/IRQ11/RC11[5,8]	I/O	NVDD
W26	GPIO3/DRQ1/IRQ3/RC3[5,8]	I/O	NVDD
W27	GPIO7/IRQ7/RC7[5,8]	I/O	NVDD
W28	GPIO2/IRQ2/RC2[5,8]	I/O	NVDD
Y1	M1DQS1	I/O	GVDD1
Y2	M1DQS1	I/O	GVDD1
Y3	M1DQ10	I/O	GVDD1
Y4	M1DQ11	I/O	GVDD1
Y5	M1DQ14	I/O	GVDD1
Y6	M1DQ23	I/O	GVDD1
Y7	M1ODT0	O	GVDD1
Y8	M1A12	O	GVDD1
Y9	M1A14	O	GVDD1
Y10	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AB1	$\overline{\text{M1DQS2}}$	I/O	GVDD1
AB2	M1DQS2	I/O	GVDD1
AB3	M1DQ19	I/O	GVDD1
AB4	M1DM2	O	GVDD1
AB5	M1DQ21	I/O	GVDD1
AB6	M1DQ22	I/O	GVDD1
AB7	M1CKE0	O	GVDD1
AB8	M1A11	O	GVDD1
AB9	M1A7	O	GVDD1
AB10	$\overline{\text{M1CK2}}$	O	GVDD1
AB11	M1APAR_OUT	O	GVDD1
AB12	M1ODT1	O	GVDD1
AB13	$\overline{\text{M1APAR\_IN}}$	I	GVDD1
AB14	M1DQ43	I/O	GVDD1
AB15	M1DM5	O	GVDD1
AB16	M1DQ44	I/O	GVDD1
AB17	M1DQ40	I/O	GVDD1
AB18	M1DQ59	I/O	GVDD1
AB19	M1DM7	O	GVDD1
AB20	M1DQ60	I/O	GVDD1
AB21	VSS	Ground	N/A
AB22	GPIO31/I2C_SDA[5,8]	I/O	NVDD
AB23	GPIO27/TMR4/RCW_SRC0[5,8]	I/O	NVDD
AB24	GPIO25/TMR2/RCW_SRC1[5,8]	I/O	NVDD
AB25	GPIO24/TMR1/RCW_SRC2[5,8]	I/O	NVDD
AB26	GPIO10/$\overline{\text{IRQ10}}$/RC10[5,8]	I/O	NVDD
AB27	GPIO5/$\overline{\text{IRQ5}}$/RC5[5,8]	I/O	NVDD
AB28	GPIO0/$\overline{\text{IRQ0}}$/RC0[5,8]	I/O	NVDD
AC1	VSS	Ground	N/A
AC2	GVDD1	Power	N/A
AC3	M1DQ16	I/O	GVDD1
AC4	VSS	Ground	N/A
AC5	GVDD1	Power	N/A
AC6	M1DQ17	I/O	GVDD1
AC7	VSS	Ground	N/A
AC8	GVDD1	Power	N/A
AC9	M1BA2	O	GVDD1
AC10	VSS	Ground	N/A
AC11	GVDD1	Power	N/A
AC12	M1A4	O	GVDD1
AC13	VSS	Ground	N/A
AC14	GVDD1	Power	N/A
AC15	M1DQ42	I/O	GVDD1
AC16	VSS	Ground	N/A
AC17	GVDD1	Power	N/A
AC18	M1DQ58	I/O	GVDD1

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8252 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8252.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–3	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	 –0.3 to 1.98 –0.3 to 1.65	 V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3**.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8252 (see Figure 37 and Figure 38)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}	0.97	1.0	1.05	V
M3 memory supply voltage	V_{DDM3}	0.97	1.0	1.05	V
DDR memory supply voltage • DDR2 mode • DDR3 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 1.7 1.425 $0.49 \times V_{DDDDR}$	 1.8 1.5 $0.5 \times V_{DDDDR}$	 1.9 1.575 $0.51 \times V_{DDDDR}$	 V V V
I/O voltage excluding DDR and RapidIO lines	V_{DDIO}	2.375	2.5	2.625	V
Rapid I/O pad voltage	V_{DDSXP}	0.97	1.0	1.05	V
Rapid I/O core voltage	V_{DDSXC}	0.97	1.0	1.05	V
Operating temperature range: • Standard • Higher • Extended	 T_J T_J T_A T_J	 0 0 –40 —	 	 90 105 — 105	 °C °C °C
Typical power: 1 GHz at 1.0 V[1]	P	—	3.54	—	W

Notes: **1.** The typical power values are derived for a device running under the following conditions.
- Two cores running at 1 GHz, Core voltage at 1V, 75% utilization (50% control/50% DSP).
- A single 64 bit DDR3 running at 800 MHz, 50% utilization (50% reads/50% writes).
- M3 Memory 50% utilized, PCI Express controller disabled, TDM enabled 20% loading, Serial RapidIO controller disabled, 1 RGMII at 1 Gbps 50% loading.
- A junction temperature of 60°C.

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8252 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8252

Characteristic	Symbol	FC-PBGA 29 × 29 mm²		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	18	12	°C/W
Junction-to-ambient, four-layer board[1, 2]	$R_{\theta JA}$	13	9	°C/W
Junction-to-board (bottom)[3]	$R_{\theta JB}$	5		°C/W
Junction-to-case[4]	$R_{\theta JC}$	0.6		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESDC51-6. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-case at the top of the package determined using MIL- STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer

2.5.2.2 SerDes Reference Clock Receiver Characteristics

The SerDes reference clock inputs are applied to an internal PLL whose output creates the clock used by the corresponding SerDes lanes. The SerDes reference clock inputs are SR1_REF_CLK/$\overline{\text{SR1\_REF\_CLK}}$ or SR2_REF_CLK/$\overline{\text{SR2\_REF\_CLK}}$. Figure 5 shows a receiver reference diagram of the SerDes reference clocks.

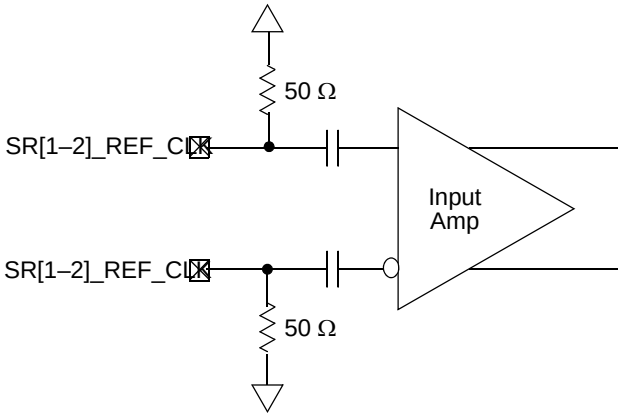


Figure 5. Receiver of SerDes Reference Clocks

The characteristics of the clock signals are as follows:

- The supply voltage requirements for V_{DDSXC} are as specified in **Table 3.**
- The SerDes reference clock receiver reference circuit structure is as follows:
  - The SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ are internally AC-coupled differential inputs as shown in Figure 5. Each differential clock input (SR[1–2]_REF_CLK or $\overline{\text{SR[1–2]\_REF\_CLK}}$) has on-chip 50-Ω termination to GND_{SXC} followed by on-chip AC-coupling.
  - The external reference clock driver must be able to drive this termination.
  - The SerDes reference clock input can be either differential or single-ended. Refer to the differential mode and single-ended mode descriptions below for detailed requirements.
- The maximum average current requirement also determines the common mode voltage range.
  - When the SerDes reference clock differential inputs are DC coupled externally with the clock driver chip, the maximum average current allowed for each input pin is 8 mA. In this case, the exact common mode input voltage is not critical as long as it is within the range allowed by the maximum average current of 8 mA because the input is AC-coupled on-chip.
  - This current limitation sets the maximum common mode input voltage to be less than 0.4 V (0.4 V / 50 = 8 mA) while the minimum common mode input level is 0.1 V above GND_{SXC}. For example, a clock with a 50/50 duty cycle can be produced by a clock driver with output driven by its current source from 0 mA to 16 mA (0–0.8 V), such that each phase of the differential input has a single-ended swing from 0 V to 800 mV with the common mode voltage at 400 mV.
  - If the device driving the SR[1–2]_REF_CLK and $\overline{\text{SR[1–2]\_REF\_CLK}}$ inputs cannot drive 50 Ω to GND_{SXC} DC or the drive strength of the clock driver chip exceeds the maximum input current limitations, it must be AC-coupled externally.
- The input amplitude requirement is described in detail in the following sections.

Figure 13 shows the DDR SDRAM output timing diagram.

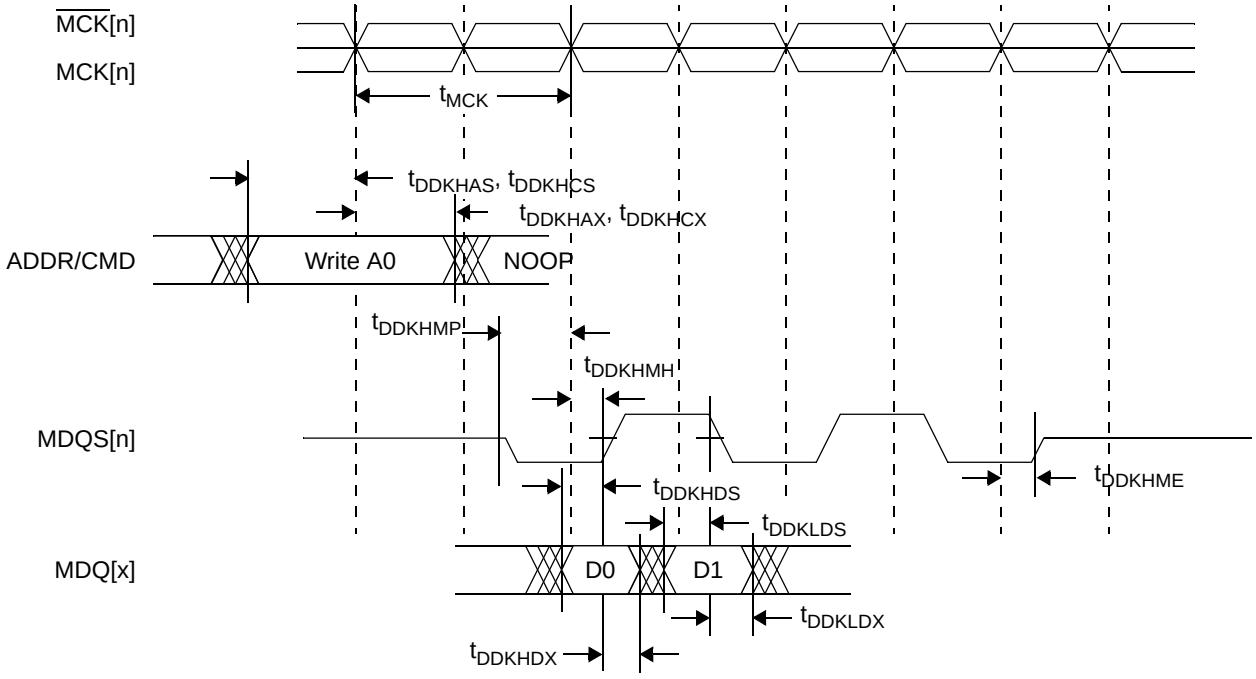


Figure 13. DDR SDRAM Output Timing

Figure 14 provides the AC test load for the DDR2 and DDR3 controller bus.

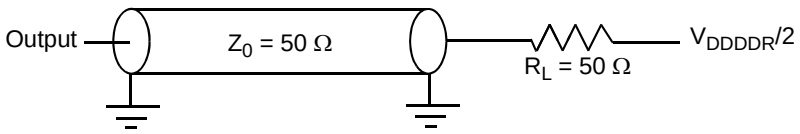


Figure 14. DDR2 and DDR3 Controller Bus AC Test Load

2.6.1.3 DDR2 and DDR3 SDRAM Differential Timing Specifications

This section describes the DC and AC differential timing specifications for the DDR2 and DDR3 SDRAM controller interface. Figure 15 shows the differential timing specification.

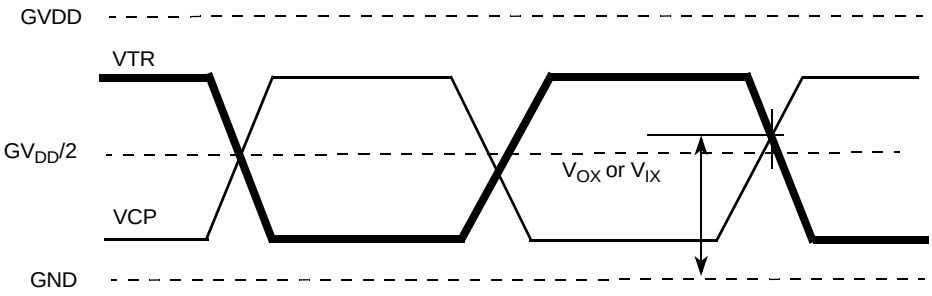
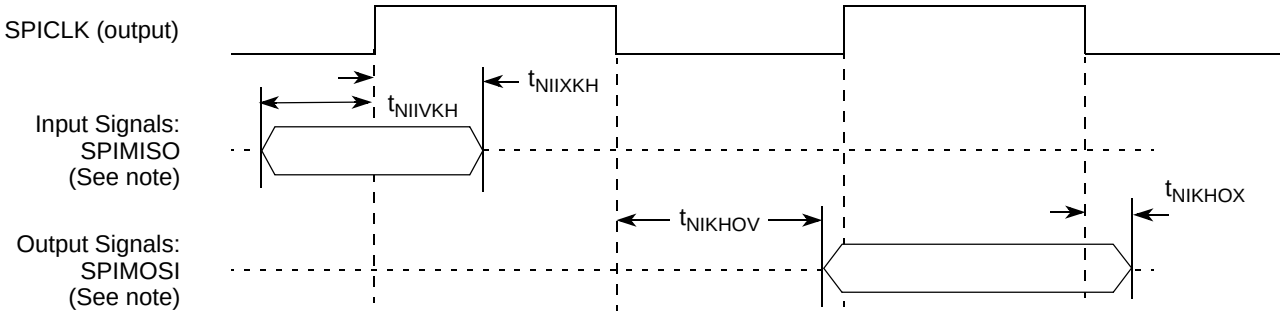


Figure 15. DDR2 and DDR3 SDRAM Differential Timing Specifications

Note: VTR specifies the true input signal (such as MCK or MDQS) and VCP is the complementary input signal (such as $\overline{\text{MCK}}$ or $\overline{\text{MDQS}}$).



Note: measured with SPMODE[CI] = 0, SPMODE[CP] = 0

Figure 28. SPI AC Timing in Master Mode (Internal Clock)

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8252 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8252 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

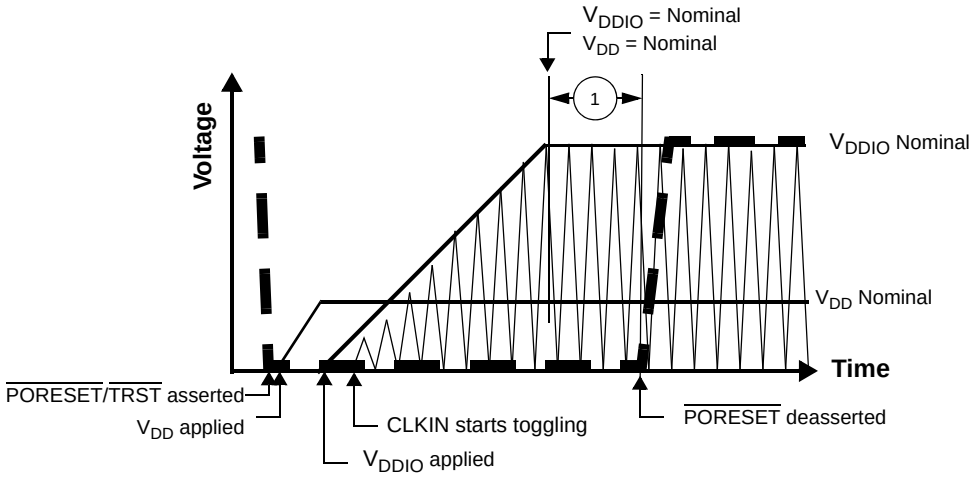


Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the *Reset* chapter in the *MSC8252 Reference Manual*.

3.3 Clock and Timing Signal Board Layout Considerations

When laying out the system board, use the following guidelines:

- Keep clock and timing signal paths as short as possible and route with 50 Ω impedance.
- Use a serial termination resistor placed close to the clock buffer to minimize signal reflection. Use the following equation to compute the resistor value:

  Rterm = Rim – Rbuf

  where Rim = trace characteristic impedance

  Rbuf = clock buffer internal impedance.

3.4 SGMII AC-Coupled Serial Link Connection Example

Figure 39 shows an example of a 4-wire AC-coupled serial link connection. For additional layout suggestions, see *AN3556 MSC815x High Speed Serial Interface Hardware Design Considerations*, available on the Freescale website or from your local sales office or representative.

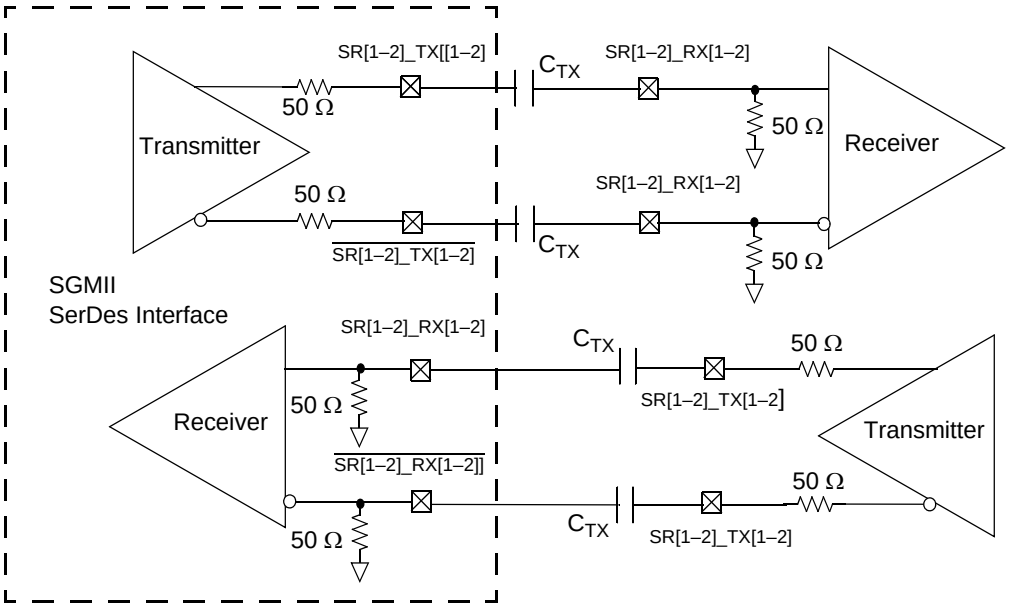


Figure 39. 4-Wire AC-Coupled SGMII Serial Link Connection Example

3.5.1 DDR Memory Related Pins

This section discusses the various scenarios that can be used with either of the MSC8252 DDR ports.

Note: The signal names in Table 40, Table 41 and Table 42 are generic names for a DDR SDRAM interface. For actual pin names refer to Table 1.

3.5.1.1 DDR Interface Is Not Used

Table 40. Connectivity of DDR Related Pins When the DDR Interface Is Not Used

Signal Name	Pin Connection
MDQ[0–63]	NC
MDQS[7–0]	NC
$\overline{\text{MDQS[7–0]}}$	NC
MA[15–0]	NC
MCK[0–2]	NC
$\overline{\text{MCK[0–2]}}$	NC
$\overline{\text{MCS[1–0]}}$	NC
MDM[7–0]	NC
MBA[2–0]	NC
$\overline{\text{MCAS}}$	NC
MCKE[1–0]	NC
MODT[1–0]	NC
MMDIC[1–0]	NC
$\overline{\text{MRAS}}$	NC
$\overline{\text{MWE}}$	NC
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC
MVREF[3]	NC
GVDD1/GVDD2[3]	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. If the DDR controller is not used, disable the internal DDR clock by setting the appropriate bit in the System Clock Control Register (SCCR) and put all DDR I/O in sleep mode by setting DRx_GCR[DDRx_DOZE] (for DDR controller x). See the *Clocks* and *General Configuration Registers* chapters in the ***MSC8252 Reference Manual*** for details.
3. For MSC8252 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.1.2 DDR Interface Is Used With 32-Bit DDR Memory Only

Table 41 lists unused pin connection when using 32-bit DDR memory. The 32 most significant data lines are not used.

Table 41. Connectivity of DDR Related Pins When Using 32-bit DDR Memory Only

Signal Name	Pin Connection
MDQ[31–0]	in use
MDQ[63–32]	NC
MDQS[3–0]	in use
MDQS[7–4]	NC
$\overline{\text{MDQS}}$[3–0]	in use
$\overline{\text{MDQS}}$[7–4]	NC
MA[15–0]	in use
MCK[2–0]	in use
$\overline{\text{MCK}}$[2–0]	in use
$\overline{\text{MCS}}$[1–0]	in use
MDM[3–0]	in use
MDM[7–4]	NC
MBA[2–0]	in use
$\overline{\text{MCAS}}$	in use
MCKE[1–0]	in use
MODT[1–0]	in use
MMDIC[1–0]	in use
$\overline{\text{MRAS}}$	in use
$\overline{\text{MWE}}$	in use
MVREF	in use
GVDD1/GVDD2	in use

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8252 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.1.3 ECC Unused Pin Connections

When the error code correction mechanism is not used in any 32- or 64-bit DDR configuration, refer to Table 42 to determine the correct pin connections.

Table 42. Connectivity of Unused ECC Mechanism Pins

Signal Name	Pin connection
MECC[7–0]	NC
MDM8	NC
MDQS8	NC
$\overline{\text{MDQS8}}$	NC

Notes:
1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is not used.
2. For MSC8252 Revision 1 silicon, these pins were connected to GND (or VDD). For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

Signal Name	Pin connection
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC

Notes: 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8252 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	NC
SR_IMP_CAL_TX	NC
$\overline{\text{SR[1–2]\_REF\_CLK}}$	SXCVSS
SR[1–2]_REF_CLK	SXCVSS
SR[1–2]_RXD[3–0]	SXCVSS
$\overline{\text{SR[1–2]\_RXD[3–0]}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD[3–0]}}$	NC
SR[1–2]_TXD[3–0]	NC
SR[1–2]_PLL_AVDD	In use
SR[1–2]_PLL_AGND	In use
SXPVSS	In use
SXCVSS	In use
SXPVDD	In use
SXCVDD	In use

Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8252 Reference Manual* for details.

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
$\overline{\text{SR[1–2]\_REF\_CLK}}$	In use
SR[1–2]_REF_CLK	In use

6 Product Documentation

Following is a general list of supporting documentation:

- *MSC8252 Technical Data Sheet* (MSC8252). Details the signals, AC/DC characteristics, clock signal characteristics, package and pinout, and electrical design considerations of the MSC8252 device.
- *MSC8252 Reference Manual* (MSC8252RM). Includes functional descriptions of the extended cores and all the internal subsystems including configuration and programming information.
- *Application Notes*. Cover various programming topics related to the StarCore DSP core and the MSC8252 device.
- *QUICC Engine Block Reference Manual with Protocol Interworking* (QEIWRM). Provides detailed information regarding the QUICC Engine technology including functional description, registers, and programming information.
- *SC3850 DSP Core Reference Manual*. Covers the SC3850 core architecture, control registers, clock registers, program control, and instruction set.
- *MSC8156SC3850 DSP Core Subsystem Reference Manual*. Covers core subsystem architecture, functionality, and registers.

7 Revision History

Table 50 provides a revision history for this data sheet.

Table 50. Document Revision History

Rev.	Date	Description
0	Apr. 2010	• Initial public release.
1	May 2010	• Changed connection for pins K17, L14, L16, M15, M17, and N14 from VDD to VSS in Table 1. • Updated **Section 3.1.2**, *Power-On Ramp Time*.
2	Jun 2010	• Changed the number of cores in the first bullet on the first page from four to two. • The correction to the L16 connection was not made in Rev. 1. Fixed the entry to change from VDD to VSS in Table 1.
3	Dec 2010	• Updated Table 16. • Updated **Section 3.1.2**, *Power-On Ramp Time*. • Updated **Section 4**, *Ordering Information*.
4	Mar 2011	• Updated Table 8. • Updated Table 15. • Updated Table 17. • Updated Table 33. • Updated Table 35. • Updated Table 39.
5	May 2011	• Updated Table 1. Changed the pin types for the following: – F25 from ground to power. – F26 from power to ground. – T6 from power to O.
6	Oct 2011	• Updated Table 34 and Table 35 to reflect 1 Gbps and 100 Mbps data rate instead of 1 GHz and 100 MHz.
7	Dec 2011	• Added note 4 to Table 39.
8	Aug 2013	• Updated Section 4, “Ordering Information”.

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Document Number: MSC8252
Rev. 8
08/2013