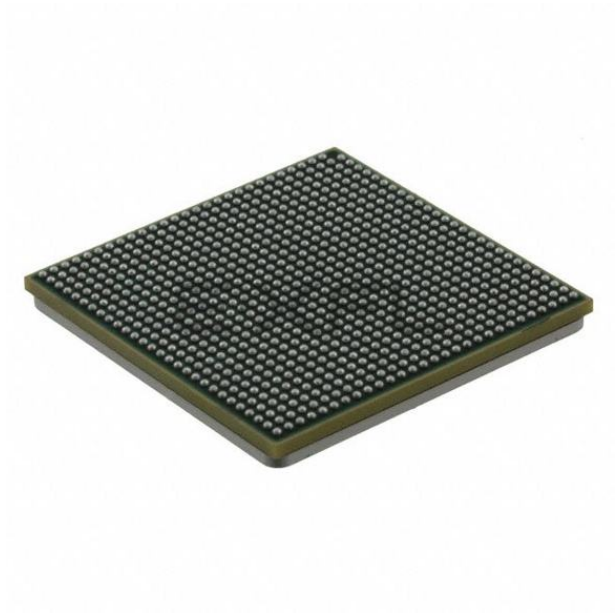

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Understanding Embedded - DSP (Digital Signal Processors)

Embedded - DSP (Digital Signal Processors) are specialized microprocessors designed to perform complex mathematical computations on digital signals in real-time. Unlike general-purpose processors, DSPs are optimized for high-speed numeric processing tasks, making them ideal for applications that require efficient and precise manipulation of digital data. These processors are fundamental in converting and processing signals in various forms, including audio, video, and communication signals, ensuring that data is accurately interpreted and utilized in embedded systems.

Applications of Embedded - DSP (Digital Signal Processors)

Details	
Product Status	Obsolete
Type	SC3850 Dual Core
Interface	Ethernet, I²C, PCI, RGMII, Serial RapidIO, SGMII, SPI, UART/USART
Clock Rate	1GHz
Non-Volatile Memory	ROM (96kB)
On-Chip RAM	576kB
Voltage - I/O	2.50V
Voltage - Core	1.00V
Operating Temperature	-40°C ~ 105°C (TJ)
Mounting Type	Surface Mount
Package / Case	783-BBGA, FCBGA
Supplier Device Package	783-FCPBGA (29x29)
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/msc8252tvt1000b

1 Pin Assignment

This section includes diagrams of the MSC8252 package ball grid array layouts and tables showing how the pinouts are allocated for the package.

1.1 FC-PBGA Ball Layout Diagram

The top view of the FC-PBGA package is shown in Figure 3 with the ball location index numbers.

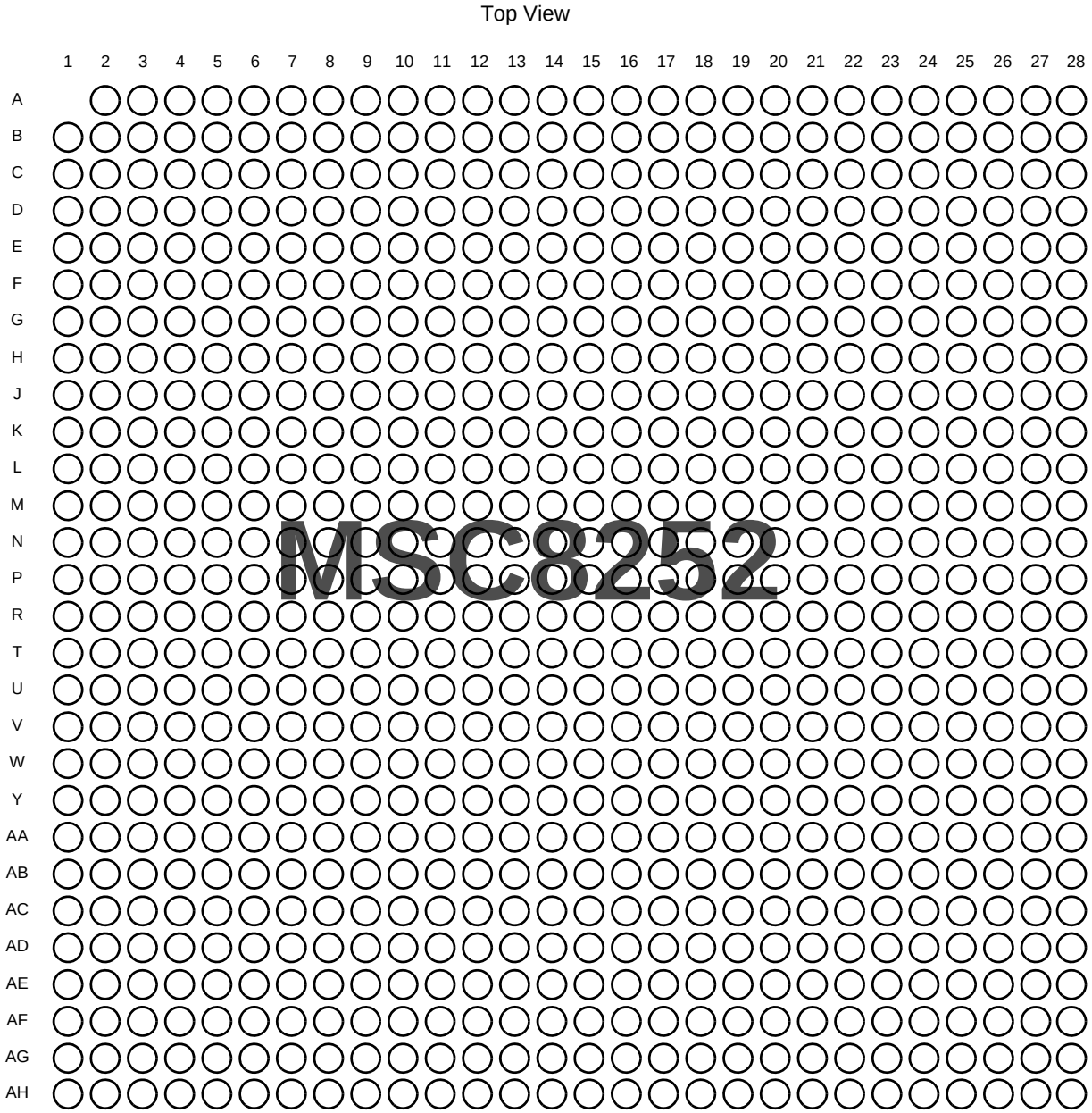


Figure 3. MSC8252 FC-PBGA Package, Top View

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
C27	Reserved	NC	—
C28	Reserved	NC	—
D1	GVDD2	Power	N/A
D2	VSS	Ground	N/A
D3	M2DQ29	I/O	GVDD2
D4	GVDD2	Power	N/A
D5	VSS	Ground	N/A
D6	M2ECC5	I/O	GVDD2
D7	GVDD2	Power	N/A
D8	VSS	Ground	N/A
D9	M2A8	O	GVDD2
D10	GVDD2	Power	N/A
D11	VSS	Ground	N/A
D12	M2A0	O	GVDD2
D13	GVDD2	Power	N/A
D14	VSS	Ground	N/A
D15	M2DQ39	I/O	GVDD2
D16	GVDD2	Power	N/A
D17	VSS	Ground	N/A
D18	M2DQ54	I/O	GVDD2
D19	GVDD2	Power	N/A
D20	VSS	Ground	N/A
D21	SXPVSS1	Ground	N/A
D22	SXPVDD1	Power	N/A
D23	SR1_TXD1	O	SXPVDD1
D24	$\overline{\text{SR1\_TXD1}}$	O	SXPVDD1
D25	SXCVSS1	Ground	N/A
D26	SXCVDD1	Power	N/A
D27	$\overline{\text{SR1\_RXD1}}$	I	SXCVDD1
D28	SR1_RXD1	I	SXCVDD1
E1	M2DQ31	I/O	GVDD2
E2	M2DQ30	I/O	GVDD2
E3	M2DQ27	I/O	GVDD2
E4	M2ECC7	I/O	GVDD2
E5	M2ECC6	I/O	GVDD2
E6	M2ECC3	I/O	GVDD2
E7	M2A9	O	GVDD2
E8	M2A6	O	GVDD2
E9	M2A3	O	GVDD2
E10	M2A10	O	GVDD2
E11	$\overline{\text{M2RAS}}$	O	GVDD2
E12	M2A2	O	GVDD2
E13	M2DQ38	I/O	GVDD2
E14	$\overline{\text{M2DQS5}}$	I/O	GVDD2
E15	M2DQS5	I/O	GVDD2
E16	M2DQ33	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
H25	SXCVSS1	Ground	N/A
H26	SXCVDD1	Power	N/A
H27	$\overline{\text{SR1\_RXD3}}$/$\overline{\text{SG2\_RX}}$[4]	I	SXCVDD1
H28	SR1_RXD3/SG2_RX[4]	I	SXCVDD1
J1	M2DQS1	I/O	GVDD2
J2	$\overline{\text{M2DQS1}}$	I/O	GVDD2
J3	M2DQ10	I/O	GVDD2
J4	M2DQ11	I/O	GVDD2
J5	M2DQ14	I/O	GVDD2
J6	M2DQ23	I/O	GVDD2
J7	M2ODT0	O	GVDD2
J8	M2A12	O	GVDD2
J9	M2A14	O	GVDD2
J10	VSS	Ground	N/A
J11	GVDD2	Power	N/A
J12	VSS	Ground	N/A
J13	GVDD2	Power	N/A
J14	VSS	Ground	N/A
J15	GVDD2	Power	N/A
J16	VSS	Ground	N/A
J17	GVDD2	Power	N/A
J18	VSS	Ground	N/A
J19	GVDD2	Power	N/A
J20	Reserved	NC	—
J21	Reserved	NC	—
J22	Reserved	NC	—
J23	SXPVDD1	Power	N/A
J24	SXPVSS1	Ground	N/A
J25	SXCVDD1	Power	N/A
J26	SXCVSS1	Ground	N/A
J27	SXCVDD1	Power	N/A
J28	SXCVSS1	Ground	N/A
K1	VSS	Ground	N/A
K2	GVDD2	Power	N/A
K3	M2DM1	O	GVDD2
K4	VSS	Ground	N/A
K5	GVDD2	Power	N/A
K6	M2DQ0	I/O	GVDD2
K7	VSS	Ground	N/A
K8	GVDD2	Power	N/A
K9	M2DQ5	I/O	GVDD2
K10	VSS	Ground	N/A
K11	VDD	Power	N/A
K12	VSS	Ground	N/A
K13	VDD	Power	N/A
K14	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
K15	VDD	Power	N/A
K16	VSS	Ground	N/A
K17	VSS	Ground	N/A
K18	VSS	Ground	N/A
K19	VDD	Power	N/A
K20	Reserved	NC	—
K21	Reserved	NC	—
K22	Reserved	NC	—
K23	SXPVDD2	Power	N/A
K24	SXPVSS2	Ground	N/A
K25	SXCVDD2	Power	N/A
K26	SXCVSS2	Ground	N/A
K27	SXCVDD2	Power	N/A
K28	SXCVSS2	Ground	N/A
L1	M2DQ9	I/O	GVDD2
L2	M2DQ12	I/O	GVDD2
L3	M2DQ13	I/O	GVDD2
L4	$\overline{\text{M2DQS0}}$	I/O	GVDD2
L5	M2DQS0	I/O	GVDD2
L6	M2DM0	O	GVDD2
L7	M2DQ3	I/O	GVDD2
L8	M2DQ2	I/O	GVDD2
L9	M2DQ4	I/O	GVDD2
L10	VDD	Power	N/A
L11	VSS	Ground	N/A
L12	M3VDD	Power	N/A
L13	VSS	Ground	N/A
L14	VSS	Ground	N/A
L15	VSS	Ground	N/A
L16	VSS	Ground	N/A
L17	VSS	Ground	N/A
L18	VDD	Power	N/A
L19	VSS	Ground	N/A
L20	Reserved	NC	—
L21	Reserved	NC	—
L22	Reserved	NC	—
L23	SR2_TXD3/PE_TXD3/SG2_TX[4]	O	SXPVDD2
L24	$\overline{\text{SR2\_TXD3}}$/$\overline{\text{PE\_TXD3}}$/$\overline{\text{SG2\_TX}}$[4]	O	SXPVDD2
L25	SXCVSS2	Ground	N/A
L26	SXCVDD2	Power	N/A
L27	$\overline{\text{SR2\_RXD3}}$/$\overline{\text{PE\_RXD3}}$/$\overline{\text{SG2\_RX}}$[4]	I	SXCVDD2
L28	SR2_RXD3/PE_RXD3/SG2_RX[4]	I	SXCVDD2
M1	M2DQ8	I/O	GVDD2
M2	VSS	Ground	N/A
M3	GVDD2	Power	N/A
M4	M2DQ15	I/O	GVDD2

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
N23	SR2_TXD2/PE_TXD2/SG1_TX[4]	O	SXPVDD2
N24	$\overline{\text{SR2\_TXD2}}$/PE_TXD2/$\overline{\text{SG1\_TX}}$[4]	O	SXPVDD2
N25	SXCVDD2	Power	N/A
N26	SXCVSS2	Ground	N/A
N27	$\overline{\text{SR2\_RXD2}}$/$\overline{\text{PE\_RXD2}}$/$\overline{\text{SG1\_RX}}$[4]	I	SXCVDD2
N28	SR2_RXD2/PE_RXD2/SG1_RX[4]	I	SXCVDD2
P1	CLKIN	I	QVDD
P2	EE0	I	QVDD
P3	QVDD	Power	N/A
P4	VSS	Ground	N/A
P5	STOP_BS	I	QVDD
P6	QVDD	Power	N/A
P7	VSS	Ground	N/A
P8	PLL0_AVDD[9]	Power	VDD
P9	PLL2_AVDD[9]	Power	VDD
P10	VSS	Ground	N/A
P11	VDD	Power	N/A
P12	VSS	Ground	N/A
P13	VDD	Power	N/A
P14	VSS	Ground	N/A
P15	VSS	Ground	N/A
P16	VSS	Ground	N/A
P17	VSS	Ground	N/A
P18	VSS	Ground	N/A
P19	VDD	Power	N/A
P20	Reserved	NC	—
P21	Reserved	NC	—
P22	Reserved	NC	—
P23	SXPVDD2	Power	N/A
P24	SXPVSS2	Ground	N/A
P25	SR2_PLL_AGND[9]	Ground	SXCVSS2
P26	SR2_PLL_AVDD[9]	Power	SXCVDD2
P27	SXCVSS2	Ground	N/A
P28	SXCVDD2	Power	N/A
R1	VSS	Ground	N/A
R2	$\overline{\text{NMI}}$	I	QVDD
R3	$\overline{\text{NMI\_OUT}}$[6]	O	QVDD
R4	$\overline{\text{HRESET}}$[6,7]	I/O	QVDD
R5	$\overline{\text{INT\_OUT}}$[6]	O	QVDD
R6	EE1	O	QVDD
R7	VSS	Ground	N/A
R8	PLL1_AVDD[9]	Power	VDD
R9	VSS	Ground	N/A
R10	VDD	Power	N/A
R11	VSS	Non-user	N/A
R12	VDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
R13	VSS	Ground	N/A
R14	VDD	Power	N/A
R15	VSS	Ground	N/A
R16	VSS	Ground	N/A
R17	VSS	Ground	N/A
R18	VDD	Power	N/A
R19	VSS	Ground	N/A
R20	VSS	Non-user	N/A
R21	SXPVSS2	Ground	N/A
R22	SXPVDD2	Power	N/A
R23	SR2_TXD1/PE_TXD1[4]	O	SXPVDD2
R24	$\overline{\text{SR2\_TXD1}}$/$\overline{\text{PE\_TXD1}}$[4]	O	SXPVDD2
R25	SXCVSS2	Ground	N/A
R26	SXCVDD2	Power	N/A
R27	$\overline{\text{SR2\_RXD1}}$/$\overline{\text{PE\_RXD1}}$[4]	I	SXCVDD2
R28	SR2_RXD1/PE_RXD1[4]	I	SXCVDD2
T1	VSS	Ground	N/A
T2	TCK	I	QVDD
T3	$\overline{\text{SRESET}}$[6,7]	I/O	QVDD
T4	TDI	I	QVDD
T5	VSS	Ground	N/A
T6	TDO	O	QVDD
T7	VSS	Ground	N/A
T8	VSS	Ground	N/A
T9	QVDD	Power	N/A
T10	VSS	Ground	N/A
T11	VDD	Power	N/A
T12	VSS	Ground	N/A
T13	M3VDD	Power	N/A
T14	VSS	Ground	N/A
T15	VDD	Power	N/A
T16	VSS	Ground	N/A
T17	VSS	Ground	N/A
T18	VSS	Ground	N/A
T19	VDD	Power	N/A
T20	VSS	Ground	N/A
T21	VSS	Non-user	N/A
T22	SR2_IMP_CAL_RX	I	SXCVDD2
T23	SXPVSS2	Ground	N/A
T24	SXPVDD2	Power	N/A
T25	SR2_REF_CLK	I	SXCVDD2
T26	$\overline{\text{SR2\_REF\_CLK}}$	I	SXCVDD2
T27	Reserved	NC	—
T28	Reserved	NC	—
U1	M1DQ8	I/O	GVDD1
U2	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
U3	GVDD1	Power	N/A
U4	M1DQ15	I/O	GVDD1
U5	M1DQ1	I/O	GVDD1
U6	VSS	Ground	N/A
U7	GVDD1	Power	N/A
U8	M1DQ7	I/O	GVDD1
U9	M1DQ6	I/O	GVDD1
U10	VDD	Power	N/A
U11	VSS	Ground	N/A
U12	M3VDD	Power	N/A
U13	VSS	Ground	N/A
U14	VDD	Power	N/A
U15	VSS	Ground	N/A
U16	VDD	Power	N/A
U17	VSS	Ground	N/A
U18	VDD	Power	N/A
U19	VSS	Ground	N/A
U20	VSS	Ground	N/A
U21	VSS	Ground	N/A
U22	VSS	Non-user	N/A
U23	SR2_TXD0/PE_TXD0[4]	O	SXPVDD2
U24	$\overline{\text{SR2\_TXD0}}/\overline{\text{PE\_TXD0}}$[4]	O	SXPVDD2
U25	SXCVDD2	Power	N/A
U26	SXCVSS2	Ground	N/A
U27	$\overline{\text{SR2\_RXD0}}/\overline{\text{PE\_RXD0}}$[4]	I	SXCVDD2
U28	SR2_RXD0/PE_RXD0[4]	I	SXCVDD2
V1	M1DQ9	I/O	GVDD1
V2	M1DQ12	I/O	GVDD1
V3	M1DQ13	I/O	GVDD1
V4	$\overline{\text{M1DQS0}}$	I/O	GVDD1
V5	M1DQS0	I/O	GVDD1
V6	M1DM0	O	GVDD1
V7	M1DQ3	I/O	GVDD1
V8	M1DQ2	I/O	GVDD1
V9	M1DQ4	I/O	GVDD1
V10	VSS	Ground	N/A
V11	VDD	Power	N/A
V12	VSS	Ground	N/A
V13	VDD	Power	N/A
V14	VSS	Ground	N/A
V15	VDD	Power	N/A
V16	VSS	Ground	N/A
V17	VDD	Power	N/A
V18	VSS	Ground	N/A
V19	VDD	Power	N/A
V20	NVDD	Power	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AC19	VSS	Ground	N/A
AC20	GVDD1	Power	N/A
AC21	VSS	Ground	N/A
AC22	NVDD	Power	N/A
AC23	GPIO30/I2C_SCL[5,8]	I/O	NVDD
AC24	GPIO26/TMR3[5,8]	I/O	NVDD
AC25	VSS	Ground	N/A
AC26	NVDD	Power	N/A
AC27	GPIO23/TMR0[5,8]	I/O	NVDD
AC28	GPIO22[5,8]	I/O	NVDD
AD1	M1DQ31	I/O	GVDD1
AD2	M1DQ30	I/O	GVDD1
AD3	M1DQ27	I/O	GVDD1
AD4	M1ECC7	I/O	GVDD1
AD5	M1ECC6	I/O	GVDD1
AD6	M1ECC3	I/O	GVDD1
AD7	M1A9	O	GVDD1
AD8	M1A6	O	GVDD1
AD9	M1A3	O	GVDD1
AD10	M1A10	O	GVDD1
AD11	$\overline{\text{M1RAS}}$	O	GVDD1
AD12	M1A2	O	GVDD1
AD13	M1DQ38	I/O	GVDD1
AD14	$\overline{\text{M1DQS}}$5	I/O	GVDD1
AD15	M1DQS5	I/O	GVDD1
AD16	M1DQ33	I/O	GVDD1
AD17	M1DQ56	I/O	GVDD1
AD18	M1DQ57	I/O	GVDD1
AD19	$\overline{\text{M1DQS7}}$	I/O	GVDD1
AD20	M1DQS7	I/O	GVDD1
AD21	VSS	Ground	N/A
AD22	GE2_TX_CTL	O	NVDD
AD23	GPIO15/DDN0/$\overline{\text{IRQ15}}$/RC15[5,8]	I/O	NVDD
AD24	GPIO13/$\overline{\text{IRQ13}}$/RC13[5,8]	I/O	NVDD
AD25	GE_MDC	O	NVDD
AD26	GE_MDIO	I/O	NVDD
AD27	TDM2TCK/GE1_TD3[3]	I/O	NVDD
AD28	TDM2RCK/GE1_TD0[3]	I/O	NVDD
AE1	GVDD1	Power	N/A
AE2	VSS	Ground	N/A
AE3	M1DQ29	I/O	GVDD1
AE4	GVDD1	Power	N/A
AE5	VSS	Ground	N/A
AE6	M1ECC5	I/O	GVDD1
AE7	GVDD1	Power	N/A
AE8	VSS	Ground	N/A

Table 1. Signal List by Ball Number (continued)

Ball Number	Signal Name[1,2]	Pin Type[10]	Power Rail Name
AH17	$\overline{\text{M1DQS6}}$	I/O	GVDD1
AH18	M1DQS6	I/O	GVDD1
AH19	M1DQ48	I/O	GVDD1
AH20	M1DQ49	I/O	GVDD1
AH21	VSS	Ground	N/A
AH22	TDM0RCK/GE2_RD2[3]	I/O	NVDD
AH23	TDM0RDT/GE2_RD3[3]	I/O	NVDD
AH24	TDM0TSN/GE2_RD0[3]	I/O	NVDD
AH25	TDM1RCK/GE2_RD1[3]	I/O	NVDD
AH26	TDM3TDT/GE1_RD3[3]	I/O	NVDD
AH27	TDM3TCK/GE1_RD2[3]	I	NVDD
AH28	VSS	Ground	N/A

Notes:
1. Reserved signals should be disconnected for compatibility with future revisions of the device. Non-user signals are reserved for manufacturing and test purposes only. The assigned signal name is used to indicate whether the signal must be unconnected (Reserved), pulled down (VSS), or pulled up (VDD).
2. Signal function during power-on reset is determined by the RCW source type.
3. Selection of TDM versus RGMII functionality is determined by the RCW bit values.
4. Selection of RapidIO, SGMII, and PCI Express functionality is determined by the RCW bit values.
5. Selection of the GPIO function and other functions is done by GPIO register setup. For configuration details, see the *GPIO* chapter in the *MSC8252 Reference Manual*.
6. Open-drain signal.
7. Internal 20 KΩ pull-up resistor.
8. For signals with GPIO functionality, the open-drain and internal 20 KΩ pull-up resistor can be configured by GPIO register programming. See the *GPIO* chapter of the *MSC8252 Reference Manual* for configuration details.
9. Connect to power supply via external filter. See **Section 3.2**, *PLL Power Supply Design Considerations* for details.
10. Pin types are: Ground = all VSS connections; Power = all VDD connections; I = Input; O = Output; I/O = Input/Output; NC = not connected.

2 Electrical Characteristics

This document contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications. For additional information, see the *MSC8252 Reference Manual*.

2.1 Maximum Ratings

In calculating timing requirements, adding a maximum value of one specification to a minimum value of another specification does not yield a reasonable sum. A maximum specification is calculated using a worst case variation of process parameter values in one direction. The minimum specification is calculated using the worst case for the same parameters in the opposite direction. Therefore, a “maximum” value for a specification never occurs in the same device with a “minimum” value for another specification; adding a maximum to a minimum represents a condition that can never exist.

Table 2 describes the maximum electrical ratings for the MSC8252.

Table 2. Absolute Maximum Ratings

Rating	Power Rail Name	Symbol	Value	Unit
Core supply voltage • Cores 0–3	VDD	V_{DD}	–0.3 to 1.1	V
PLL supply voltage[3]		V_{DDPLL0} V_{DDPLL1} V_{DDPLL2}	–0.3 to 1.1 –0.3 to 1.1 –0.3 to 1.1	V V V
M3 memory supply voltage	M3VDD	V_{DDM3}	–0.3 to 1.1	V
DDR memory supply voltage • DDR2 mode • DDR3 mode	GVDD1, GVDD2	V_{DDDDR}	 –0.3 to 1.98 –0.3 to 1.65	 V V
DDR reference voltage	MVREF	MV_{REF}	–0.3 to 0.51 × V_{DDDDR}	V
Input DDR voltage		V_{INDDR}	–0.3 to V_{DDDDR} + 0.3	V
I/O voltage excluding DDR and RapidIO lines	NVDD, QVDD	V_{DDIO}	–0.3 to 2.625	V
Input I/O voltage		V_{INIO}	–0.3 to V_{DDIO} + 0.3	V
RapidIO pad voltage	SXPVDD1, SXPVDD2	V_{DDSXP}	–0.3 to 1.26	V
Rapid I/O core voltage	SXCVDD1, SXCVDD2	V_{DDSXC}	–0.3 to 1.21	V
Rapid I/O PLL voltage[3]		$V_{DDRIOPLL}$	–0.3 to 1.21	V
Input RapidIO I/O voltage		V_{INRIO}	–0.3 to V_{DDSXC} + 0.3	V
Operating temperature		T_J	–40 to 105	°C
Storage temperature range		T_{STG}	–55 to +150	°C

Notes:
1. Functional operating conditions are given in Table 3**.**
2. Absolute maximum ratings are stress ratings only, and functional operation at the maximum is not guaranteed. Stress beyond the listed limits may affect device reliability or cause permanent damage.
3. PLL supply voltage is specified at input of the filter and not at pin of the MSC8252 (see Figure 37 and Figure 38)

2.2 Recommended Operating Conditions

Table 3 lists recommended operating conditions. Proper device operation outside of these conditions is not guaranteed.

Table 3. Recommended Operating Conditions

Rating	Symbol	Min	Nominal	Max	Unit
Core supply voltage	V_{DD}	0.97	1.0	1.05	V
M3 memory supply voltage	V_{DDM3}	0.97	1.0	1.05	V
DDR memory supply voltage • DDR2 mode • DDR3 mode DDR reference voltage	V_{DDDDR} MV_{REF}	 1.7 1.425 $0.49 \times V_{DDDDR}$	 1.8 1.5 $0.5 \times V_{DDDDR}$	 1.9 1.575 $0.51 \times V_{DDDDR}$	 V V V
I/O voltage excluding DDR and RapidIO lines	V_{DDIO}	2.375	2.5	2.625	V
Rapid I/O pad voltage	V_{DDSXP}	0.97	1.0	1.05	V
Rapid I/O core voltage	V_{DDSXC}	0.97	1.0	1.05	V
Operating temperature range: • Standard • Higher • Extended	 T_J T_J T_A T_J	 0 0 –40 —	 	 90 105 — 105	 °C °C °C
Typical power: 1 GHz at 1.0 V[1]	P	—	3.54	—	W

Notes: **1.** The typical power values are derived for a device running under the following conditions.
- Two cores running at 1 GHz, Core voltage at 1V, 75% utilization (50% control/50% DSP).
- A single 64 bit DDR3 running at 800 MHz, 50% utilization (50% reads/50% writes).
- M3 Memory 50% utilized, PCI Express controller disabled, TDM enabled 20% loading, Serial RapidIO controller disabled, 1 RGMII at 1 Gbps 50% loading.
- A junction temperature of 60°C.

2.3 Thermal Characteristics

Table 4 describes thermal characteristics of the MSC8252 for the FC-PBGA packages.

Table 4. Thermal Characteristics for the MSC8252

Characteristic	Symbol	FC-PBGA 29 × 29 mm²		Unit
		Natural Convection	200 ft/min (1 m/s) airflow	
Junction-to-ambient[1, 2]	$R_{\theta JA}$	18	12	°C/W
Junction-to-ambient, four-layer board[1, 2]	$R_{\theta JA}$	13	9	°C/W
Junction-to-board (bottom)[3]	$R_{\theta JB}$	5		°C/W
Junction-to-case[4]	$R_{\theta JC}$	0.6		°C/W

Notes:
1. Junction temperature is a function of die size, on-chip power dissipation, package thermal resistance, mounting site (board) temperature, ambient temperature, air flow, power dissipation of other components on the board, and board thermal resistance.
2. Junction-to-ambient thermal resistance determined per JEDEC JESD51-3 and JESDC51-6. Thermal test board meets JEDEC specification for the specified package.
3. Junction-to-board thermal resistance determined per JEDEC JESD 51-8. Thermal test board meets JEDEC specification for the specified package.
4. Junction-to-case at the top of the package determined using MIL- STD-883 Method 1012.1. The cold plate temperature is used for the case temperature. Reported value includes the thermal resistance of the interface layer

2.4 CLKIN Requirements

Table 5 summarizes the required characteristics for the CLKIN signal.

Table 5. CLKIN Requirements

Parameter/Condition[1]	Symbol	Min	Typ	Max	Unit	Notes
CLKIN duty cycle	—	40	—	60	%	2
CLKIN slew rate	—	1	—	4	V/ns	3
CLKIN peak period jitter	—	—	—	±150	ps	—
CLKIN jitter phase noise at –56 dBc	—	—	—	500	KHz	4
AC input swing limits	ΔV_{AC}	1.5	—	—	V	—
Input capacitance	C_{IN}	—	—	15	pf	—

Notes:
1. For clock frequencies, see the *Clock* chapter in the *MSC8252 Reference Manual.*
2. Measured at the rising edge and/or the falling edge at $V_{DDIO}/2$.
3. Slew rate as measured from ±20% to 80% of voltage swing at clock input.
4. Phase noise is calculated as FFT of TIE jitter.

2.5 DC Electrical Characteristics

This section describes the DC electrical characteristics for the MSC8252.

2.5.1 DDR SDRAM DC Electrical Characteristics

This section describes the DC electrical specifications for the DDR SDRAM interface of the MSC8252.

Note: DDR2 SDRAM uses V_{DDDDR}(typ) = 1.8 V and DDR3 SDRAM uses V_{DDDDR}(typ) = 1.5 V.

2.5.1.1 DDR2 (1.8 V) SDRAM DC Electrical Characteristics

Table 6 provides the recommended operating conditions for the DDR SDRAM controller when interfacing to DDR2 SDRAM.

Note: At recommended operating conditions (see Table 3) with V_{DDDDR} = 1.8 V.

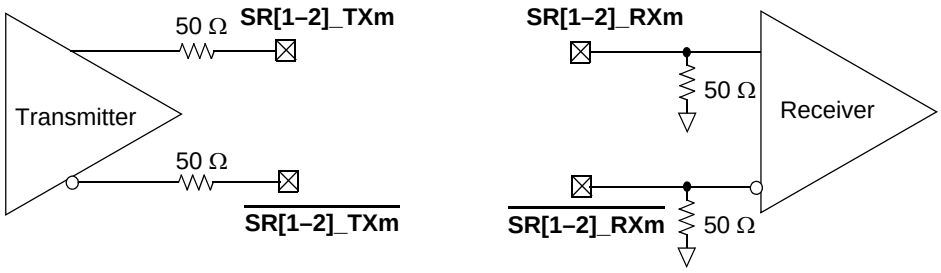
Table 6. DDR2 SDRAM Interface DC Electrical Characteristics

Parameter/Condition	Symbol	Min	Max	Unit	Notes
I/O reference voltage	MV_{REF}	0.49 × V_{DDDDR}	0.51 × V_{DDDDR}	V	2, 3, 4
Input high voltage	V_{IH}	MV_{REF} + 0.125	V_{DDDDR} + 0.3	V	5
Input low voltage	V_{IL}	–0.3	MV_{REF} – 0.125	V	5
I/O leakage current	I_{OZ}	–50	50	μA	6
Output high current (V_{OUT} (VOH) = 1.37 V)	I_{OH}	–13.4	—	mA	7
Output low current (V_{OUT} (VOL) = 0.33 V)	I_{OL}	13.4	—	mA	7

Notes:
1. V_{DDDDR} is expected to be within 50 mV of the DRAM V_{DD} supply voltage at all times. The DRAM and memory controller can use the same or different sources.
2. MV_{REF} is expected to be equal to 0.5 × V_{DDDDR}, and to track V_{DDDDR} DC variations as measured at the receiver. Peak-to-peak noise on MV_{REF} may not exceed ±2% of the DC value.
3. V_{TT} is not applied directly to the device. It is the supply to which far end signal termination is made and is expected to be equal to MV_{REF} with a minimum value of MV_{REF} – 0.4 and a maximum value of MV_{REF} + 0.04 V. V_{TT} should track variations in the DC-level of MV_{REF}.
4. The voltage regulator for MV_{REF} must be able to supply up to 300 μA.
5. Input capacitance load for DQ, DQS, and DQS signals are available in the IBIS models.
6. Output leakage is measured with all outputs are disabled, 0 V ≤ V_{OUT} ≤ V_{DDDDR}.
7. Refer to the IBIS model for the complete output IV curve characteristics.

2.5.2.3 SerDes Transmitter and Receiver Reference Circuits

Figure 6 shows the reference circuits for SerDes data lane transmitter and receiver.



Note: The [1–2] indicates the specific SerDes Interface (1 or 2) and the m indicates the specific channel within that interface (0,1,2,3). Actual signals are assigned by the HRCW assignments at reset (see **Chapter 5**, *Reset* in the reference manual for details)

Figure 6. SerDes Transmitter and Receiver Reference Circuits

2.5.3 DC-Level Requirements for SerDes Interfaces

The following subsections define the DC-level requirements for the SerDes reference clocks, the PCI Express data lines, the Serial RapidIO data lines, and the SGMII data lines.

2.5.3.1 DC-Level Requirements for SerDes Reference Clocks

The DC-level requirement for the SerDes reference clock inputs is different depending on the signaling mode used to connect the clock driver chip and SerDes reference clock inputs, as described below:

- Differential Mode
  - The input amplitude of the differential clock must be between 400 mV and 1600 mV differential peak-peak (or between 200 mV and 800 mV differential peak). In other words, each signal wire of the differential pair must have a single-ended swing of less than 800 mV and greater than 200 mV. This requirement is the same for both external DC-coupled or AC-coupled connection.
  - For an external DC-coupled connection, the maximum average current requirements sets the requirement for average voltage (common mode voltage) as between 100 mV and 400 mV. Figure 7 shows the SerDes reference clock input requirement for DC-coupled connection scheme.

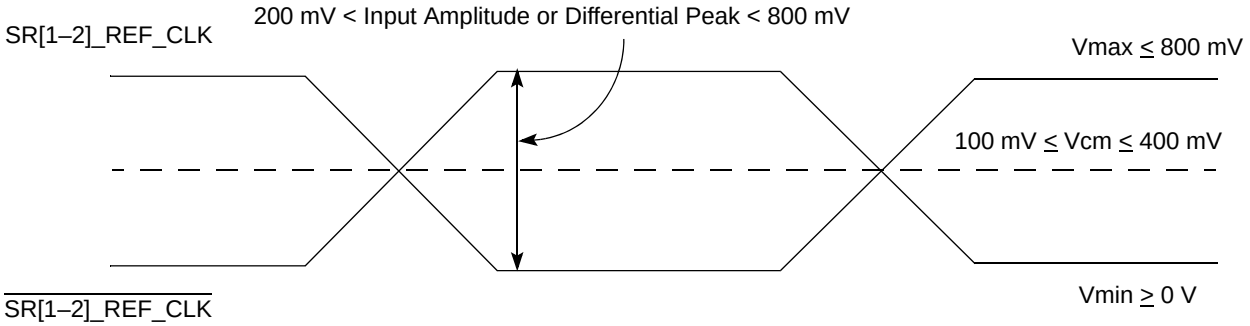


Figure 7. Differential Reference Clock Input DC Requirements (External DC-Coupled)

2.6.2.4 SGMII AC Timing Specifications

Note: Specifications are valid at the recommended operating conditions listed in Table 3.

Transmitter and receiver AC characteristics are measured at the transmitter outputs (SR[1–2]_TX[n] and $\overline{\text{SR[1–2]\_TX}}$[n]) or at the receiver inputs (SR[1–2]_RX[n] and $\overline{\text{SR[1–2]\_RX}}$[n]) as depicted in Figure 19, respectively.

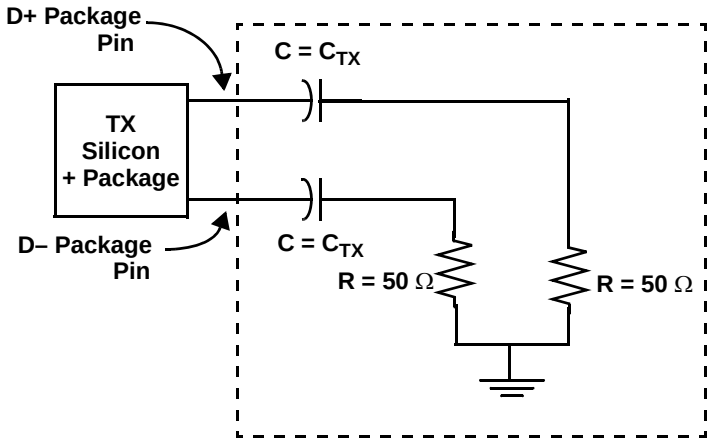


Figure 19. SGMII AC Test/Measurement Load

Table 29 provides the SGMII transmit AC timing specifications. A source synchronous clock is not supported. The AC timing specifications do not include REF_CLK jitter.

Table 29. SGMII Transmit AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter	JD	—	—	0.17	UI p-p	—
Total Jitter	JT	—	—	0.35	UI p-p	2
Unit Interval	UI	799.92	800	800.08	ps	1

Notes: 1. See Figure 18 for single frequency sinusoidal jitter limits
2. Each UI is 800 ps ± 100 ppm.

Table 30 provides the SGMII receiver AC timing specifications. The AC timing specifications do not include REF_CLK jitter.

Table 30. SGMII Receive AC Timing Specifications

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Deterministic Jitter Tolerance	JD	0.37	—	—	UI p-p	1, 2
Combined Deterministic and Random Jitter Tolerance	JDR	0.55	—	—	UI p-p	1, 2
Total Jitter Tolerance	JT	0.65	—	—	UI p-p	1,2
Bit Error Ratio	BER	—	—	10^{-12}	—	—
Unit Interval	UI	799.92	800.00	800.08	ps	3

Notes: 1. Measured at receiver.
2. Refer to RapidIO™ 1x/4x LP Serial Physical Layer Specification for interpretation of jitter specifications. Also see Figure 18.
3. Each UI is 800 ps ± 100 ppm.

Figure 21 shows the TDM transmit signal timing.

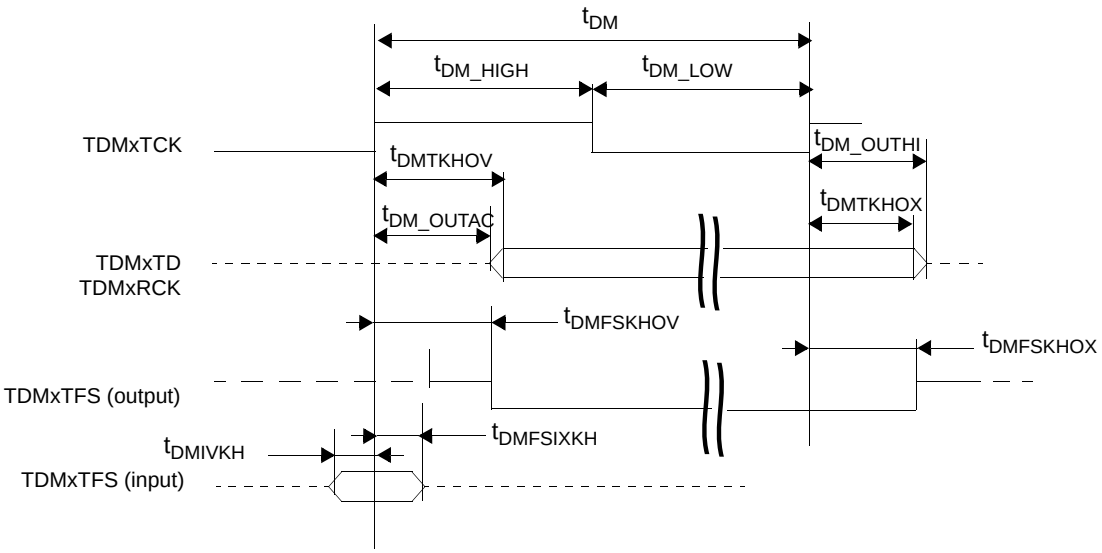


Figure 21. TDM Transmit Signals

Figure 22 provides the AC test load for the TDM/SI.

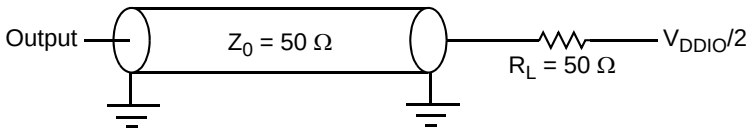


Figure 22. TDM AC Test Load

2.6.4 Timers AC Timing Specifications

Table 32 lists the timer input AC timing specifications.

Table 32. Timers Input AC Timing Specifications

Characteristics	Symbol	Minimum	Unit	Notes
Timers inputs—minimum pulse width	T_{TIWID}	8	ns	1, 2

Notes:
1. The maximum allowed frequency of timer outputs is 125 MHz. Configure the timer modules appropriately.
2. Timer inputs and outputs are asynchronous to any visible clock. Timer outputs should be synchronized before use by any external synchronous logic. Timer inputs are required to be valid for at least t_{TIWID} ns to ensure proper operation.

Note: For recommended operating conditions, see Table 3.

Figure 23 shows the AC test load for the timers.

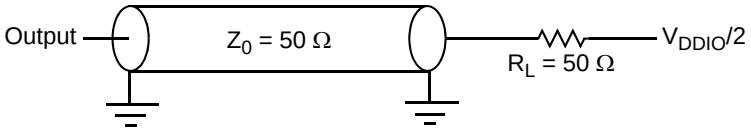


Figure 23. Timer AC Test Load

2.6.7 Asynchronous Signal Timing

Table 35 lists the asynchronous signal timing specifications.

Table 37. Signal Timing

Characteristics	Symbol	Type	Min
Input	t_{IN}	Asynchronous	One CLKIN cycle
Output	t_{OUT}	Asynchronous	Application dependent
Note: Input value relevant for EE0, $\overline{\text{IRQ}}$[15–0], and $\overline{\text{NMI}}$ only.			

The following interfaces use the specified asynchronous signals:

- *GPIO*. Signals GPIO[31–0], when used as GPIO signals, that is, when the alternate multiplexed special functions are not selected.

Note: When used as a general purpose input (GPI), the input signal should be driven until it is acknowledged by the MSC8252 device, that is, when the expected input value is read from the GPIO data register.

- *EE port*. Signals EE0, EE1.
- *Boot function*. Signal STOP_BS.
- *I^2C interface*. Signals I2C_SCL and I2C_SDA.
- *Interrupt inputs*. Signals $\overline{\text{IRQ}}$[15–0] and $\overline{\text{NMI}}$.
- *Interrupt outputs*. Signals $\overline{\text{INT\_OUT}}$ and $\overline{\text{NMI\_OUT}}$ (minimum pulse width is 32 ns).

2.6.8 JTAG Signals

Table 38 lists the JTAG timing specifications shown in Figure 29 through Figure 32.

Table 38. JTAG Timing

Characteristics	Symbol	All frequencies		Unit
		Min	Max	
TCK cycle time	t_{TCKX}	36.0	—	ns
TCK clock high phase measured at $V_M = V_{DDIO}/2$	t_{TCKH}	15.0	—	ns
Boundary scan input data setup time	t_{BSVKH}	0.0	—	ns
Boundary scan input data hold time	t_{BSXKH}	15.0	—	ns
TCK fall to output data valid	t_{TCKHOV}	—	20.0	ns
TCK fall to output high impedance	t_{TCKHOZ}	—	24.0	ns
TMS, TDI data setup time	t_{TDIVKH}	0.0	—	ns
TMS, TDI data hold time	t_{TDIXKH}	5.0	—	ns
TCK fall to TDO data valid	t_{TDOHOV}	—	10.0	ns
TCK fall to TDO high impedance	t_{TDOHOZ}	—	12.0	ns
$\overline{\text{TRST}}$ assert time	t_{TRST}	100.0	—	ns
Note: All timings apply to OnCE module data transfers as well as any other transfers via the JTAG port.				

Figure 29 shows the test clock input timing diagram

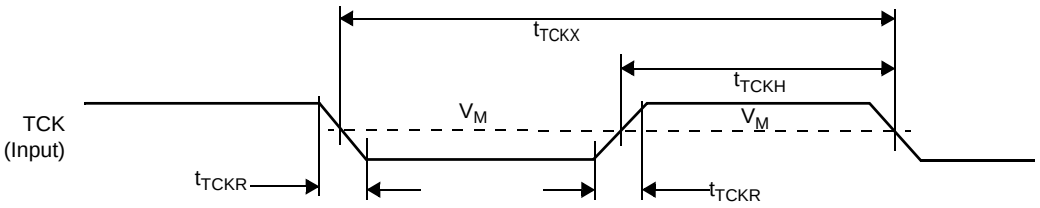


Figure 29. Test Clock Input Timing

3 Hardware Design Considerations

The following sections discuss areas to consider when the MSC8252 device is designed into a system.

3.1 Power Supply Ramp-Up Sequence

The following subsections describe the required device initialization sequence.

3.1.1 Clock, Reset, and Supply Coordination

Starting the device requires coordination between several inputs including: clock, reset, and power supplies. Follow this guidelines when starting up an MSC8252 device:

- $\overline{\text{PORESET}}$ and $\overline{\text{TRST}}$ must be asserted externally for the duration of the supply ramp-up, using the V_{DDIO} supply. $\overline{\text{TRST}}$ deassertion does not have to be synchronized with $\overline{\text{PORESET}}$ deassertion. However, $\overline{\text{TRST}}$ must be deasserted before normal operation begins to ensure correct functionality of the device.
- CLKIN should toggle at least 32 cycles before $\overline{\text{PORESET}}$ deassertion to guarantee correct device operation. The 32 cycles should only be counted from the time after V_{DDIO} reaches its nominal value (see timing 1 in Figure 33).
- CLKIN should either be stable low during ramp-up of V_{DDIO} supply (and start its swings after ramp-up) or should swing within V_{DDIO} range during V_{DDIO} ramp-up, so its amplitude grows as V_{DDIO} grows during ramp-up.

Figure 33 shows a sequence in which V_{DDIO} ramps-up after V_{DD} and CLKIN begins to toggle with the raise of V_{DDIO} supply.

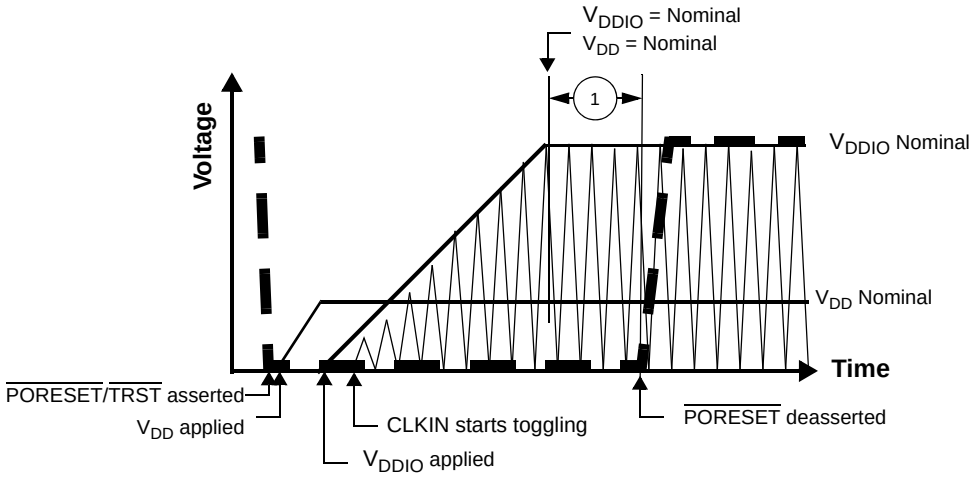


Figure 33. Supply Ramp-Up Sequence with V_{DD} Ramping Before V_{DDIO} and CLKIN Starting With V_{DDIO}

Note: For details on power-on reset flow and duration, see the *Reset* chapter in the *MSC8252 Reference Manual*.

3.2 PLL Power Supply Design Considerations

Each global PLL power supply must have an external RC filter for the PLLn_AVDD input (see Figure 37) in which the following components are defined as listed:

- R = 5 Ω ± 5%
- C1 = 10 µF ± 10%, 0603, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.
- C2 = 1.0 µF ± 10%, 0402, X5R, with ESL ≤ 0.5 nH, low ESL Surface Mount Capacitor.

Note: A higher capacitance value for C2 may be used to improve the filter as long as the other C2 parameters do not change.

All three PLLs can connect to a single supply voltage source (such as a voltage regulator) as long as the external RC filter is applied to each PLL separately. For optimal noise filtering, place the circuit as close as possible to its PLLn_AVDD inputs.

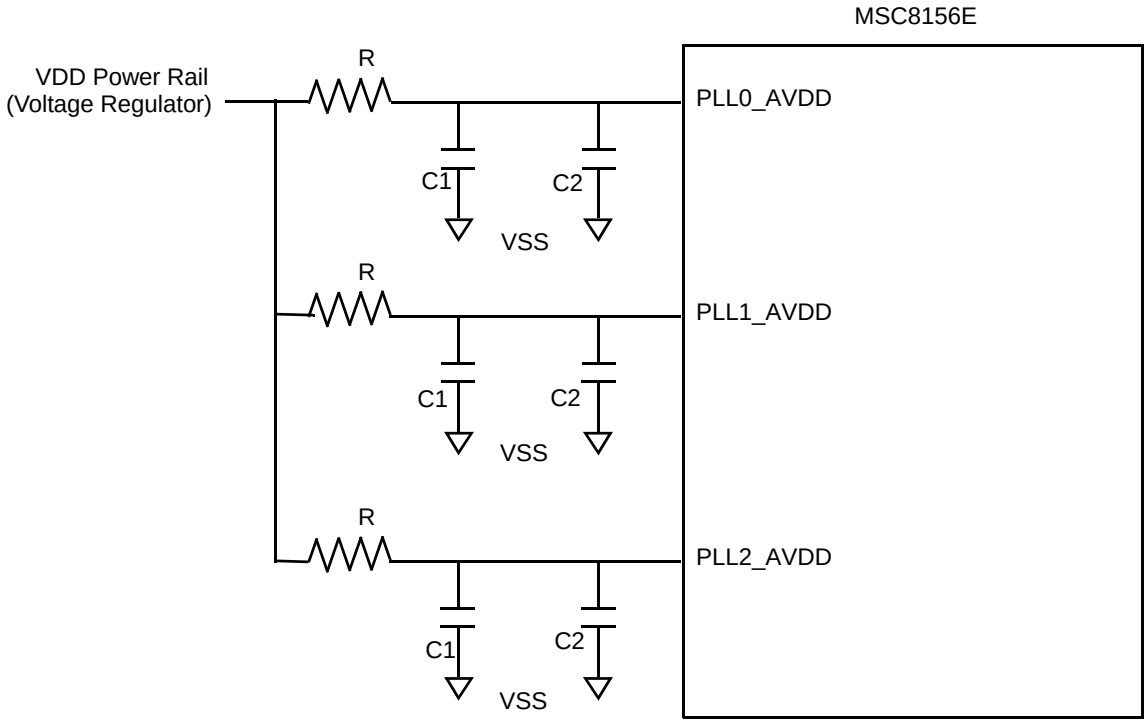


Figure 37. PLL Supplies

Each SerDes PLL power supply must be filtered using a circuit similar to the one shown in Figure 38, to ensure stability of the internal clock. For maximum effectiveness, the filter circuit should be placed as closely as possible to the SRn_PLL_AVDD ball to ensure it filters out as much noise as possible. The ground connection should be near the SRn_PLL_AVDD ball. The 0.003 µF capacitor is closest to the ball, followed by the two 2.2 µF capacitors, and finally the 1 Ω resistor to the board supply plane. The capacitors are connected from SRn_PLL_AVDD to the ground plane. Use ceramic chip capacitors with the highest possible self-resonant frequency. All trances should be kept short, wide, and direct.

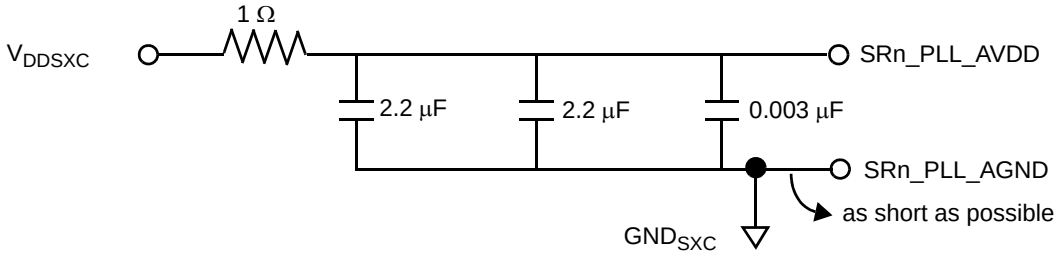


Figure 38. SerDes PLL Supplies

3.5.1.4 DDR2 Unused MAPAR Pin Connections

When the MAPAR signals are not used, refer to Table 43 to determine the correct pin connections.

Table 43. Connectivity of MAPAR Pins for DDR2

Signal Name	Pin connection
MAPAR_OUT	NC
$\overline{\text{MAPAR\_IN}}$	NC

Notes: 1. For the signals listed in this table, the initial M stands for M1 or M2 depending on which DDR controller is used for DDR2.
2. For MSC8252 Revision 1 silicon, these pins were connected to GND. For newer revisions of the MSC8252, connecting these pins to GND increases device power consumption.

3.5.2 HSSI-Related Pins

3.5.2.1 HSSI Port Is Not Used

The signal names in Table 44 and Table 45 are generic names for a RapidIO interface. For actual pin names refer to Table 1.

Table 44. Connectivity of Serial RapidIO Interface Related Pins When the RapidIO Interface Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	NC
SR_IMP_CAL_TX	NC
$\overline{\text{SR[1–2]\_REF\_CLK}}$	SXCVSS
SR[1–2]_REF_CLK	SXCVSS
SR[1–2]_RXD[3–0]	SXCVSS
$\overline{\text{SR[1–2]\_RXD[3–0]}}$	SXCVSS
$\overline{\text{SR[1–2]\_TXD[3–0]}}$	NC
SR[1–2]_TXD[3–0]	NC
SR[1–2]_PLL_AVDD	In use
SR[1–2]_PLL_AGND	In use
SXPVSS	In use
SXCVSS	In use
SXPVDD	In use
SXCVDD	In use

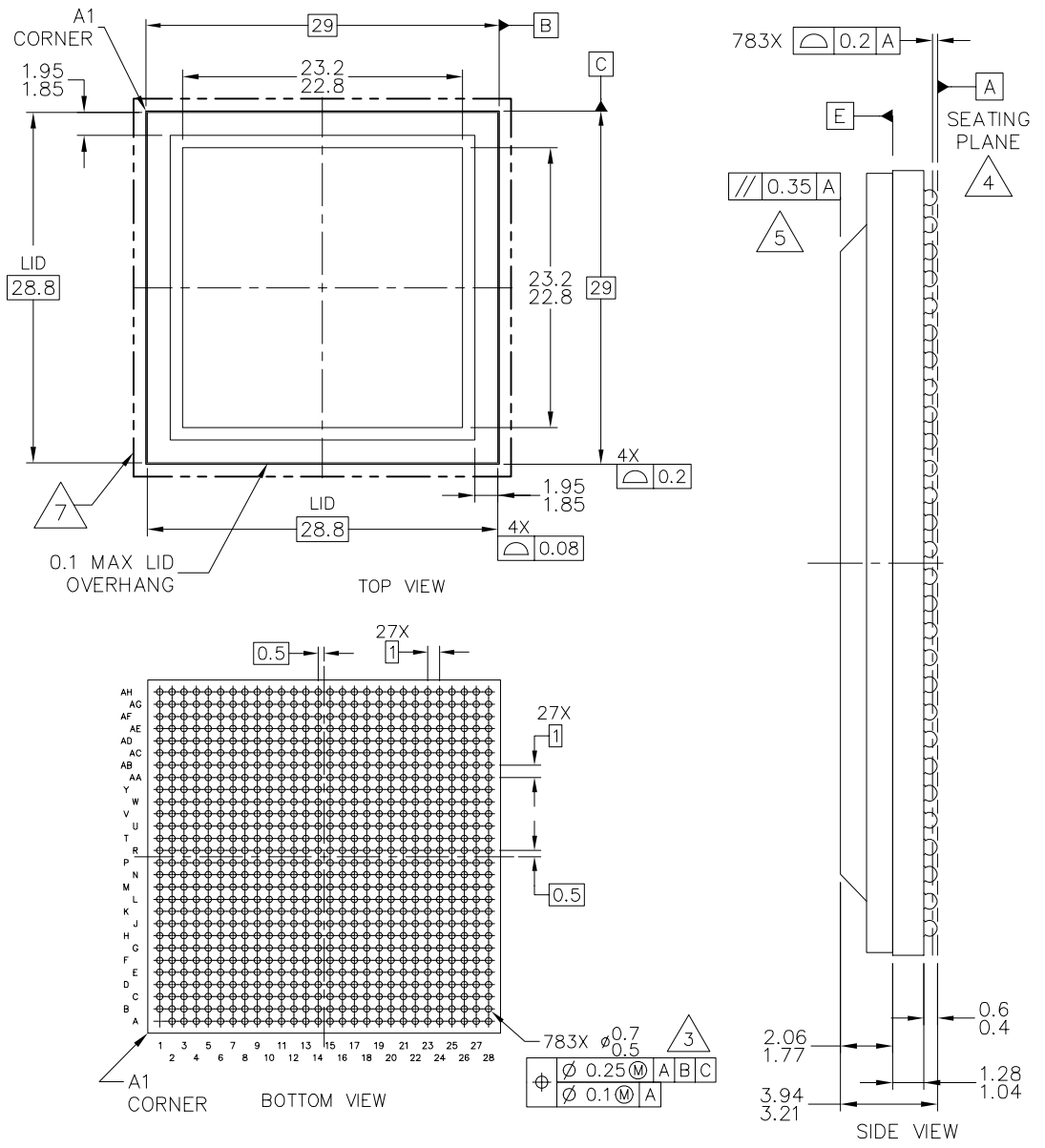
Note: All lanes in the HSSI SerDes should be powered down. Refer to the *MSC8252 Reference Manual* for details.

3.5.2.2 HSSI Specific Lane Is Not Used

Table 45. Connectivity of HSSI Related Pins When Specific Lane Is Not Used

Signal Name	Pin Connection
SR_IMP_CAL_RX	In use
SR_IMP_CAL_TX	In use
$\overline{\text{SR[1–2]\_REF\_CLK}}$	In use
SR[1–2]_REF_CLK	In use

5 Package Information



NOTES:

1. ALL DIMENSIONS IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. MAXIMUM SOLDER BALL DIAMETER MEASURE PARALLEL TO DATUM A.
4. DATUM A, THE SEATING PLANE, IS DETERMINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
5. PARALLELISM MEASUREMENT SHALL EXCLUDE ANY EFFECT OF MARK ON TOP SURFACE OF PACKAGE.
6. ALL DIMENSIONS ARE SYMMETRIC ACROSS THE PACKAGE CENTER LINES, UNLESS DIMENSIONED OTHERWISE.
7. 29.2MM MAXIMUM PACKAGE ASSEMBLY (LID + LAMINATE) X AND Y.

Figure 40. MSC8252 Mechanical Information, 783-ball FC-PBGA Package