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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

Product Status	Discontinued at Digi-Key
Core Processor	ARM® Cortex®-M4F
Core Size	32-Bit Single-Core
Speed	48MHz
Connectivity	I ² C, IrDA, SmartCard, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, DMA, I ² S, POR, PWM, WDT
Number of I/O	56
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	32K x 8
Voltage - Supply (Vcc/Vdd)	1.98V ~ 3.8V
Data Converters	A/D 8x12b; D/A 2x12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	64-VFQFN Exposed Pad
Supplier Device Package	64-QFN (9x9)
Purchase URL	https://www.e-xfl.com/product-detail/silicon-labs/efm32wg230f64-qfn64

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

2 System Summary

2.1 System Introduction

The EFM32 MCUs are the world's most energy friendly microcontrollers. With a unique combination of the powerful 32-bit ARM Cortex-M4, with DSP instruction support and floating-point unit, innovative low energy techniques, short wake-up time from energy saving modes, and a wide selection of peripherals, the EFM32WG microcontroller is well suited for any battery operated application as well as other systems requiring high performance and low-energy consumption. This section gives a short introduction to each of the modules in general terms and also shows a summary of the configuration for the EFM32WG230 devices. For a complete feature set and in-depth information on the modules, the reader is referred to the *EFM32WG Reference Manual*.

A block diagram of the EFM32WG230 is shown in Figure 2.1 (p. 3) .



Figure 2.1. Block Diagram

2.1.1 ARM Cortex-M4 Core

The ARM Cortex-M4 includes a 32-bit RISC processor, with DSP instruction support and floating-point unit, which can achieve as much as 1.25 Dhrystone MIPS/MHz. A Memory Protection Unit with support for up to 8 memory segments is included, as well as a Wake-up Interrupt Controller handling interrupts triggered while the CPU is asleep. The EFM32 implementation of the Cortex-M4 is described in detail in *ARM Cortex-M4 Devices Generic User Guide*.

2.1.2 Debug Interface (DBG)

This device includes hardware debug support through a 2-pin serial-wire debug interface and an Embedded Trace Module (ETM) for data/instruction tracing. In addition there is also a 1-wire Serial Wire Viewer pin which can be used to output profiling information, data trace and software-generated messages.

2.1.19 Analog Comparator (ACMP)

The Analog Comparator is used to compare the voltage of two analog inputs, with a digital output indicating which input voltage is higher. Inputs can either be one of the selectable internal references or from external pins. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.20 Voltage Comparator (VCMP)

The Voltage Supply Comparator is used to monitor the supply voltage from software. An interrupt can be generated when the supply falls below or rises above a programmable threshold. Response time and thereby also the current consumption can be configured by altering the current supply to the comparator.

2.1.21 Analog to Digital Converter (ADC)

The ADC is a Successive Approximation Register (SAR) architecture, with a resolution of up to 12 bits at up to one million samples per second. The integrated input mux can select inputs from 8 external pins and 6 internal signals.

2.1.22 Digital to Analog Converter (DAC)

The Digital to Analog Converter (DAC) can convert a digital value to an analog output voltage. The DAC is fully differential rail-to-rail, with 12-bit resolution. It has two single ended output buffers which can be combined into one differential output. The DAC may be used for a number of different applications such as sensor interfaces or sound output.

2.1.23 Operational Amplifier (OPAMP)

The EFM32WG230 features 3 Operational Amplifiers. The Operational Amplifier is a versatile general purpose amplifier with rail-to-rail differential input and rail-to-rail single ended output. The input can be set to pin, DAC or OPAMP, whereas the output can be pin, OPAMP or ADC. The current is programmable and the OPAMP has various internal configurations such as unity gain, programmable gain using internal resistors etc.

2.1.24 Low Energy Sensor Interface (LESENSE)

The Low Energy Sensor Interface (LESENSETM), is a highly configurable sensor interface with support for up to 16 individually configurable sensors. By controlling the analog comparators and DAC, LESENSE is capable of supporting a wide range of sensors and measurement schemes, and can for instance measure LC sensors, resistive sensors and capacitive sensors. LESENSE also includes a programmable FSM which enables simple processing of measurement results without CPU intervention. LESENSE is available in energy mode EM2, in addition to EM0 and EM1, making it ideal for sensor monitoring in applications with a strict energy budget.

2.1.25 Backup Power Domain

The backup power domain is a separate power domain containing a Backup Real Time Counter, BURTC, and a set of retention registers, available in all energy modes. This power domain can be configured to automatically change power source to a backup battery when the main power drains out. The backup power domain enables the EFM32WG230 to keep track of time and retain data, even if the main power source should drain out.

2.1.26 Advanced Encryption Standard Accelerator (AES)

The AES accelerator performs AES encryption and decryption with 128-bit or 256-bit keys. Encrypting or decrypting one 128-bit data block takes 52 HFCORECLK cycles with 128-bit keys and 75 HFCORECLK cycles with 256-bit keys. The AES module is an AHB slave which enables efficient access to the data

Module	Configuration	Pin Connections
PCNT0	Full configuration, 16-bit count register	PCNT0_S[1:0]
PCNT1	Full configuration, 8-bit count register	PCNT1_S[1:0]
PCNT2	Full configuration, 8-bit count register	PCNT2_S[1:0]
ACMP0	Full configuration	ACMP0_CH[7:0], ACMP0_O
ACMP1	Full configuration	ACMP1_CH[7:0], ACMP1_O
VCMP	Full configuration	NA
ADC0	Full configuration	ADC0_CH[7:0]
DAC0	Full configuration	DAC0_OUT[1:0], DAC0_OUTxALT
ОРАМР	Full configuration	Outputs: OPAMP_OUTx, OPAMP_OUTxALT, Inputs: OPAMP_Px, OPAMP_Nx
AES	Full configuration	NA
GPIO	56 pins	Available pins are shown in Table 4.3 (p. 60)

2.3 Memory Map

The *EFM32WG230* memory map is shown in Figure 2.2 (p. 8), with RAM and Flash sizes for the largest memory configuration.

Figure 2.2. EFM32WG230 Memory Map with largest RAM and Flash sizes



3 Electrical Characteristics

3.1 Test Conditions

3.1.1 Typical Values

The typical data are based on $T_{AMB}=25^{\circ}C$ and $V_{DD}=3.0$ V, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.1.2 Minimum and Maximum Values

The minimum and maximum values represent the worst conditions of ambient temperature, supply voltage and frequencies, as defined in Table 3.2 (p. 9), by simulation and/or technology characterisation unless otherwise specified.

3.2 Absolute Maximum Ratings

The absolute maximum ratings are stress ratings, and functional operation under such conditions are not guaranteed. Stress beyond the limits specified in Table 3.1 (p. 9) may affect the device reliability or cause permanent damage to the device. Functional operating conditions are given in Table 3.2 (p. 9).

Symbol	Parameter	Condition	Min	Тур	Max	Unit
T _{STG}	Storage tempera- ture range		-40		150 ¹	°C
T _S	Maximum soldering temperature	Latest IPC/JEDEC J-STD-020 Standard			260	°C
V _{DDMAX}	External main sup- ply voltage		0		3.8	V
V _{IOPIN}	Voltage on any I/O pin		-0.3		V _{DD} +0.3	V

Table 3.1. Absolute Maximum Ratings

¹Based on programmed devices tested for 10000 hours at 150°C. Storage temperature affects retention of preprogrammed calibration values stored in flash. Please refer to the Flash section in the Electrical Characteristics for information on flash data retention for different temperatures.

3.3 General Operating Conditions

3.3.1 General Operating Conditions

Table 3.2. General Operating Conditions

Symbol	Parameter	Min	Тур	Мах	Unit
T _{AMB}	Ambient temperature range	-40		85	°C
V _{DDOP}	Operating supply voltage	1.98		3.8	V
f _{APB}	Internal APB clock frequency			48	MHz
f _{AHB}	Internal AHB clock frequency			48	MHz



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		1.2 MHz HFRCO, all peripher- al clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		271	286	µA/ MHz
		1.2 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		275		μΑ/ MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		63	75	µA/ MHz
		48 MHz HFXO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		65	76	µA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		64	75	µA/ MHz
		28 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		65	77	μΑ/ MHz
	EM1 current (Pro- duction test condi- tion = 14 MHz)	21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		65	76	μΑ/ MHz
		21 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		66	78	μΑ/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		67	79	µA/ MHz
		14 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		68	82	μΑ/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		68	81	μΑ/ MHz
		11 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		70	83	μΑ/ MHz
		6.6 MHz HFRCO, all peripher- al clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		74	87	μΑ/ MHz
		6.6 MHz HFRCO, all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		76	89	µA/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =25°C		106	120	μΑ/ MHz
		1.2 MHz HFRCO. all peripheral clocks disabled, V_{DD} = 3.0 V, T_{AMB} =85°C		112	129	μΑ/ MHz
I _{EM2}	EM2 current	EM2 current with RTC prescaled to 1 Hz, 32.768 kHz LFRCO, V_{DD} = 3.0 V, T_{AMB} =25°C		0.95 ¹	1.7 ¹	μΑ

Figure 3.5. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 11MHz



Figure 3.6. EM1 Current consumption with all peripheral clocks disabled and HFRCO running at 6.6MHz







3.4.2 EM2 Current Consumption

Figure 3.8. EM2 current consumption. RTC¹ prescaled to 1kHz, 32.768 kHz LFRCO.



¹Using backup RTC.

3.4.3 EM3 Current Consumption

Figure 3.9. EM3 current consumption.





3.4.4 EM4 Current Consumption

Figure 3.10. EM4 current consumption.



3.5 Transition between Energy Modes

The transition times are measured from the trigger to the first clock edge in the CPU.

Table 3.5. Energy wodes Transitions	Table	3.5.	Energy	Modes	Transitions
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Symbol	Parameter	Min	Тур	Max	Unit
t _{EM10}	Transition time from EM1 to EM0		0		HF- CORE- CLK cycles
t _{EM20}	Transition time from EM2 to EM0		2		μs
t _{EM30}	Transition time from EM3 to EM0		2		μs
t _{EM40}	Transition time from EM4 to EM0		163		μs

3.6 Power Management

The EFM32WG requires the AVDD_x, VDD_DREG and IOVDD_x pins to be connected together (with optional filter) at the PCB level. For practical schematic recommendations, please see the application note, "AN0002 EFM32 Hardware Design Considerations".

Table 3.6. Power Management

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V _{BODextthr} -	BOD threshold on falling external supply voltage		1.74		1.96	V
V _{BODextthr+}	BOD threshold on rising external sup- ply voltage			1.85	1.98	V
V _{PORthr+}	Power-on Reset (POR) threshold on rising external sup- ply voltage				1.98	V
t _{RESET}	Delay from reset is released until program execution starts	Applies to Power-on Reset, Brown-out Reset and pin reset.		163		μs
C _{DECOUPLE}	Voltage regulator decoupling capaci- tor.	X5R capacitor recommended. Apply between DECOUPLE pin and GROUND		1		μF

3.7 Flash

Table 3.7. Flash

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
EC _{FLASH}	Flash erase cycles before failure		20000			cycles
		T _{AMB} <150°C	10000			h
RET _{FLASH}	Flash data retention	T _{AMB} <85°C	10			years
		T _{AMB} <70°C	20			years
t _{W_PROG}	Word (32-bit) pro- gramming time		20			μs
t _{PERASE}	Page erase time		20	20.4	20.8	ms
t _{DERASE}	Device erase time		40	40.8	41.6	ms
I _{ERASE}	Erase current				7 ¹	mA
I _{WRITE}	Write current				7 ¹	mA
V _{FLASH}	Supply voltage dur- ing flash erase and write		1.98		3.8	V

¹Measured at 25°C



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		Sinking 20 mA, V _{DD} =3.0 V, GPIO_Px_CTRL DRIVEMODE = HIGH			0.25V _{DD}	V
I _{IOLEAK}	Input leakage cur- rent	High Impedance IO connected to GROUND or Vdd		±0.1	±100	nA
R _{PU}	I/O pin pull-up resis- tor			40		kOhm
R _{PD}	I/O pin pull-down re- sistor			40		kOhm
R _{IOESD}	Internal ESD series resistor			200		Ohm
t _{IOGLITCH}	Pulse width of puls- es to be removed by the glitch sup- pression filter		10		50	ns
tioof	Output fall time	GPIO_Px_CTRL DRIVEMODE = LOWEST and load capaci- tance C_L =12.5-25pF.	20+0.1C _L		250	ns
			20+0.1C _L		250	ns
V _{IOHYST}	I/O pin hysteresis (V _{IOTHR+} - V _{IOTHR-})	V _{DD} = 1.98 - 3.8 V	0.10V _{DD}			V

Figure 3.22. Calibrated HFRCO 21 MHz Band Frequency vs Supply Voltage and Temperature



Figure 3.23. Calibrated HFRCO 28 MHz Band Frequency vs Supply Voltage and Temperature





Symbol	Parameter	Condition	Min	Тур	Max	Unit
	erence voltage on channel 6					
V _{ADCCMIN}	Common mode in- put range		0		V _{DD}	V
	Input current	2pF sampling capacitors		<100		nA
CMRR _{ADC}	Analog input com- mon mode rejection ratio			65		dB
		1 MSamples/s, 12 bit, external reference		351		μA
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b00		67		μΑ
I _{ADC}	Average active cur- rent	10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b01		63		μΑ
		10 kSamples/s 12 bit, internal 1.25 V reference, WARMUP- MODE in ADCn_CTRL set to 0b10		64		μΑ
I _{ADCREF}	Current consump- tion of internal volt- age reference	Internal voltage reference		65		μΑ
C _{ADCIN}	Input capacitance			2		pF
R _{ADCIN}	Input ON resistance		1			MOhm
R _{ADCFILT}	Input RC filter resis- tance			10		kOhm
C _{ADCFILT}	Input RC filter/de- coupling capaci- tance			250		fF
f _{ADCCLK}	ADC Clock Fre- quency				13	MHz
		6 bit	7			ADC- CLK Cycles
t _{ADCCONV}	Conversion time	8 bit	11			ADC- CLK Cycles
		12 bit	13			ADC- CLK Cycles
t _{ADCACQ}	Acquisition time	Programmable	1		256	ADC- CLK Cycles
t _{ADCACQVDD3}	Required acquisi- tion time for VDD/3 reference		2			μs
t _{ADCSTART}	Startup time of ref- erence generator			5		μs



Symbol	Parameter	Condition	Min	Тур	Max	Unit
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		64		dB
		1 MSamples/s, 12 bit, differen- tial, 5V reference		54		dB
		1 MSamples/s, 12 bit, differential, V_{DD} reference		66		dB
		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		68		dB
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		61		dB
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		65		dB
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, internal 1.25V reference		63		dB
		200 kSamples/s, 12 bit, differ- ential, internal 2.5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, 5V reference		66		dB
		200 kSamples/s, 12 bit, differ- ential, V _{DD} reference	62	66		dB
		200 kSamples/s, 12 bit, differ- ential, 2xV _{DD} reference		69		dB
		1 MSamples/s, 12 bit, single ended, internal 1.25V refer- ence		64		dBc
		1 MSamples/s, 12 bit, single ended, internal 2.5V reference		76		dBc
		1 MSamples/s, 12 bit, single ended, V _{DD} reference		73		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 1.25V reference		66		dBc
		1 MSamples/s, 12 bit, differen- tial, internal 2.5V reference		77		dBc
SFDR _{ADC}	Spurious-Free Dy- namic Range (SF- DR)	1 MSamples/s, 12 bit, differential, V_{DD} reference		76		dBc
		1 MSamples/s, 12 bit, differen- tial, 2xV _{DD} reference		75		dBc
		1 MSamples/s, 12 bit, differen- tial, 5V reference		69		dBc
		200 kSamples/s, 12 bit, sin- gle ended, internal 1.25V refer- ence		75		dBc
		200 kSamples/s, 12 bit, single ended, internal 2.5V reference		75		dBc
		200 kSamples/s, 12 bit, single ended, V _{DD} reference		76		dBc



Figure 3.34. OPAMP Negative Power Supply Rejection Ratio



Figure 3.35. OPAMP Voltage Noise Spectral Density (Unity Gain) Vout=1V



Figure 3.36. OPAMP Voltage Noise Spectral Density (Non-Unity Gain)



3.14 Voltage Comparator (VCMP)

Table 3.19. VCMP

Symbol	Parameter	Condition	Min	Тур	Мах	Unit
V _{VCMPIN}	Input voltage range			V _{DD}		V
V _{VCMPCM}	VCMP Common Mode voltage range			V _{DD}		V
IVCMP	Active current	BIASPROG=0b0000 and HALFBIAS=1 in VCMPn_CTRL register		0.3	0.6	μA
		BIASPROG=0b1111 and HALFBIAS=0 in VCMPn_CTRL register. LPREF=0.		22	35	μA
t _{VCMPREF}	Startup time refer- ence generator	NORMAL		10		μs
V _{VCMPOFFSET}	Offset voltage	Single ended		10		mV
	Unset voltage	Differential		10		mV
V _{VCMPHYST}	VCMP hysteresis			61	210	mV
t _{VCMPSTART}	Startup time				10	μs

The V_{DD} trigger level can be configured by setting the TRIGLEVEL field of the VCMP_CTRL register in accordance with the following equation:

VCMP Trigger Level as a Function of Level Setting

V_{DD Trigger Level}=1.667V+0.034 ×TRIGLEVEL

3.15 I2C

Table 3.20. I2C Standard-mode (Sm)

Symbol	Parameter	Min	Тур	Мах	Unit
f _{SCL}	SCL clock frequency	0		100 ¹	kHz
t _{LOW}	SCL clock low time	4.7			μs
t _{HIGH}	SCL clock high time	4.0			μs
t _{SU,DAT}	SDA set-up time	250			ns
t _{HD,DAT}	SDA hold time	8		3450 ^{2,3}	ns
t _{SU,STA}	Repeated START condition set-up time	4.7			μs
t _{HD,STA}	(Repeated) START condition hold time	4.0			μs
t _{SU,STO}	STOP condition set-up time	4.0			μs
t _{BUF}	Bus free time between a STOP and a START condition	4.7			μs

¹For the minimum HFPERCLK frequency required in Standard-mode, see the I2C chapter in the EFM32WG Reference Manual. ²The maximum SDA hold time ($t_{HD,DAT}$) needs to be met only when the device does not stretch the low time of SCL (t_{LOW}). ³When transmitting data, this number is guaranteed only when I2Cn_CLKDIV < ((3450*10⁻⁹ [s] * f_{HFPERCLK} [Hz]) - 4).

(3.2)



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Symbol	Parameter	Min	Тур	Мах	Unit
t _{SCLK_MI} ¹²	SCLK to MISO	-264 + t _{HF-} PERCLK		-234 + 2 * t _{HFPERCLK}	ns

¹Applies for both CLKPHA = 0 and CLKPHA = 1 (figure only shows CLKPHA = 0)

 $^2\text{Measurement}$ done at 10% and 90% of V_{DD} (figure shows 50% of $_{\text{VDD}})$

3.17 Digital Peripherals

Table 3.27. Digital Peripherals

Symbol	Parameter	Condition	Min	Тур	Max	Unit
I _{USART}	USART current	USART idle current, clock en- abled		4.0		µA/ MHz
I _{UART}	UART current	UART idle current, clock en- abled		3.8		μΑ/ MHz
I _{LEUART}	LEUART current	LEUART idle current, clock en- abled		194.0		nA
I _{I2C}	I2C current	I2C idle current, clock enabled		7.6		µA/ MHz
I _{TIMER}	TIMER current	TIMER_0 idle current, clock enabled		6.5		µA/ MHz
I _{LETIMER}	LETIMER current	LETIMER idle current, clock enabled		85.8		nA
I _{PCNT}	PCNT current	PCNT idle current, clock en- abled		91.4		nA
I _{RTC}	RTC current	RTC idle current, clock enabled		54.6		nA
I _{AES}	AES current	AES idle current, clock enabled		1.8		μΑ/ MHz
I _{GPIO}	GPIO current	GPIO idle current, clock en- abled		3.4		μΑ/ MHz
I _{PRS}	PRS current	PRS idle current		3.9		μΑ/ MHz
I _{DMA}	DMA current	Clock enable		10.9		μΑ/ MHz

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Alternate	LOCATION							
Functionality	0	1	2	3	4	5	6	Description
LETIM0_OUT0	PD6	PB11	PF0	PC4				Low Energy Timer LETIM0, output channel 0.
LETIM0_OUT1	PD7	PB12	PF1	PC5				Low Energy Timer LETIM0, output channel 1.
LEU0_RX	PD5	PB14	PE15	PF1	PA0			LEUART0 Receive input.
LEU0_TX	PD4	PB13	PE14	PF0	PF2			LEUART0 Transmit output. Also used as receive input in half duplex communication.
LEU1_RX	PC7	PA6						LEUART1 Receive input.
LEU1_TX	PC6	PA5						LEUART1 Transmit output. Also used as receive input in half duplex communication.
LFXTAL_N	PB8							Low Frequency Crystal (typically 32.768 kHz) negative pin. Also used as an optional external clock input pin.
LFXTAL_P	PB7							Low Frequency Crystal (typically 32.768 kHz) positive pin.
PCNT0_S0IN	PC13		PC0	PD6				Pulse Counter PCNT0 input number 0.
PCNT0_S1IN	PC14		PC1	PD7				Pulse Counter PCNT0 input number 1.
PCNT1_S0IN	PC4							Pulse Counter PCNT1 input number 0.
PCNT1_S1IN	PC5							Pulse Counter PCNT1 input number 1.
PCNT2_S0IN	PD0	PE8						Pulse Counter PCNT2 input number 0.
PCNT2_S1IN	PD1	PE9						Pulse Counter PCNT2 input number 1.
PRS_CH0	PA0	PF3						Peripheral Reflex System PRS, channel 0.
PRS_CH1	PA1	PF4						Peripheral Reflex System PRS, channel 1.
PRS_CH2	PC0	PF5						Peripheral Reflex System PRS, channel 2.
PRS_CH3	PC1	PE8						Peripheral Reflex System PRS, channel 3.
TIM0_CC0	PA0	PA0		PD1	PA0	PF0		Timer 0 Capture Compare input / output channel 0.
TIM0_CC1	PA1	PA1		PD2	PC0	PF1		Timer 0 Capture Compare input / output channel 1.
TIM0_CC2	PA2	PA2		PD3	PC1	PF2		Timer 0 Capture Compare input / output channel 2.
TIM0_CDTI0	PA3	PC13	PF3	PC13	PC2	PF3		Timer 0 Complimentary Deat Time Insertion channel 0.
TIM0_CDTI1	PA4	PC14	PF4	PC14	PC3	PF4		Timer 0 Complimentary Deat Time Insertion channel 1.
TIM0_CDTI2	PA5	PC15	PF5	PC15	PC4	PF5		Timer 0 Complimentary Deat Time Insertion channel 2.
TIM1_CC0	PC13	PE10		PB7	PD6			Timer 1 Capture Compare input / output channel 0.
TIM1_CC1	PC14	PE11		PB8	PD7			Timer 1 Capture Compare input / output channel 1.
TIM1_CC2	PC15	PE12		PB11	PC13			Timer 1 Capture Compare input / output channel 2.
TIM2_CC0	PA8		PC8					Timer 2 Capture Compare input / output channel 0.
TIM2_CC1	PA9		PC9					Timer 2 Capture Compare input / output channel 1.
TIM2_CC2	PA10		PC10					Timer 2 Capture Compare input / output channel 2.
TIM3_CC0	PE14							Timer 3 Capture Compare input / output channel 0.
TIM3_CC1	PE15							Timer 3 Capture Compare input / output channel 1.
TIM3_CC2	PA15							Timer 3 Capture Compare input / output channel 2.
US0_CLK	PE12		PC9	PC15	PB13	PB13		USART0 clock input / output.
US0_CS	PE13		PC8	PC14	PB14	PB14		USART0 chip select input / output.
								USART0 Asynchronous Receive.
US0_RX	PE11		PC10	PE12	PB8	PC1		USART0 Synchronous mode Master Input / Slave Output (MISO).
US0 TX	PE10		PC11	PE13	PB7	PC0		USART0 Asynchronous Transmit.Also used as receive input in half duplex communication.
								USART0 Synchronous mode Master Output / Slave Input (MOSI).



Figure 5.2. QFN64 PCB Solder Mask



|--|

Symbol	Dim. (mm)	Symbol	Dim. (mm)
а	0.97	е	8.90
b	0.42	f	7.32
С	0.50	g	7.32
d	8.90	-	-

Removed UART mentioned incorrectly in the QFN64 parts.

Updated Environmental information.

Updated trademark, disclaimer and contact information.

Other minor corrections.

7.4 Revision 1.20

June 28th, 2013

Updated power requirements in the Power Management section.

Removed minimum load capacitance figure and table. Added reference to application note.

Other minor corrections.

7.5 Revision 1.10

May 6th, 2013

Updated current consumption table and figures in Electrical characteristics section.

Other minor corrections.

7.6 Revision 1.00

September 11th, 2012

Updated the HFRCO 1 MHz band typical value to 1.2 MHz.

Updated the HFRCO 7 MHz band typical value to 6.6 MHz.

Other minor corrections.

7.7 Revision 0.95

May 3rd, 2012 Updated EM2/EM3 current consumption at 85°C.

7.8 Revision 0.90

February 27th, 2012

Initial preliminary release.



List of Equations

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