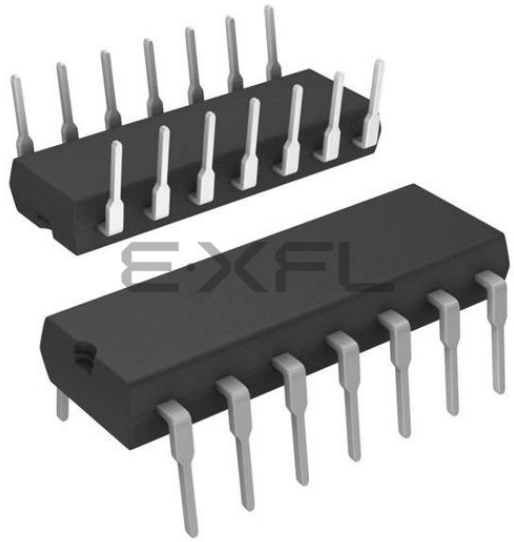


Welcome to E-XFL.COM

What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Through Hole
Package / Case	14-DIP (0.300", 7.62mm)
Supplier Device Package	14-DIP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc915fn-112

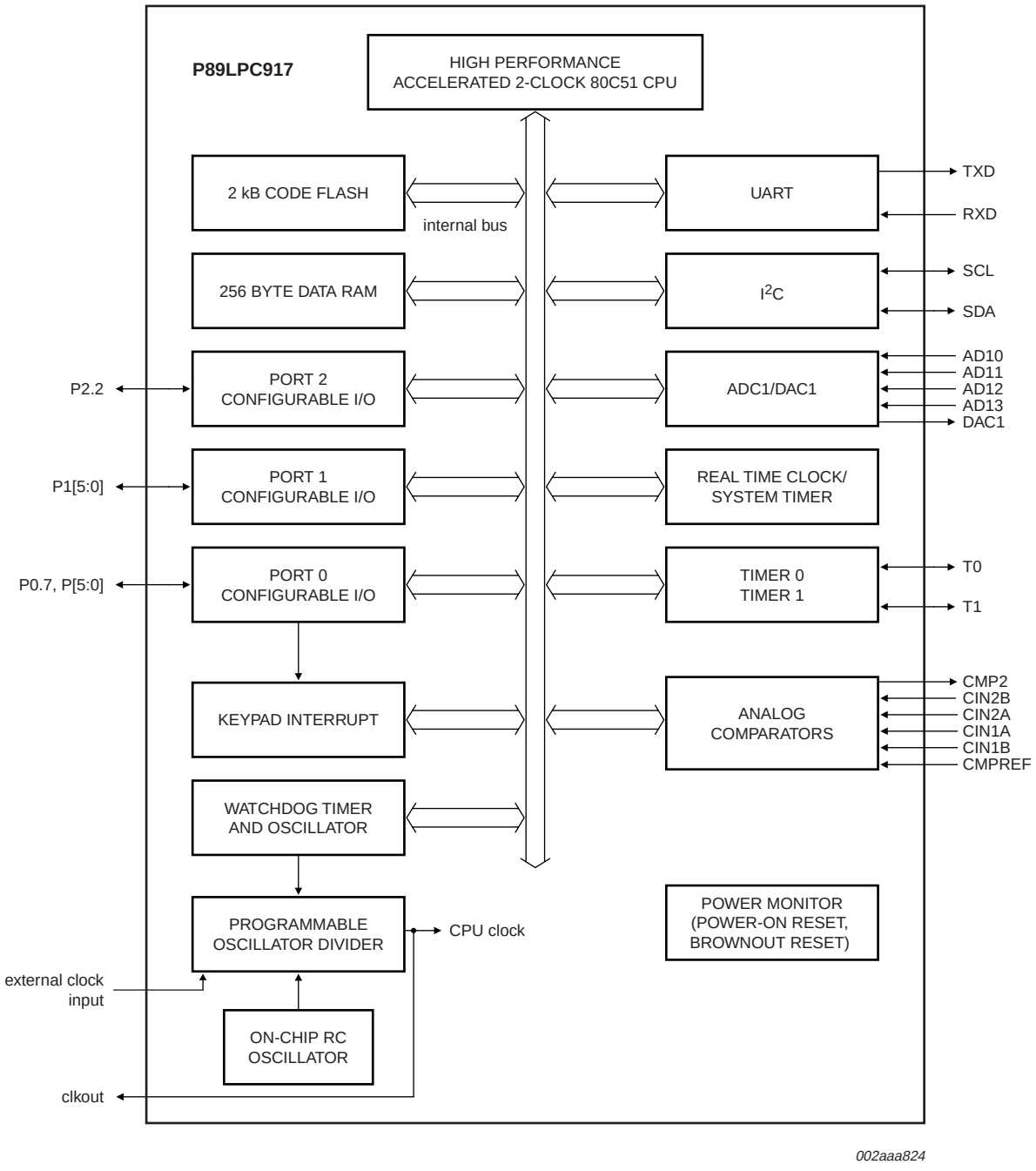


Fig 3. P89LPC917 block diagram

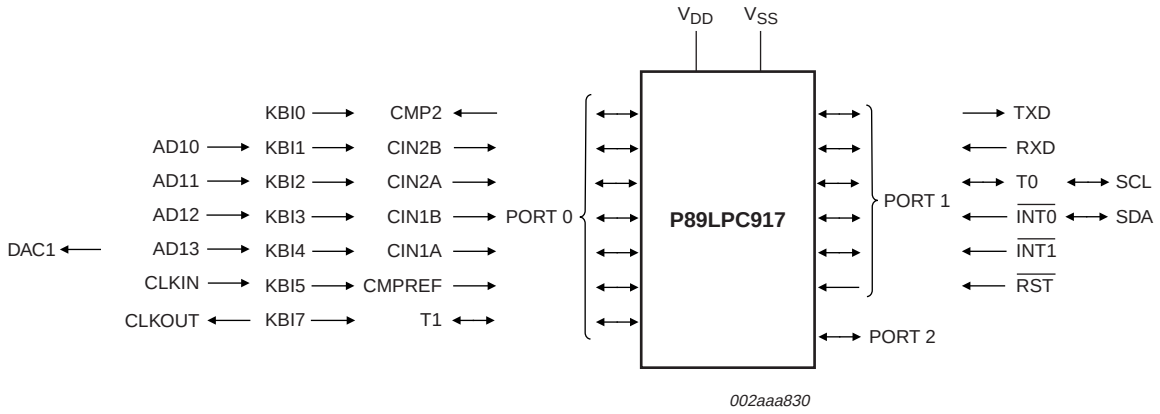


Fig 6. P89LPC917 functional diagram

7. Pinning information

7.1 Pinning

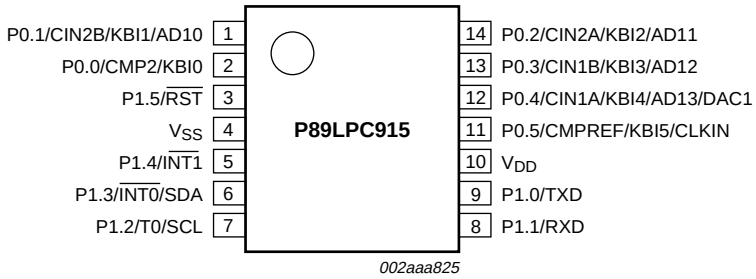


Fig 7. P89LPC915 TSSOP14 pin configuration

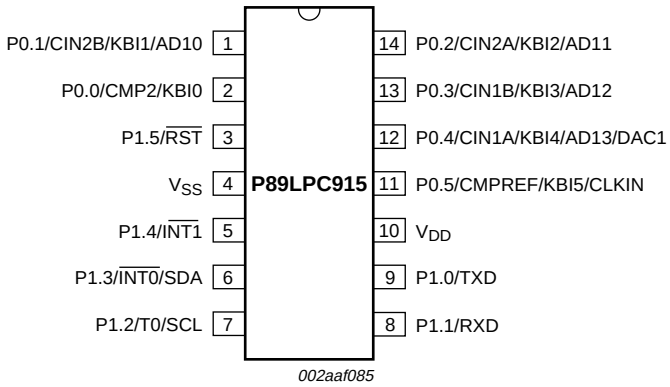


Fig 8. P89LPC915 DIP14 pin configuration

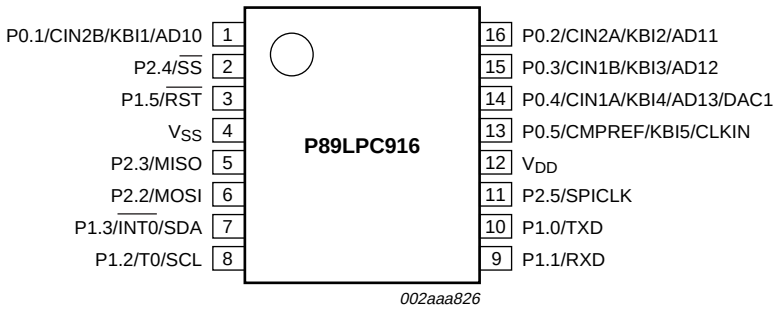


Fig 9. P89LPC916 TSSOP16 pin configuration

7.2 Pin description

Table 4. P89LPC915 pin description

Symbol	Pin	Type	Description
P0.0 to P0.5		I/O	**Port 0:** Port 0 is a 6-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/KBI0	2	I/O	**P0.0 —** Port 0 bit 0.
		O	**CMP2 —** Comparator 2 output.
		I	**KBI0 —** Keyboard input 0.
P0.1/CIN2B/KBI1/AD10	1	I/O	**P0.1 —** Port 0 bit 1.
		I	**CIN2B —** Comparator 2 positive input B.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/CIN2A/KBI2/AD11	14	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/KBI3/AD12	13	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input B.
		I	**KBI3 —** Keyboard input 3.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/KBI4/AD13/DAC1	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
		I	**AD13 —** ADC1 channel 3 analog input.
		I	**DAC1 —** DAC1 analog output.
P0.5/CMPREF/KBI5/CLKIN	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
		I	**CLKIN —** External clock input.
P1.0 to P1.5		I/O, I [1]	**Port 1:** Port 1 is a 6-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:

Table 4. P89LPC915 pin description *…continued*

Symbol	Pin	Type	Description
P1.0/TXD	9	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD	8	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
P1.2/T0/SCL	7	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C serial clock input/output.
P1.3/$\overline{INT0}$/SDA	6	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{INT0}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C serial data input/output.
P1.4/$\overline{INT1}$	5	I	**P1.4 —** Port 1 bit 4.
		I	**$\overline{INT1}$ —** External interrupt 1 input.
P1.5/$\overline{RST}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	10	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4. Input for P1.5.

Table 5. P89LPC916 pin description

Symbol	Pin	Type	Description
P0.0 to P0.5		I/O	**Port 0:** Port 0 is an 6-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:

Table 6. P89LPC917 pin description *…continued*

Symbol	Pin	Type	Description
P0.7/T1/KBI7/CLKOUT	11	I/O	**P0.7 —** Port 0 bit 7.
		I/O	**T1 —** Timer/counter 1 external count input or overflow output.
		I	**KBI7 —** Keyboard input 7.
		O	**CLKOUT —** Clock output.
P1.0 to P1.5		I/O, I [1]	**Port 1:** Port 1 is a 6-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	10	I/O	**P1.0 —** Port 1 bit 0.
		O	**TXD —** Transmitter output for serial port.
P1.1/RXD	9	I/O	**P1.1 —** Port 1 bit 1.
		I	**RXD —** Receiver input for serial port.
P1.2/T0/SCL	8	I/O	**P1.2 —** Port 1 bit 2 (open-drain when used as output).
		I/O	**T0 —** Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL —** I^2C serial clock input/output.
P1.3/$\overline{INT0}$/SDA	7	I/O	**P1.3 —** Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{INT0}$ —** External interrupt 0 input.
		I/O	**SDA —** I^2C serial data input/output.
P1.4/$\overline{INT1}$	6	I	**P1.4 —** Port 1 bit 4.
		I	**$\overline{INT1}$ —** External interrupt 1 input.
P1.5/$\overline{RST}$	3	I	**P1.5 —** Port 1 bit 5 (input only).
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

8. Functional description

8.1 Special function registers

Remark: SFR accesses are restricted in the following ways:

- User must **not** attempt to access any SFR locations not defined.
- Accesses to any defined SFR locations must be strictly for the functions for the SFRs.
- SFR bits labeled '-', '0' or '1' can **only** be written and read as follows:
  - '-' Unless otherwise specified, **must** be written with '0', but can return any value when read (even if it was written with '0'). It is a reserved bit and may be used in future derivatives.
  - '0' **must** be written with '0', and will return a '0' when read.
  - '1' **must** be written with '1', and will return a '1' when read.

Table 7. P89LPC915 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	-	-	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[1]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD	TXD	[1]	
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P0M1	Port 0 output mode 1	84H	-	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	1111 1111
P0M2	Port 0 output mode 2	85H	-	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H	-	-	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	-	SPD	-	00[1]	0000 0000
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00
RTCH	RTC register high	D2H									00[6]	0000 0000
RTCL	RTC register low	D3H									00[6]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	-	-	-	-	T0M2	00	xxx0 xxx0

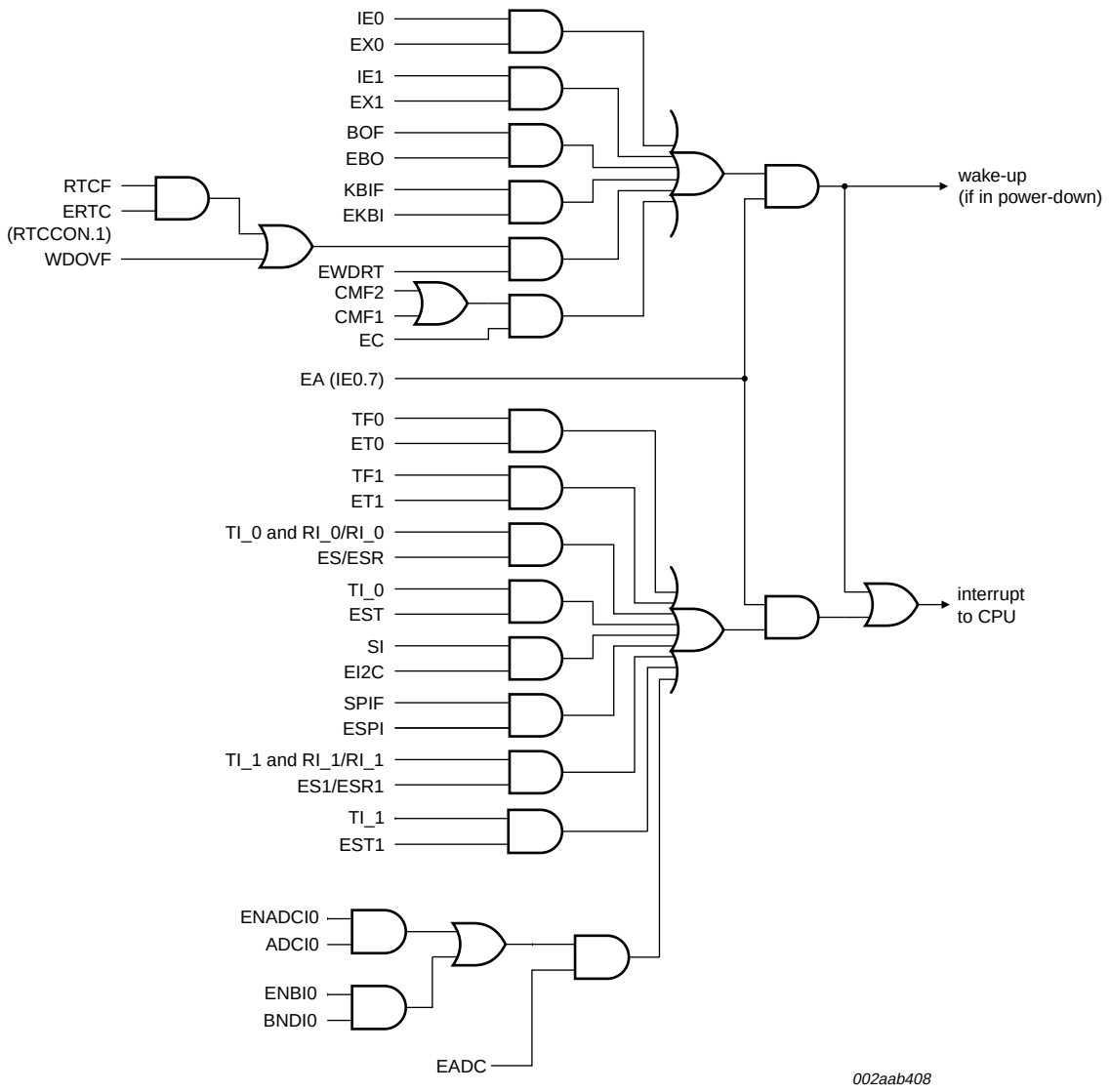


Fig 12. Interrupt sources, interrupt enables, and power-down wake-up sources

The P89LPC915/916/917 is a 3 V device, but the pins are 5 V tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

8.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.2 Port 0 analog functions

The P89LPC915/916/917 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, PT0AD bits default to ‘0’s to enable digital functions.

8.13.3 Additional port features

After power-up, all pins are in Input-Only mode. After power-up, all I/O pins except P1.5, may be configured by software.

- Pin P1.5 is input only.
- Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC915/916/917 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 15 “Static characteristics” for detailed specifications.

8.22 Analog comparators

Two analog comparators are provided on the P89LPC915/916/917. Input and output options allow use of the comparators in a number of different configurations. Comparator operation is such that the output is a logical one when the positive input is greater than the negative input (selectable from a pin or an internal reference voltage). Otherwise the output is a zero. Each comparator may be configured to cause an interrupt when the output value changes. Comparator 1 may be output to a port pin.

The overall connections to both comparators are shown in Figure 20. The comparators function to V_{DD} = 2.4 V.

When each comparator is first enabled, the comparator output and interrupt flag are not guaranteed to be stable for 10 microseconds. The corresponding comparator interrupt should not be enabled during that time, and the comparator interrupt flag must be cleared before the interrupt is enabled in order to prevent an immediate interrupt service.

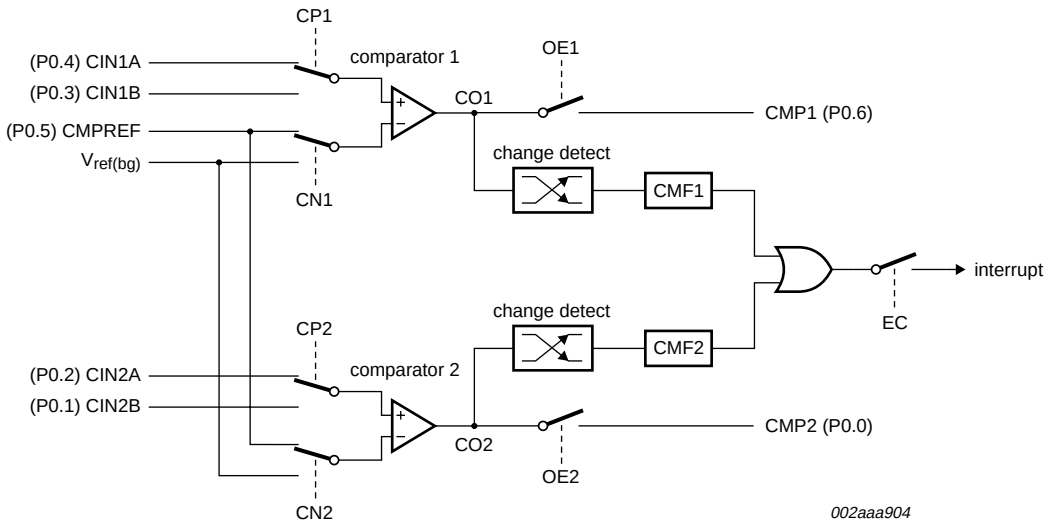


Fig 20. Comparator input and output connections

8.22.1 Internal reference voltage

An internal reference voltage generator may supply a default reference when a single comparator input pin is used. The value of the internal reference voltage, referred to as $V_{ref(bg)}$, is 1.23 V ± 10 %.

8.22.2 Comparator interrupt

Each comparator has an interrupt flag contained in its configuration register. This flag is set whenever the comparator output changes state. The flag may be polled by software or may be used to generate an interrupt. The two comparators use one common interrupt vector. If both comparators enable interrupts, after entering the interrupt service routine, the user needs to read the flags to determine which comparator caused the interrupt.

8.22.3 Comparators and power reduction modes

Either or both comparators may remain enabled when Power-down or Idle mode is activated, but both comparators are disabled automatically in Total Power-down mode.

If a comparator interrupt is enabled (except in Total Power-down mode), a change of the comparator output state will generate an interrupt and wake-up the processor. If the comparator output to a pin is enabled, the pin should be configured in the push-pull mode in order to obtain fast switching times while in Power-down mode. The reason is that with the **oscillator** stopped, the temporary strong pull-up that normally occurs during switching on a quasi-bidirectional port pin does not take place.

Comparators consume power in Power-down and Idle modes, as well as in the normal operating mode. This fact should be taken into account when system power consumption is an issue. To minimize power consumption, the user can disable the comparators via PCONA.5, or put the device in Total Power-down mode.

8.23 KBI

The Keypad Interrupt function is intended primarily to allow a single interrupt to be generated when Port 0 is equal to or not equal to a certain pattern. This function can be used for bus address recognition or keypad recognition. The user can configure the port via SFRs for different tasks.

The Keypad Interrupt Mask Register (KBMASK) is used to define which input pins connected to Port 0 can trigger the interrupt. The Keypad Pattern Register (KBPATN) is used to define a pattern that is compared to the value of Port 0. The Keypad Interrupt Flag (KBIF) in the Keypad Interrupt Control Register (KBCON) is set when the condition is matched while the Keypad Interrupt function is active. An interrupt will be generated if enabled. The PATN_SEL bit in the Keypad Interrupt Control Register (KBCON) is used to define equal or not-equal for the comparison.

In order to use the Keypad Interrupt as an original KBI function like in 87LPC76x series, the user needs to set KBPATN = 0FFH and PATN_SEL = 1 (not equal), then any key connected to Port 0 which is enabled by the KBMASK register will cause the hardware to set KBIF and generate an interrupt if it has been enabled. The interrupt may be used to wake-up the CPU from Idle or Power-down modes. This feature is particularly useful in handheld, battery-powered systems that need to carefully manage power consumption yet also need to be convenient to use.

In order to set the flag and cause an interrupt, the pattern on Port 0 must be held longer than six CCLKs.

8.26.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC915/916/917 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC915/916/917 *User's Manual*.

8.26.7 IAP-Lite

IAP-Lite is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The IAP-Lite operations are accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC915/916/917 *User's Manual*.

8.26.8 Power-on reset code execution

The P89LPC915/916/917 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC915/916/917 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 13 shows the factory default Boot Vector setting for this device. While these devices do not contain a factory bootloader, the Boot Vector and Status bit do provide a mechanism for an alternate code execution at reset.

Table 13. Default boot vector and Status bit values

Device	Default boot vector	Default Status bit
P89LPC915	00H	0
P89LPC916	00H	0
P89LPC917	00H	0

8.26.9 Hardware activation of the alternate code

The alternate code execution address can be forced during a power-on sequence (see the P89LPC915/916/917 *User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code starting at address 0000H but can be manually forced into executing from an alternated address using the Boot Vector. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

8.27 User configuration bytes

Some user-configurable features of the P89LPC915/916/917 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC915/916/917 *User's Manual* for additional details.

11. Static characteristics

Table 15. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C, or −40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	7	13	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	11	16	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.6	4.8	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	4	6	mA
$I_{DD(pd)}$	power supply current, power-down mode, voltage comparators powered-down	V_{DD} = 3.6 V, industrial	[2]	-	45	70	µA
		V_{DD} = 3.6 V, extended	[2]		-	150	µA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V, industrial	[3]	-	<0.1	5	µA
		V_{DD} = 3.6 V, extended	[3]	-	-	50	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.2	V
V_{DDR}	data retention voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		−0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; all ports except SCL, SDA	[4]	-	0.6	1.0	V
		I_{OL} = 10 mA; all ports except SCL, SDA		-	0.2	0.3	V
		I_{OL} = 3.2 mA; all ports except SCL, SDA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = −8 mA; push-pull mode; all ports except SCL, SDA		V_{DD} − 1	-	-	V
		I_{OH} = −3.2 mA; push-pull mode; all ports except SCL, SDA		V_{DD} − 0.7	V_{DD} − 0.4	-	V
		I_{OH} = −20 µA; quasi-bidirectional mode; all ports except SCL, SDA		V_{DD} − 0.3	V_{DD} − 0.2	-	V
V_{xtal}	crystal voltage	voltage on XTAL1, XTAL2 pins with respect to V_{SS}		−0.5	-	+4.0	V
V_n	voltage on any pin (except XTAL1, XTAL2, V_{DD})	with respect to V_{SS}	[5]	−0.5	-	+5.5	V
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	logical 0 input current	V_I = 0.4 V	[7]	-	-	−80	µA

Table 15. Static characteristics *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C, or −40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
I_{LI}	input leakage current	$V_I = V_{IL}$, V_{IH} or $V_{th(HL)}$	[8]	-	-	±10	µA
I_{TL}	logical 1-to-0 transition current, all ports	V_I = 1.5 V at V_{DD} = 3.6 V	[9]	−30	-	−450	µA
$R_{RST(int)}$	internal pull-up resistance on pin $\overline{RST}$			10	-	30	kΩ
V_{bo}	brownout trip voltage	2.4 V < V_{DD} < 3.6 V; with BOV = 1, BOPD = 0		2.40	-	2.70	V
$V_{ref(bg)}$	band gap reference voltage			1.11	1.23	1.34	V
TC_{bg}	band gap temperature coefficient			-	10	20	ppm/°C

[1] Typical ratings are not guaranteed. The values listed are at room temperature, 3 V.

[2] The $I_{DD(oper)}$, $I_{DD(idle)}$, and $I_{DD(pd)}$ specifications are measured using an external clock with the following functions disabled: comparators, real-time clock, and watchdog timer.

[3] The $I_{DD(tpd)}$ specification is measured using an external clock with the following functions disabled: comparators, real-time clock, brownout detect, and watchdog timer.

[4] See Section 10 “Limiting values” for steady state (non-transient) limits on I_{OL} or I_{OH}. If I_{OL}/I_{OH} exceeds the test condition, V_{OL}/V_{OH} may exceed the related specification.

[5] This specification can be applied to pins which have A/D input or analog comparator input functions when the pin is not being used for those analog functions. When the pin is being used as an analog input pin, the maximum voltage on the pin must be limited to 4.0 V with respect to V_{SS}.

[6] Pin capacitance is characterized but not tested.

[7] Measured with port in quasi-bidirectional mode.

[8] Measured with port in high-impedance mode.

[9] Port pins source a transition current when used in quasi-bidirectional mode and externally driven from logic 1 to logic 0. This current is highest when V_I is approximately 2 V.

Table 17. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C, or −40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	industrial	7.189	7.557	7.189	7.557	MHz
		extended	7.004	7.741	7.004	7.741	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{CLKLP}	low power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 28	55	-	-	-	ns
t_{CHCX}	clock HIGH time	see Figure 28	22	$T_{cy(CLK)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 28	22	$T_{cy(CLK)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 28	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 28	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 27	$16T_{cy(CLK)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 27	$13T_{cy(CLK)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 27	-	$T_{cy(CLK)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 27	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 27	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 23, 24, 25, 26					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 25, 26					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 25, 26	250	-	250	-	ns

Table 17. Dynamic characteristics (18 MHz) *…continued*

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.

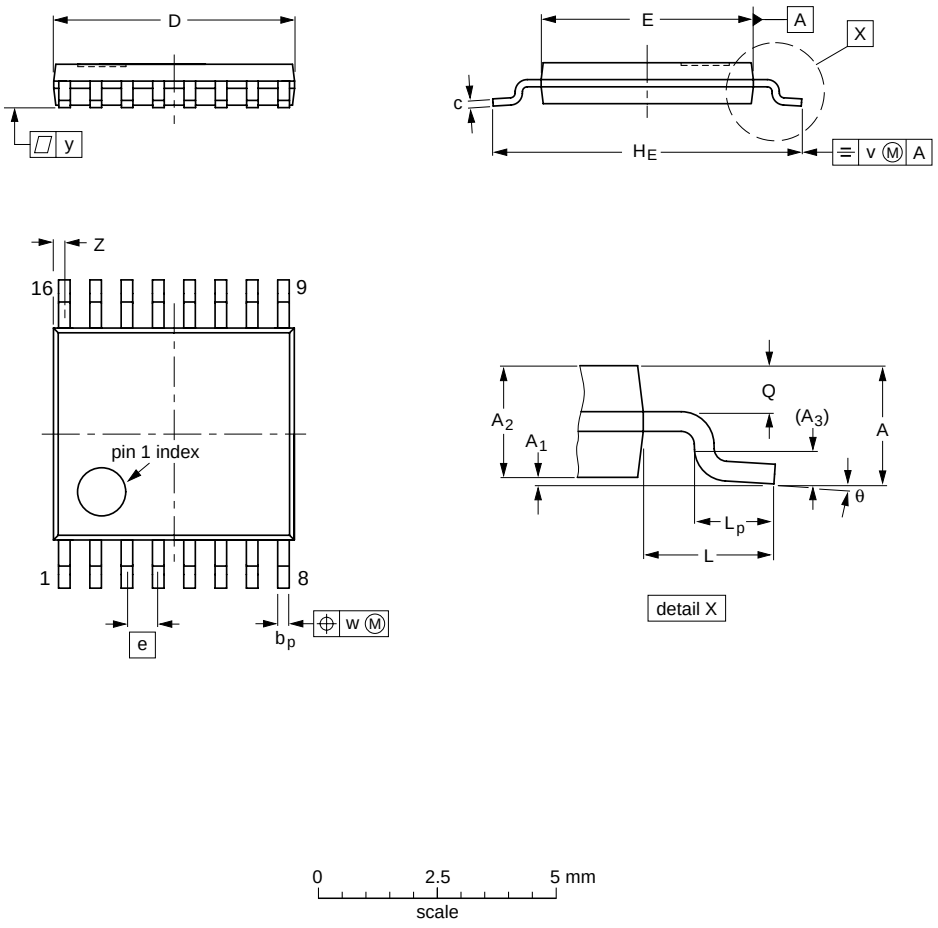
T_{amb} = −40 °C to +85 °C, or −40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 23, 24, 25, 26					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 23, 24, 25, 26					
	master		$^{2}/_{CCLK}$	-	111	-	ns
	slave		$^{3}/_{CCLK}$	-	167	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 23, 24, 25, 26					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 23, 24, 25, 26					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 25, 26					
	slave		0	80	0	80	ns
t_{SPIDIS}	SPI disable time	see Figure 25, 26					
	slave		0	160	-	160	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 23, 24, 25, 26					
	slave		-	160	-	160	ns
	master		-	111	-	111	ns
t_{SPIOH}	SPI output data hold time	see Figure 23, 24, 25, 26	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm **SOT403-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (2)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	1.1	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	5.1 4.9	4.5 4.3	0.65	6.6 6.2	1	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.40 0.06	8^o 0^o

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT403-1		MO-153				~~99-12-27~~ 03-02-18

Fig 32. Package outline SOT403-1 (TSSOP16)

17. Legal information

17.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

17.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. NXP Semiconductors does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local NXP Semiconductors sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

17.3 Disclaimers

General — Information in this document is believed to be accurate and reliable. However, NXP Semiconductors does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information.

Right to make changes — NXP Semiconductors reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

Suitability for use — NXP Semiconductors products are not designed, authorized or warranted to be suitable for use in medical, military, aircraft, space or life support equipment, nor in applications where failure or malfunction of an NXP Semiconductors product can reasonably be expected to result in personal injury, death or severe property or environmental damage. NXP Semiconductors accepts no liability for inclusion and/or use of NXP Semiconductors products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. NXP Semiconductors makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) may cause permanent damage to the device. Limiting values are stress ratings only and operation of the device at these or any other conditions above those given in the Characteristics sections of this document is not implied. Exposure to limiting values for extended periods may affect device reliability.

Terms and conditions of sale — NXP Semiconductors products are sold subject to the general terms and conditions of commercial sale, as published at http://www.nxp.com/profile/terms, including those pertaining to warranty, intellectual property rights infringement and limitation of liability, unless explicitly otherwise agreed to in writing by NXP Semiconductors. In case of any inconsistency or conflict between information in this document and such terms and conditions, the latter will prevail.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from national authorities.

17.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

I^2C-bus — logo is a trademark of NXP B.V.

18. Contact information

For more information, please visit: **http://www.nxp.com**

For sales office addresses, please send an email to: **salesaddresses@nxp.com**

9.4 A/D operating modes 54
9.4.1 Fixed channel, single conversion mode 54
9.4.2 Fixed channel, continuous conversion mode . 54
9.4.3 Auto scan, single conversion mode 54
9.4.4 Auto scan, continuous conversion mode 55
9.4.5 Dual channel, continuous conversion mode . . 55
9.4.6 Single step mode 55
9.5 Conversion start modes 55
9.5.1 Timer triggered start 55
9.5.2 Start immediately 55
9.5.3 Edge triggered 55
9.6 Boundary limits interrupt 55
9.7 DAC output to a port pin with high output impedance 56
9.8 Clock divider 56
9.9 Power-down and Idle mode 56
10 Limiting values 57
11 Static characteristics 58
12 Dynamic characteristics 60
12.1 Waveforms 64
12.2 ISP entry mode 66
13 Other characteristics 67
13.1 Comparator electrical characteristics 67
13.2 ADC electrical characteristics 67
14 Package outline 68
15 Abbreviations 71
16 Revision history 72
17 Legal information 73
17.1 Data sheet status 73
17.2 Definitions 73
17.3 Disclaimers 73
17.4 Trademarks 73
18 Contact information 73
19 Contents 74

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

Date of release: 15 December 2009
Document identifier: P89LPC915_916_917_5