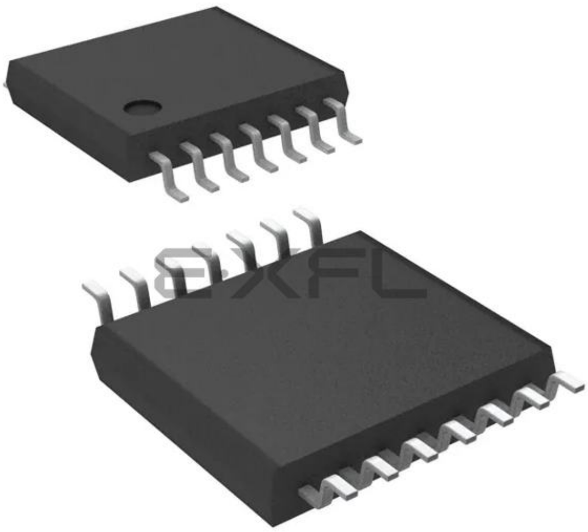

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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	12
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	14-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	14-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc915hdh-129

- Serial Flash In-Circuit Programming (ICP) allows simple production coding with commercial EPROM programmers. Flash security bits prevent reading of sensitive application programs.
- Watchdog timer with separate on-chip oscillator, requiring no external components. The Watchdog prescaler is selectable from 8 values.
- Low voltage brownout detect allows a graceful system shutdown when power fails. May optionally be configured as an interrupt.
- Idle and two different power-down reduced power modes. Improved wake-up from Power-down mode (a LOW interrupt input starts execution). Typical power-down current is 1 μA (total power-down with voltage comparators disabled).
- Active-LOW reset. On-chip power-on reset allows operation without external reset components. A reset counter and reset glitch suppression circuitry prevent spurious and incomplete resets. A software reset function is also available.
- Programmable port output configuration options: quasi-bidirectional, open drain, push-pull, input-only.
- Port 'input pattern match' detect. Port 0 may generate an interrupt when the value of the pins match or do not match a programmable pattern.
- LED drive capability (20 mA) on all port pins. A maximum limit is specified for the entire chip.
- Controlled slew rate port outputs to reduce EMI. Outputs have approximately 10 ns minimum ramp times.
- Only power and ground connections are required to operate the P89LPC915/916/917 when internal reset option is selected.
- Four interrupt priority levels.
- Five (P89LPC916), six (P89LPC915), or seven (P89LPC917) keypad interrupt inputs.
- Second data pointer.
- Schmitt trigger port inputs.
- Emulation support.

3. Product comparison overview

Table 1 highlights the differences between these three devices. For a complete list of device features, please see Section 2 "Features".

Table 1. Product comparison overview

Type number	Comparator 2 output	SPI	T1 toggle/PWM	CLKOUT	$\overline{INT1}$	KBI
P89LPC915	X	-	-	-	X	6
P89LPC916	-	X	-	-	-	5
P89LPC917	X	-	X	X	X	7

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC915FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC915FN	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
P89LPC915HDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC916FDH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
P89LPC917FDH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4.1 Ordering options

Table 3. Ordering options[1]

Type number	Temperature range	Frequency
P89LPC915FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC915FN		
P89LPC916FDH		
P89LPC917FDH		
P89LPC915HDH	–40 °C to +125 °C	

[1] Please contact your local NXP sales office for availability of extended temperature (–40 °C to +125 °C) versions of the P89LPC916 and P89LPC917 devices.

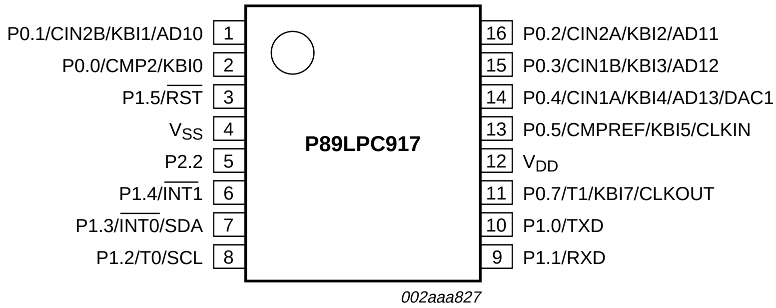

Fig 10. P89LPC917 TSSOP16 pin configuration

Table 6. P89LPC917 pin description

Symbol	Pin	Type	Description
P0.0 to P0.5, P0.7		I/O	**Port 0:** Port 0 is a 7-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 "Port configurations" and Table 15 "Static characteristics" for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/KBI0	2	I/O	**P0.0** — Port 0 bit 0.
		O	**CMP2** — Comparator 2 output.
		I	**KBI0** — Keyboard input 0.
P0.1/CIN2B/KBI1/AD10	1	I/O	**P0.1** — Port 0 bit 1.
		I	**CIN2B** — Comparator 2 positive input B.
		I	**KBI1** — Keyboard input 1.
		I	**AD10** — ADC1 channel 0 analog input.
P0.2/CIN2A/KBI2/AD11	16	I/O	**P0.2** — Port 0 bit 2.
		I	**CIN2A** — Comparator 2 positive input A.
		I	**KBI2** — Keyboard input 2.
		I	**AD11** — ADC1 channel 1 analog input.
P0.3/CIN1B/KBI3/AD12	15	I/O	**P0.3** — Port 0 bit 3.
		I	**CIN1B** — Comparator 1 positive input B.
		I	**KBI3** — Keyboard input 3.
		I	**AD12** — ADC1 channel 2 analog input.
P0.4/CIN1A/KBI4/AD13/DAC1	14	I/O	**P0.4** — Port 0 bit 4.
		I	**CIN1A** — Comparator 1 positive input A.
		I	**KBI4** — Keyboard input 4.
		I	**AD13** — ADC1 channel 3 analog input.
		O	**DAC1** — DAC1 analog output.
P0.5/CMPREF/KBI5	13	I/O	**P0.5** — Port 0 bit 5.
		I	**CMPREF** — Comparator reference (negative) input.
		I	**KBI5** — Keyboard input 5.
		I	**CLKIN** — External clock input.

Table 6. P89LPC917 pin description *…continued*

Symbol	Pin	Type	Description
P0.7/T1/KBI7/CLKOUT	11	I/O	**P0.7** — Port 0 bit 7.
		I/O	**T1** — Timer/counter 1 external count input or overflow output.
		I	**KBI7** — Keyboard input 7.
		O	**CLKOUT** — Clock output.
P1.0 to P1.5		I/O, I [1]	**Port 1:** Port 1 is a 6-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 "Port configurations" and Table 15 "Static characteristics" for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:
P1.0/TXD	10	I/O	**P1.0** — Port 1 bit 0.
		O	**TXD** — Transmitter output for serial port.
P1.1/RXD	9	I/O	**P1.1** — Port 1 bit 1.
		I	**RXD** — Receiver input for serial port.
P1.2/T0/SCL	8	I/O	**P1.2** — Port 1 bit 2 (open-drain when used as output).
		I/O	**T0** — Timer/counter 0 external count input or overflow output (open-drain when used as output).
		I/O	**SCL** — I^2C serial clock input/output.
P1.3/$\overline{\text{INT0}}$/SDA	7	I/O	**P1.3** — Port 1 bit 3 (open-drain when used as output).
		I	**$\overline{\text{INT0}}$** — External interrupt 0 input.
		I/O	**SDA** — I^2C serial data input/output.
P1.4/$\overline{\text{INT1}}$	6	I	**P1.4** — Port 1 bit 4.
		I	**$\overline{\text{INT1}}$** — External interrupt 1 input.
P1.5/$\overline{\text{RST}}$	3	I	**P1.5** — Port 1 bit 5 (input only).
		I	**$\overline{\text{RST}}$** — External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**

Table 7. P89LPC915 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD. 7	FMCMD. 6	FMCMD. 5	FMCMD. 4	FMCMD. 3	FMCMD. 2	FMCMD. 1	FMCMD. 0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^{2}C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I^{2}C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^{2}C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^{2}C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	EX1	ET0	EX0	00	0000 0000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	-	EC	EKBI	EI2C	00[1]	00x0 0000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	PX1	PT0	PX0	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRT H	PBOH	PSH/ PSRH	PT1H	PX1H	PT0H	PX0H	00[1]	x000 0000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	-	PC	PKBI	PI2C	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	-	PCH	PKBIH	PI2CH	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN _SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register										FF	1111 1111

Table 8. P89LPC916 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON1	ADC control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	ADC input select	A3H	ADI13	ADI12	ADI11	ADI10	-	-	-	-	00	0000 0000
ADMODA	ADC mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	ADC mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1	-	00	000x 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	ENT0	SRST	0	-	DPS	00	0000 00x0
		Bit address	F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0	Baud rate generator rate low	BEH									00	0000 0000
BRGR1	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000

Table 8. P89LPC916 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I²C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
		Bit address	DF	DE	DD	DC	DB	DA	D9	D8		
I2CON*	I²C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I²C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I²C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
		Bit address	AF	AE	AD	AC	AB	AA	A9	A8		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	EX0	00	0000 0000
		Bit address	EF	EE	ED	EC	EB	EA	E9	E8		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	ESPI	EC	EKBI	EI2C	00[1]	00x0 0000
		Bit address	BF	BE	BD	BC	BB	BA	B9	B8		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	PX0	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	PX0H	00[1]	x000 0000
		Bit address	FF	FE	FD	FC	FB	FA	F9	F8		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	PSPI	PC	PKBI	PI2C	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register										FF	1111 1111

8.6 External clock input option

In this configuration, the processor clock is derived from an external source driving the CLKIN pin. The rate may be from 0 Hz up to 18 MHz.

When using an external clock input frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an external clock input frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.

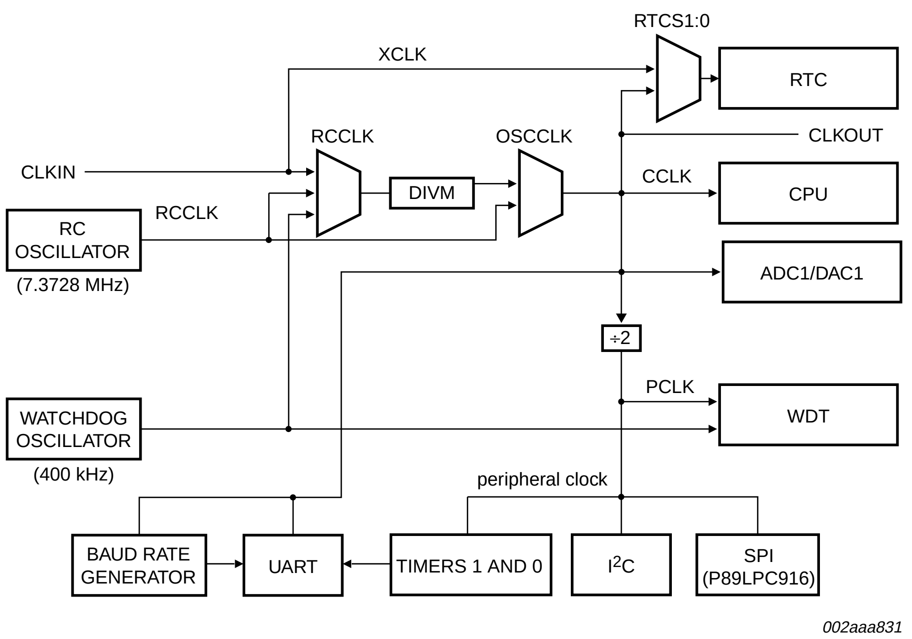

Fig 11. Block diagram of oscillator control

8.7 CCLK wake-up delay

The P89LPC915/916/917 has an internal wake-up timer that delays the clock until it stabilizes. The delay is 224 OSCCLK cycles plus 60 μs to 100 μs.

8.8 CCLK modification: DIVM register

The OSCCLK frequency can be divided down up to 510 times by configuring a dividing register, DIVM, to generate CCLK. This feature makes it possible to temporarily run the CPU at a lower rate, reducing power consumption. By dividing the clock, the CPU can retain the ability to respond to events that would not exit Idle mode by executing its normal program at a lower rate. This can also allow bypassing the oscillator start-up time in cases where Power-down mode would otherwise be used. The value of DIVM may be changed by the program at any time without interrupting code execution.

8.26.6 ICP

ICP is performed without removing the microcontroller from the system. The ICP facility consists of internal hardware resources to facilitate remote programming of the P89LPC915/916/917 through a two-wire serial interface. The NXP ICP facility has made in-circuit programming in an embedded application—using commercially available programmers—possible with a minimum of additional expense in components and circuit board area. The ICP function uses five pins. Only a small connector needs to be available to interface your application to a commercial programmer in order to use this feature. Additional details may be found in the P89LPC915/916/917 *User's Manual*.

8.26.7 IAP-Lite

IAP-Lite is performed in the application under the control of the microcontroller's firmware. The IAP facility consists of internal hardware resources to facilitate programming and erasing. The IAP-Lite operations are accomplished through the use of four SFRs consisting of a control/status register, a data register, and two address registers. Additional details may be found in the P89LPC915/916/917 *User's Manual*.

8.26.8 Power-on reset code execution

The P89LPC915/916/917 contains two special flash elements: the Boot Vector and the Boot Status bit. Following reset, the P89LPC915/916/917 examines the contents of the Boot Status bit. If the Boot Status bit is set to zero, power-up execution starts at location 0000H, which is the normal start address of the user's application code. When the Boot Status bit is set to a value other than zero, the contents of the Boot Vector are used as the high byte of the execution address and the low byte is set to 00H.

Table 13 shows the factory default Boot Vector setting for this device. While these devices do not contain a factory bootloader, the Boot Vector and Status bit do provide a mechanism for an alternate code execution at reset.

Table 13. Default boot vector and Status bit values

Device	Default boot vector	Default Status bit
P89LPC915	00H	0
P89LPC916	00H	0
P89LPC917	00H	0

8.26.9 Hardware activation of the alternate code

The alternate code execution address can be forced during a power-on sequence (see the P89LPC915/916/917 *User's Manual* for specific information). This has the same effect as having a non-zero status byte. This allows an application to be built that will normally execute user code starting at address 0000H but can be manually forced into executing from an alternated address using the Boot Vector. After programming the flash, the status byte should be programmed to zero in order to allow execution of the user's application code beginning at address 0000H.

8.27 User configuration bytes

Some user-configurable features of the P89LPC915/916/917 must be defined at power-up and therefore cannot be set by the program after start of execution. These features are configured through the use of the flash byte UCFG1. Please see the P89LPC915/916/917 *User's Manual* for additional details.

8.28 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC915/916/917. Each byte corresponds to one sector. Please see the P89LPC915/916/917 *User's Manual* for additional details.

9. A/D converter

9.1 General description

The P89LPC915/916/917 devices have a single 8-bit, 4-channel multiplexed analog-to-digital converter with a DAC module. A block diagram of the A/D converter is shown in Figure 22. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

9.2 Features

- Single 8-bit, 4-channel multiplexed input, successive approximation A/D converter.
- Four A/D result registers.
- Six operating modes:
  - Fixed channel, single conversion mode.
  - Fixed channel, continuous conversion mode.
  - Auto scan, single conversion mode.
  - Auto scan, continuous conversion mode.
  - Dual channel, continuous conversion mode.
  - Single step mode.
- Three conversion start modes:
  - Timer triggered start.
  - Start immediately.
  - Edge triggered.
- 8-bit conversion time of ≥3.9 μs at an A/D clock of 3.3 MHz.
- Interrupt or polled operation.
- Boundary limits interrupt.
- DAC output to a port pin with high output impedance.
- Clock divider.
- Power-down mode.

9.3 Block diagram

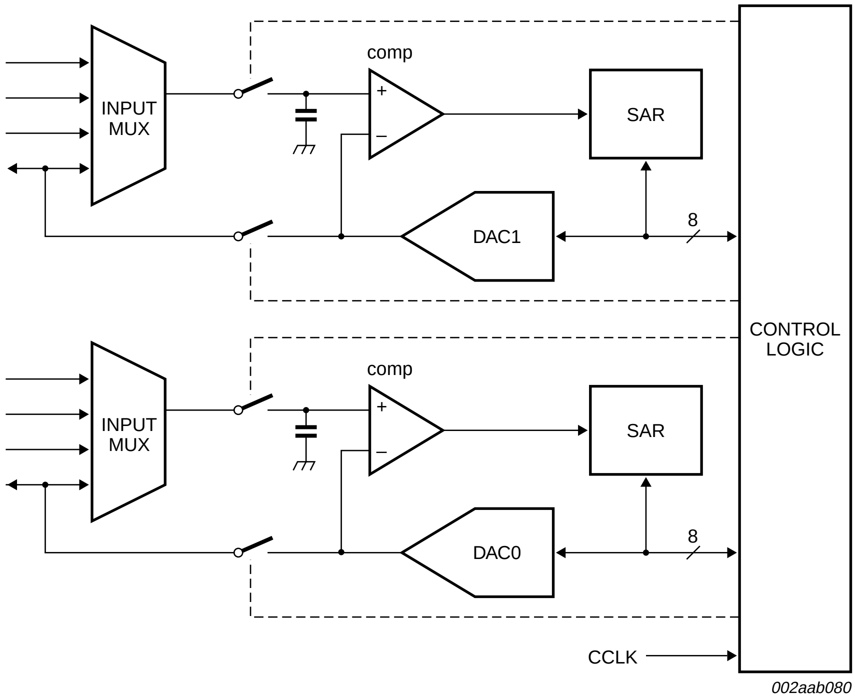

Fig 22. ADC block diagram

9.4 A/D operating modes

9.4.1 Fixed channel, single conversion mode

A single input channel can be selected for conversion. A single conversion will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after the conversion completes.

9.4.2 Fixed channel, continuous conversion mode

A single input channel can be selected for continuous conversion. The results of the conversions will be sequentially placed in the four result registers. An interrupt, if enabled, will be generated after every four conversions. Additional conversion results will again cycle through the four result registers, overwriting the previous results. Continuous conversions continue until terminated by the user.

9.4.3 Auto scan, single conversion mode

Any combination of the four input channels can be selected for conversion. A single conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. If only a single channel is selected this is equivalent to single channel, single conversion mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results.Continous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The first channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion.This start mode is available in all A/D operating modes.

9.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

9.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

11. Static characteristics

Table 15. Static characteristics

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.
T_{amb} = –40 °C to +85 °C, or –40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.

Symbol	Parameter	Conditions		Min	Typ[1]	Max	Unit
$I_{DD(oper)}$	operating supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	7	13	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	11	16	mA
$I_{DD(idle)}$	Idle mode supply current	V_{DD} = 3.6 V; f_{osc} = 12 MHz	[2]	-	3.6	4.8	mA
		V_{DD} = 3.6 V; f_{osc} = 18 MHz	[2]	-	4	6	mA
$I_{DD(pd)}$	power supply current, power-down mode, voltage comparators powered-down	V_{DD} = 3.6 V, industrial	[2]	-	45	70	µA
		V_{DD} = 3.6 V, extended	[2]		-	150	µA
$I_{DD(tpd)}$	total Power-down mode supply current	V_{DD} = 3.6 V, industrial	[3]	-	<0.1	5	µA
		V_{DD} = 3.6 V, extended	[3]	-	-	50	µA
$(dV/dt)_r$	rise rate	of V_{DD}		-	-	2	mV/µs
$(dV/dt)_f$	fall rate	of V_{DD}		-	-	50	mV/µs
V_{POR}	power-on reset voltage			-	-	0.2	V
V_{DDR}	data retention voltage			1.5	-	-	V
$V_{th(HL)}$	HIGH-LOW threshold voltage	except SCL, SDA		$0.22V_{DD}$	$0.4V_{DD}$	-	V
V_{IL}	LOW-level input voltage	SCL, SDA only		–0.5	-	$0.3V_{DD}$	V
$V_{th(LH)}$	LOW-HIGH threshold voltage	except SCL, SDA		-	$0.6V_{DD}$	$0.7V_{DD}$	V
V_{IH}	HIGH-level input voltage	SCL, SDA only		$0.7V_{DD}$	-	5.5	V
V_{hys}	hysteresis voltage	port 1		-	$0.2V_{DD}$	-	V
V_{OL}	LOW-level output voltage	I_{OL} = 20 mA; all ports except SCL, SDA	[4]	-	0.6	1.0	V
		I_{OL} = 10 mA; all ports except SCL, SDA		-	0.2	0.3	V
		I_{OL} = 3.2 mA; all ports except SCL, SDA		-	0.2	0.3	V
V_{OH}	HIGH-level output voltage	I_{OH} = –8 mA; push-pull mode; all ports except SCL, SDA		V_{DD} – 1	-	-	V
		I_{OH} = –3.2 mA; push-pull mode; all ports except SCL, SDA		V_{DD} – 0.7	V_{DD} – 0.4	-	V
		I_{OH} = –20 µA; quasi-bidirectional mode; all ports except SCL, SDA		V_{DD} – 0.3	V_{DD} – 0.2	-	V
V_{xtal}	crystal voltage	voltage on XTAL1, XTAL2 pins with respect to V_{SS}		–0.5	-	+4.0	V
V_n	voltage on any pin (except XTAL1, XTAL2, V_{DD})	with respect to V_{SS}	[5]	–0.5	-	+5.5	V
C_{iss}	input capacitance		[6]	-	-	15	pF
I_{IL}	logical 0 input current	V_I = 0.4 V	[7]	-	-	–80	µA

Table 16. Dynamic characteristics (12 MHz) *…continued*

V_{DD} = 2.4 V to 3.6 V unless otherwise specified.

T_{amb} = –40 °C to +85 °C, or –40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 12 MHz		Unit
			Min	Max	Min	Max	
$t_{SPILEAD}$	SPI enable lead time	see Figure 25, 26					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 25, 26					
	slave		250	-	250	-	ns
$t_{SPICLKH}$	SPICLK HIGH time	see Figure 23, 24, 25, 26					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
$t_{SPICLKL}$	SPICLK LOW time	see Figure 23, 24, 25, 26					
	master		$^{2}/_{CCLK}$	-	165	-	ns
	slave		$^{3}/_{CCLK}$	-	250	-	ns
t_{SPIDSU}	SPI data set-up time	see Figure 23, 24, 25, 26					
	master or slave		100	-	100	-	ns
t_{SPIDH}	SPI data hold time	see Figure 23, 24, 25, 26					
	master or slave		100	-	100	-	ns
t_{SPIA}	SPI access time	see Figure 25, 26					
	slave		0	120	0	120	ns
t_{SPIDIS}	SPI disable time	see Figure 25, 26					
	slave		0	240	-	240	ns
t_{SPIDV}	SPI enable to output data valid time	see Figure 23, 24, 25, 26					
	slave		-	240	-	240	ns
	master		-	167	-	167	ns
t_{SPIOH}	SPI output data hold time	see Figure 23, 24, 25, 26	0	-	0	-	ns
t_{SPIR}	SPI rise time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns
t_{SPIF}	SPI fall time	see Figure 23, 24, 25, 26					
	SPI outputs (SPICLK, MOSI, MISO)		-	100	-	100	ns
	SPI inputs (SPICLK, MOSI, MISO, $\overline{SS}$)		-	2000	-	2000	ns

[1] Parameters are valid over ambient temperature range unless otherwise specified.

[2] Parts are tested to 2 MHz, but are guaranteed to operate down to 0 Hz.

12.1 Waveforms

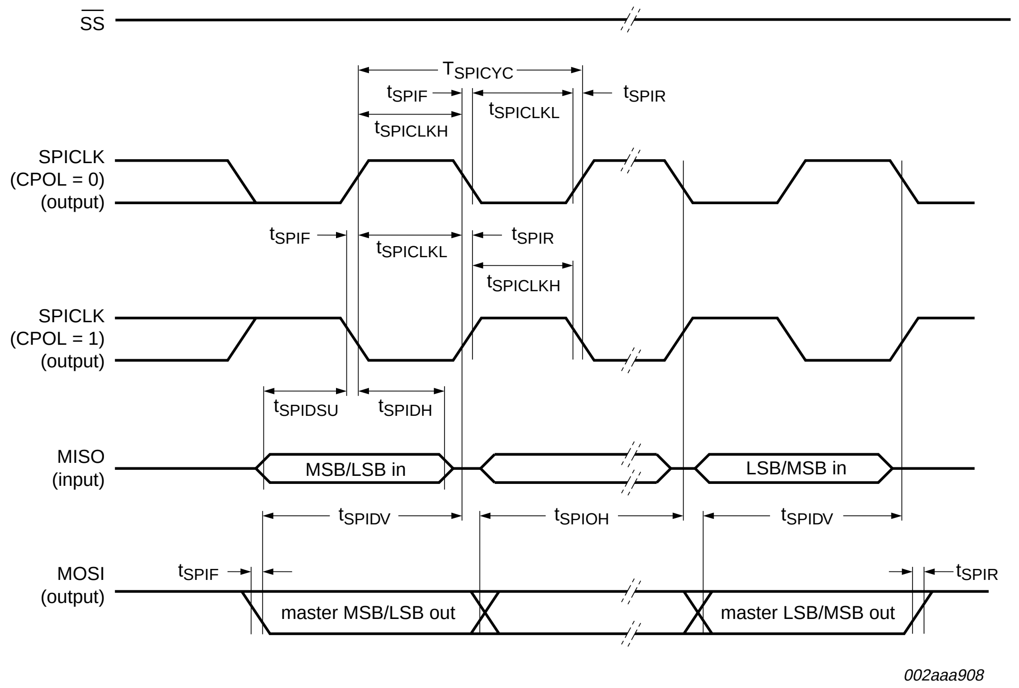

Fig 23. SPI master timing (CPHA = 0)

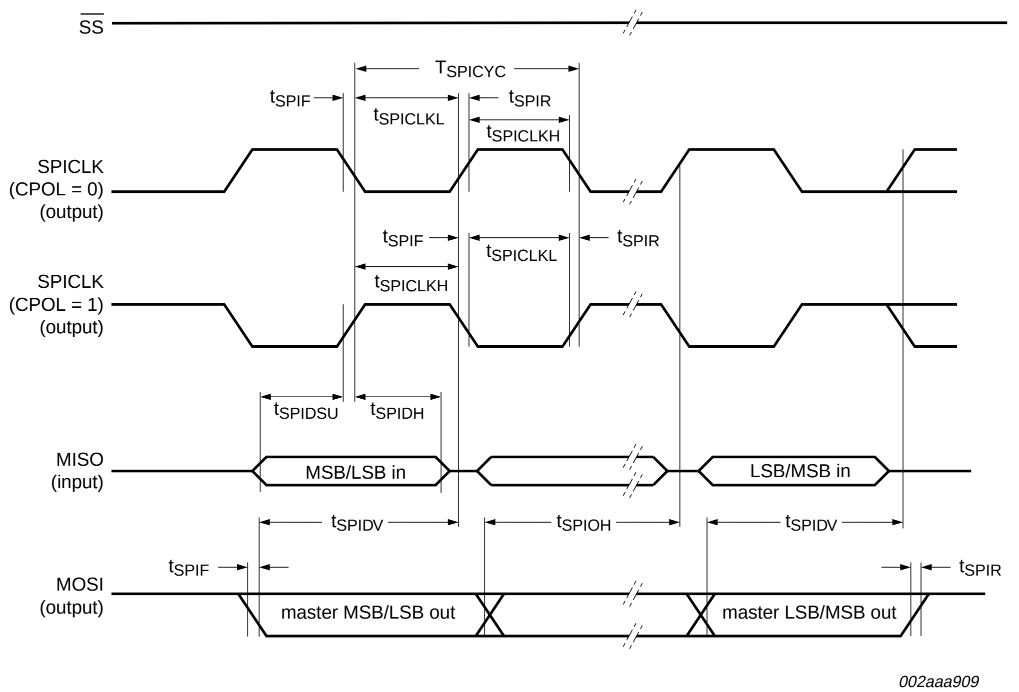

Fig 24. SPI master timing (CPHA = 1)

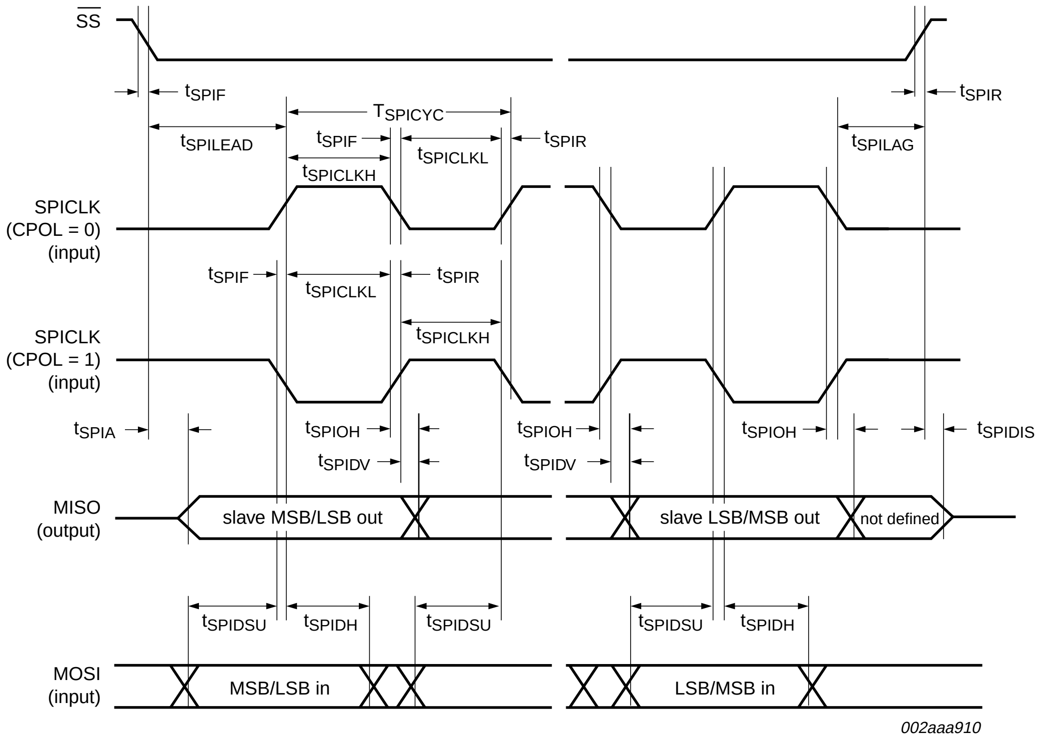

Fig 25. SPI slave timing (CPHA = 0)

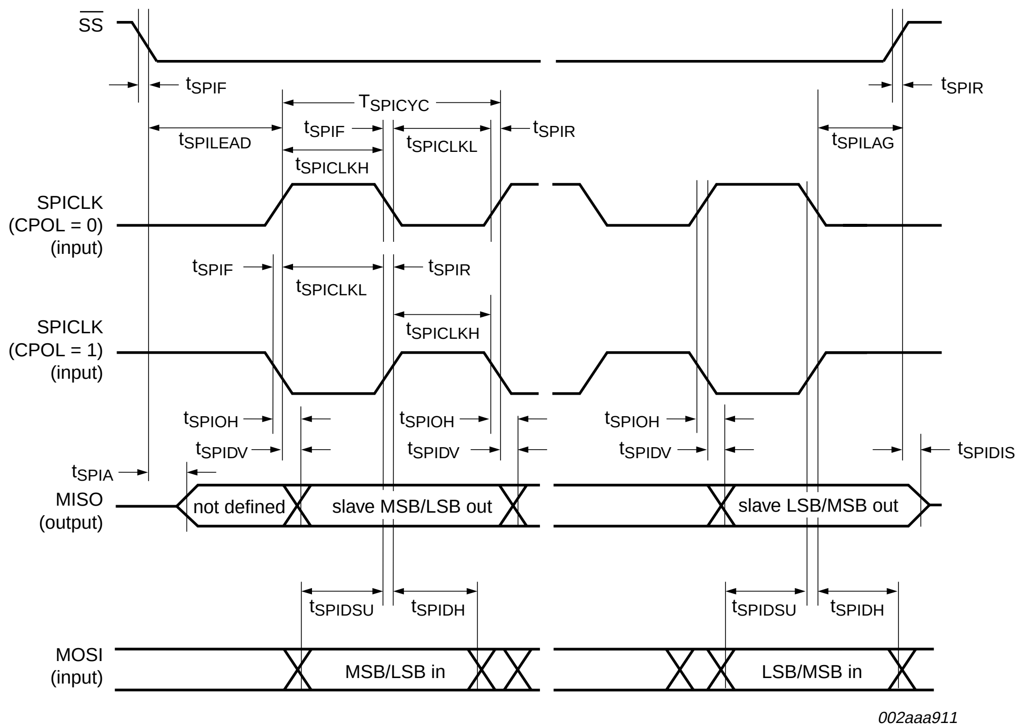

Fig 26. SPI slave timing (CPHA = 1)

15. Abbreviations

Table 21. Acronym list

Acronym	Description
ADC	Analog to Digital Converter
CPU	Central Processing Unit
CCU	Capture/Compare Unit
DAC	Digital to Analog Converter
EPROM	Erasable Programmable Read-Only Memory
EEPROM	Electrically Erasable Programmable Read-Only Memory
EMI	ElectroMagnetic Interference
PLL	Phase-Locked Loop
PWM	Pulse Width Modulator
RAM	Random Access Memory
RC	Resistance-Capacitance
RTC	Real-Time Clock
SAR	Successive Approximation Register
SFR	Special Function Register
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter

16. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC915_916_917_5	20091215	Product data sheet	-	P89LPC915_916_917-04
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added ADC electrical characteristics, Table 20. • Added P89LPC915FN.			
P89LPC915_916_917-04	20041217	Product data	-	P89LPC915_916_917-03
P89LPC915_916_917-03	20040701	Preliminary data	-	P89LPC915_916_917-02
P89LPC915_916_917-02	20040512	Preliminary data	-	P89LPC915_916_917-01
P89LPC915_916_917-01	20040408	Preliminary data	-	-

19. Contents

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