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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	8051
Core Size	8-Bit
Speed	18MHz
Connectivity	I²C, SPI, UART/USART
Peripherals	Brown-out Detect/Reset, LED, POR, PWM, WDT
Number of I/O	14
Program Memory Size	2KB (2K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	256 x 8
Voltage - Supply (Vcc/Vdd)	2.4V ~ 3.6V
Data Converters	A/D 4x8b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	16-TSSOP (0.173", 4.40mm Width)
Supplier Device Package	16-TSSOP
Purchase URL	https://www.e-xfl.com/product-detail/nxp-semiconductors/p89lpc916fdh-129

4. Ordering information

Table 2. Ordering information

Type number	Package		
	Name	Description	Version
P89LPC915FDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC915FN	DIP14	plastic dual in-line package; 14 leads (300 mil)	SOT27-1
P89LPC915HDH	TSSOP14	plastic thin shrink small outline package; 14 leads; body width 4.4 mm	SOT402-1
P89LPC916FDH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
P89LPC917FDH	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4.1 Ordering options

Table 3. Ordering options[1]

Type number	Temperature range	Frequency
P89LPC915FDH	–40 °C to +85 °C	0 MHz to 18 MHz
P89LPC915FN		
P89LPC916FDH		
P89LPC917FDH		
P89LPC915HDH	–40 °C to +125 °C	

[1] Please contact your local NXP sales office for availability of extended temperature (–40 °C to +125 °C) versions of the P89LPC916 and P89LPC917 devices.

6. Functional diagram

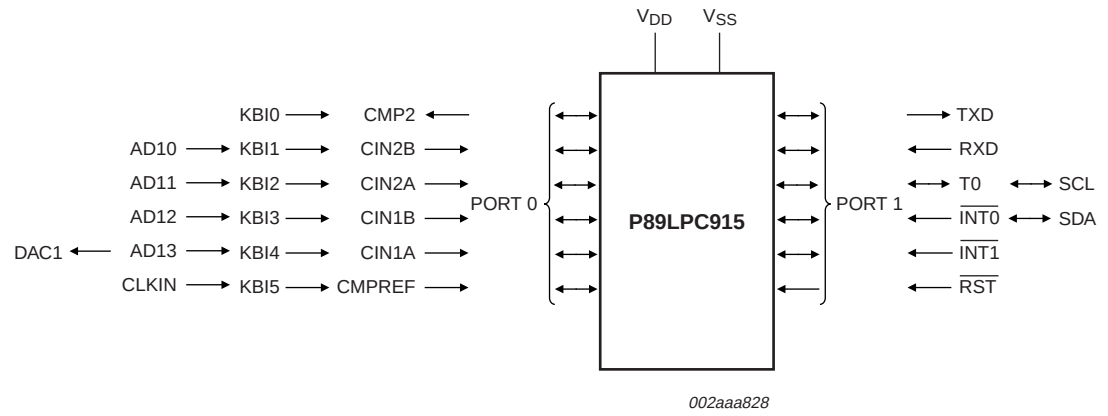

Fig 4. P89LPC915 functional diagram

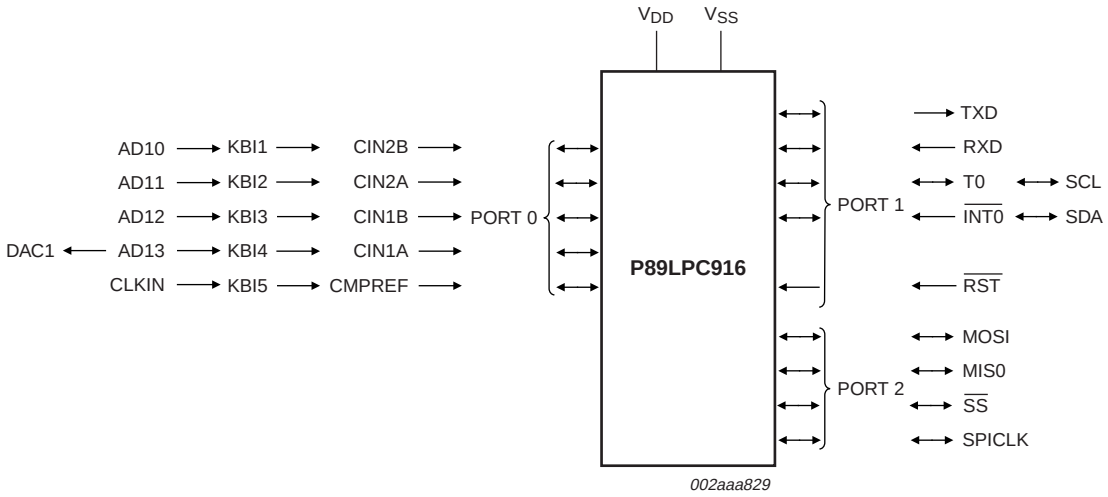

Fig 5. P89LPC916 functional diagram

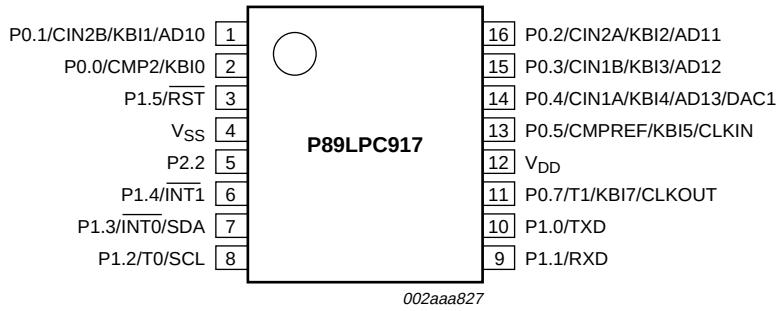

Fig 10. P89LPC917 TSSOP16 pin configuration

7.2 Pin description

Table 4. P89LPC915 pin description

Symbol	Pin	Type	Description
P0.0 to P0.5		I/O	**Port 0:** Port 0 is a 6-bit I/O port with a user-configurable output type. During reset Port 0 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 0 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. The Keypad Interrupt feature operates with Port 0 pins. All pins have Schmitt triggered inputs. Port 0 also provides various special functions as described below:
P0.0/CMP2/KBI0	2	I/O	**P0.0 —** Port 0 bit 0.
		O	**CMP2 —** Comparator 2 output.
		I	**KBI0 —** Keyboard input 0.
P0.1/CIN2B/KBI1/AD10	1	I/O	**P0.1 —** Port 0 bit 1.
		I	**CIN2B —** Comparator 2 positive input B.
		I	**KBI1 —** Keyboard input 1.
		I	**AD10 —** ADC1 channel 0 analog input.
P0.2/CIN2A/KBI2/AD11	14	I/O	**P0.2 —** Port 0 bit 2.
		I	**CIN2A —** Comparator 2 positive input A.
		I	**KBI2 —** Keyboard input 2.
		I	**AD11 —** ADC1 channel 1 analog input.
P0.3/CIN1B/KBI3/AD12	13	I/O	**P0.3 —** Port 0 bit 3.
		I	**CIN1B —** Comparator 1 positive input B.
		I	**KBI3 —** Keyboard input 3.
		I	**AD12 —** ADC1 channel 2 analog input.
P0.4/CIN1A/KBI4/AD13/DAC1	12	I/O	**P0.4 —** Port 0 bit 4.
		I	**CIN1A —** Comparator 1 positive input A.
		I	**KBI4 —** Keyboard input 4.
		I	**AD13 —** ADC1 channel 3 analog input.
		I	**DAC1 —** DAC1 analog output.
P0.5/CMPREF/KBI5/CLKIN	11	I/O	**P0.5 —** Port 0 bit 5.
		I	**CMPREF —** Comparator reference (negative) input.
		I	**KBI5 —** Keyboard input 5.
		I	**CLKIN —** External clock input.
P1.0 to P1.5		I/O, I [1]	**Port 1:** Port 1 is a 6-bit I/O port with a user-configurable output type, except for three pins as noted below. During reset Port 1 latches are configured in the input only mode with the internal pull-up disabled. The operation of the configurable Port 1 pins as inputs and outputs depends upon the port configuration selected. Each of the configurable port pins are programmed independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. P1.2 to P1.3 are open drain when used as outputs. P1.5 is input only. All pins have Schmitt triggered inputs. Port 1 also provides various special functions as described below:

Table 5. P89LPC916 pin description *…continued*

Symbol	Pin	Type	Description
		I	**$\overline{RST}$ —** External Reset input during power-on or if selected via UCFG1. When functioning as a reset input, a LOW on this pin resets the microcontroller, causing I/O ports and peripherals to take on their default states, and the processor begins execution at address 0. Also used during a power-on sequence to force ISP mode. **When using an oscillator frequency above 12 MHz, the reset input function of P1.5 must be enabled. An external circuit is required to hold the device in reset at power-up until V_{DD} has reached its specified level. When system power is removed V_{DD} will fall below the minimum specified operating voltage. When using an oscillator frequency above 12 MHz, in some applications, an external brownout detect circuit may be required to hold the device in reset when V_{DD} falls below the minimum specified operating voltage.**
P2.2 to P2.5			**Port 2:** Port 2 is a 4-bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of Port 2 pins as inputs and outputs depends upon the port configuration selected. Each port pin is configured independently. Refer to Section 8.13.1 “Port configurations” and Table 15 “Static characteristics” for details. All pins have Schmitt triggered inputs. Port 2 also provides various special functions as described below:
P2.2/MOSI	6	I/O	**P2.2 —** Port 2 bit 2.
		I/O	**MOSI —** SPI master out slave in. When configured as master, this pin is output; when configured as slave, this pin is input.
P2.3/MISO	5	I/O	**P2.3 —** Port 2 bit 3.
		I/O	**MISO —** When configured as master, this pin is input, when configured as slave, this pin is output.
P2.4/$\overline{SS}$	2	I/O	**P2.4 —** Port 2 bit 4.
		I/O	**$\overline{SS}$ —** SPI Slave select.
P2.5/SPICLK	11	I/O	**P2.5 —** Port 2 bit 5.
		I/O	**SPICLK —** SPI clock. When configured as master, this pin is output; when configured as slave, this pin is input.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	12	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.3. Input for P1.5.

Table 6. P89LPC917 pin description *...continued*

Symbol	Pin	Type	Description
P2.2	5		**Port 2:** Port 2 is a single bit I/O port with a user-configurable output type. During reset Port 2 latches are configured in the input only mode with the internal pull-up disabled. The operation of this Port 2 pin as an input and output depends upon the port configuration selected. Refer to Section 8.13.1 "Port configurations" and Table 15 "Static characteristics" for details. This pin has a Schmitt triggered input.
V_{SS}	4	I	**Ground:** 0 V reference.
V_{DD}	12	I	**Power supply:** This is the power supply voltage for normal operation as well as Idle and Power-down modes.

[1] Input/output for P1.0 to P1.4. Input for P1.5.

Table 8. P89LPC916 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON1	ADC control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	ADC input select	A3H	ADI13	ADI12	ADI11	ADI10	-	-	-	-	00	0000 0000
ADMODA	ADC mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	ADC mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1	-	00	000x 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	-	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0	Baud rate generator rate low	BEH									00	0000 0000
BRGR1	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000

Table 8. P89LPC916 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
FMCON	Program flash control (Read)	E4H	BUSY	-	-	-	HVA	HVE	SV	OI	70	0111 0000
	Program flash control (Write)	E4H	FMCMD.7	FMCMD.6	FMCMD.5	FMCMD.4	FMCMD.3	FMCMD.2	FMCMD.1	FMCMD.0		
FMDATA	Program flash data	E5H									00	0000 0000
I2ADR	I^2C slave address register	DBH	I2ADR.6	I2ADR.5	I2ADR.4	I2ADR.3	I2ADR.2	I2ADR.1	I2ADR.0	GC	00	0000 0000
	Bit address		**DF**	**DE**	**DD**	**DC**	**DB**	**DA**	**D9**	**D8**		
I2CON*	I^2C control register	D8H	-	I2EN	STA	STO	SI	AA	-	CRSEL	00	x000 00x0
I2DAT	I^2C data register	DAH										
I2SCLH	Serial clock generator/SCL duty cycle register high	DDH									00	0000 0000
I2SCLL	Serial clock generator/SCL duty cycle register low	DCH									00	0000 0000
I2STAT	I^2C status register	D9H	STA.4	STA.3	STA.2	STA.1	STA.0	0	0	0	F8	1111 1000
	Bit address		**AF**	**AE**	**AD**	**AC**	**AB**	**AA**	**A9**	**A8**		
IEN0*	Interrupt enable 0	A8H	EA	EWDRT	EBO	ES/ESR	ET1	-	ET0	EX0	00	0000 0000
	Bit address		**EF**	**EE**	**ED**	**EC**	**EB**	**EA**	**E9**	**E8**		
IEN1*	Interrupt enable 1	E8H	EAD	EST	-	-	ESPI	EC	EKBI	EI2C	00[1]	00x0 0000
	Bit address		**BF**	**BE**	**BD**	**BC**	**BB**	**BA**	**B9**	**B8**		
IP0*	Interrupt priority 0	B8H	-	PWDRT	PBO	PS/PSR	PT1	-	PT0	PX0	00[1]	x000 0000
IP0H	Interrupt priority 0 high	B7H	-	PWDRTH	PBOH	PSH/PSRH	PT1H	-	PT0H	PX0H	00[1]	x000 0000
	Bit address		**FF**	**FE**	**FD**	**FC**	**FB**	**FA**	**F9**	**F8**		
IP1*	Interrupt priority 1	F8H	PAD	PST	-	-	PSPI	PC	PKBI	PI2C	00[1]	00x0 0000
IP1H	Interrupt priority 1 high	F7H	PADH	PSTH	-	-	PSPIH	PCH	PKBIH	PI2CH	00[1]	00x0 0000
KBCON	Keypad control register	94H	-	-	-	-	-	-	PATN_SEL	KBIF	00[1]	xxxx xx00
KBMASK	Keypad interrupt mask register	86H									00	0000 0000
KBPATN	Keypad pattern register										FF	1111 1111

Table 9. P89LPC917 special function registers

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
	Bit address		E7	E6	E5	E4	E3	E2	E1	E0		
ACC*	Accumulator	E0H									00	0000 0000
ADCON1	ADC control register 1	97H	ENBI1	ENADCI 1	TMM1	EDGE1	ADCI1	ENADC1	ADCS11	ADCS10	00	0000 0000
ADINS	ADC input select	A3H	ADI13	ADI12	ADI11	ADI10	-	-	-	-	00	0000 0000
ADMODA	ADC mode register A	C0H	BNDI1	BURST1	SCC1	SCAN1	-	-	-	-	00	0000 0000
ADMODB	ADC mode register B	A1H	CLK2	CLK1	CLK0	-	ENDAC1	-	BSA1	-	00	000x 0000
AD1BH	A/D_1 boundary high register	C4H									FF	1111 1111
AD1BL	A/D_1 boundary low register	BCH									00	0000 0000
AD1DAT0	A/D_1 data register 0	D5H									00	0000 0000
AD1DAT1	A/D_1 data register 1	D6H									00	0000 0000
AD1DAT2	A/D_1 data register 2	D7H									00	0000 0000
AD1DAT3	A/D_1 data register 3	F5H									00	0000 0000
AUXR1	Auxiliary function register	A2H	CLKLP	EBRR	ENT1	ENT0	SRST	0	-	DPS	00	0000 00x0
	Bit address		F7	F6	F5	F4	F3	F2	F1	F0		
B*	B register	F0H									00	0000 0000
BRGR0	Baud rate generator rate low	BEH									00	0000 0000
BRGR1	Baud rate generator rate high	BFH									00	0000 0000
BRGCON	Baud rate generator control	BDH	-	-	-	-	-	-	SBRGS	BRGEN	00[2]	xxxx xx00
CMP1	Comparator 1 control register	ACH	-	-	CE1	CP1	CN1	-	CO1	CMF1	00[1]	xx00 0000
CMP2	Comparator 2 control register	ADH	-	-	CE2	CP2	CN2	OE2	CO2	CMF2	00[1]	xx00 0000
DIVM	CPU clock divide-by-M control	95H									00	0000 0000
DPTR	Data pointer (2 bytes)											
DPH	Data pointer high	83H									00	0000 0000
DPL	Data pointer low	82H									00	0000 0000
FMADRH	Program flash address high	E7H									00	0000 0000
FMADRL	Program flash address low	E6H									00	0000 0000

Table 9. P89LPC917 special function registers *…continued*

** indicates SFRs that are bit addressable.*

Name	Description	SFR addr.	Bit functions and addresses								Reset value	
			MSB							LSB	Hex	Binary
		Bit address	**87**	**86**	**85**	**84**	**83**	**82**	**81**	**80**		
P0*	Port 0	80H	T1/KB7/ CLKOUT	-	CMPREF /KB5	CIN1A /KB4	CIN1B /KB3	CIN2A /KB2	CIN2B /KB1	CMP2 /KB0	[1]	
		Bit address	**97**	**96**	**95**	**94**	**93**	**92**	**91**	**90**		
P1*	Port 1	90H	-	-	$\overline{\text{RST}}$	$\overline{\text{INT1}}$	$\overline{\text{INT0}}$/ SDA	T0/SCL	RXD	TXD	[1]	
		Bit address	**B7**	**B6**	**B5**	**B4**	**B3**	**B2**	**B1**	**B0**		
P0M1	Port 0 output mode 1	84H	(P0M1.7)	-	(P0M1.5)	(P0M1.4)	(P0M1.3)	(P0M1.2)	(P0M1.1)	(P0M1.0)	FF[1]	1111 1111
P0M2	Port 0 output mode 2	85H	(P0M2.7)	-	(P0M2.5)	(P0M2.4)	(P0M2.3)	(P0M2.2)	(P0M2.1)	(P0M2.0)	00[1]	0000 0000
P1M1	Port 1 output mode 1	91H	-	-	-	(P1M1.4)	(P1M1.3)	(P1M1.2)	(P1M1.1)	(P1M1.0)	D3[1]	11x1 xx11
P1M2	Port 1 output mode 2	92H	-	-	-	(P1M2.4)	(P1M2.3)	(P1M2.2)	(P1M2.1)	(P1M2.0)	00[1]	00x0 xx00
PCON	Power control register	87H	SMOD1	SMOD0	BOPD	BOI	GF1	GF0	PMOD1	PMOD0	00	0000 0000
PCONA	Power control register A	B5H	RTCPD	-	VCPD	ADPD	I2PD	-	SPD	-	00[1]	0000 0000
		Bit address	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**		
PSW*	Program status word	D0H	CY	AC	F0	RS1	RS0	OV	F1	P	00	0000 0000
PT0AD	Port 0 digital input disable	F6H	-	-	PT0AD.5	PT0AD.4	PT0AD.3	PT0AD.2	PT0AD.1	-	00	xx00 000x
RSTSRC	Reset source register	DFH	-	-	BOF	POF	R_BK	R_WD	R_SF	R_EX	[3]	
RTCCON	RTC control	D1H	RTCF	RTCS1	RTCS0	-	-	-	ERTC	RTCEN	60[1][6]	011x xx00
RTCH	RTC register high	D2H									00[6]	0000 0000
RTCL	RTC register low	D3H									00[6]	0000 0000
SADDR	Serial port address register	A9H									00	0000 0000
SADEN	Serial port address enable	B9H									00	0000 0000
SBUF	Serial Port data buffer register	99H									xx	xxxx xxxx
		Bit address	**9F**	**9E**	**9D**	**9C**	**9B**	**9A**	**99**	**98**		
SCON*	Serial port control	98H	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI	00	0000 0000
SSTAT	Serial port extended status register	BAH	DBMOD	INTLO	CIDIS	DBISEL	FE	BR	OE	STINT	00	0000 0000
SP	Stack pointer	81H									07	0000 0111
TAMOD	Timer 0 and 1 auxiliary mode	8FH	-	-	-	T1M2	-	-	-	T0M2	00	xxx0 xxx0

The P89LPC915/916/917 is a 3 V device, but the pins are 5 V tolerant. In quasi-bidirectional mode, if a user applies 5 V on the pin, there will be a current flowing from the pin to V_{DD}, causing extra power consumption. Therefore, applying 5 V in quasi-bidirectional mode is discouraged.

A quasi-bidirectional port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.1.2 Open-drain output configuration

The open-drain output configuration turns off all pull-ups and only drives the pull-down transistor of the port driver when the port latch contains a logic 0. To be used as a logic output, a port configured in this manner must have an external pull-up, typically a resistor tied to V_{DD}.

An open-drain port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.1.3 Input-only configuration

The input-only port configuration has no output drivers. It is a Schmitt triggered input that also has a glitch suppression circuit.

8.13.1.4 Push-pull output configuration

The push-pull output configuration has the same pull-down structure as both the open-drain and the quasi-bidirectional output modes, but provides a continuous strong pull-up when the port latch contains a logic 1. The push-pull mode may be used when more source current is needed from a port output. A push-pull port pin has a Schmitt triggered input that also has a glitch suppression circuit.

8.13.2 Port 0 analog functions

The P89LPC915/916/917 incorporates two Analog Comparators. In order to give the best analog function performance and to minimize power consumption, pins that are being used for analog functions must have the digital outputs and digital inputs disabled.

Digital outputs are disabled by putting the port output into the Input-Only (high-impedance) mode.

Digital inputs on Port 0 may be disabled through the use of the PT0AD register. On any reset, PT0AD bits default to ‘0’s to enable digital functions.

8.13.3 Additional port features

After power-up, all pins are in Input-Only mode. After power-up, all I/O pins except P1.5, may be configured by software.

- Pin P1.5 is input only.
- Pins P1.2 and P1.3 are configurable for either input-only or open-drain.

Every output on the P89LPC915/916/917 has been designed to sink typical LED drive current. However, there is a maximum total output current for all ports which must not be exceeded. Please refer to Table 15 “Static characteristics” for detailed specifications.

In the ‘Timer’ function, the register is incremented every machine cycle.

In the ‘Counter’ function, the register is incremented in response to a 1-to-0 transition at its corresponding external input pin, T0 or T1. In this function, the external input is sampled once during every machine cycle.

Timer 0 has five operating modes (Modes 0, 1, 2, 3 and 6).

Timer 1 has four operating modes (Modes 0, 1, 2, and 3), except on the P89LPC917 where Timer 1 also has Mode 6. Modes 0, 1, 2 and 6 are the same for both Timers/Counters. Mode 3 is different.

8.17.1 Mode 0

Putting either Timer into Mode 0 makes it look like an 8048 Timer, which is an 8-bit Counter with a divide-by-32 prescaler. In this mode, the Timer register is configured as a 13-bit register. Mode 0 operation is the same for Timer 0 and Timer 1.

8.17.2 Mode 1

Mode 1 is the same as Mode 0, except that all 16 bits of the timer register are used.

8.17.3 Mode 2

Mode 2 configures the Timer register as an 8-bit Counter with automatic reload. Mode 2 operation is the same for Timer 0 and Timer 1.

8.17.4 Mode 3

When Timer 1 is in Mode 3 it is stopped. Timer 0 in Mode 3 forms two separate 8-bit counters and is provided for applications that require an extra 8-bit timer. When Timer 1 is in Mode 3 it can still be used by the serial port as a baud rate generator.

8.17.5 Mode 6

In this mode, the corresponding timer can be changed to a PWM with a full period of 256 timer clocks.

8.17.6 Timer overflow toggle output

Timer 0 (and Timer 1 on the P89LPC917) can be configured to automatically toggle a port output whenever a timer overflow occurs. The same device pins that are used for the T0 and T1 count inputs are also used for the timer toggle outputs. The port outputs will be a logic 1 prior to the first timer overflow when this mode is turned on.

8.18 RTC/system timer

The P89LPC915/916/917 have a simple RTC that allows a user to continue running an accurate timer while the rest of the device is powered down. The RTC can be a wake-up or an interrupt source. The RTC is a 23-bit down-counter comprised of a 7-bit prescaler and a 16-bit loadable down-counter. When it reaches all ‘0’s, the counter will be reloaded again and the RTCF flag will be set.

8.21 SPI

The P89LPC916 provides another high-speed serial communication interface—the SPI interface. SPI is a full-duplex, high-speed, synchronous communication bus with two operation modes: Master mode and Slave mode. Up to 4.5 Mbit/s can be supported in Master mode or up to 3 Mbit/s in Slave mode. It has a Transfer Completion Flag and Write Collision Flag Protection.

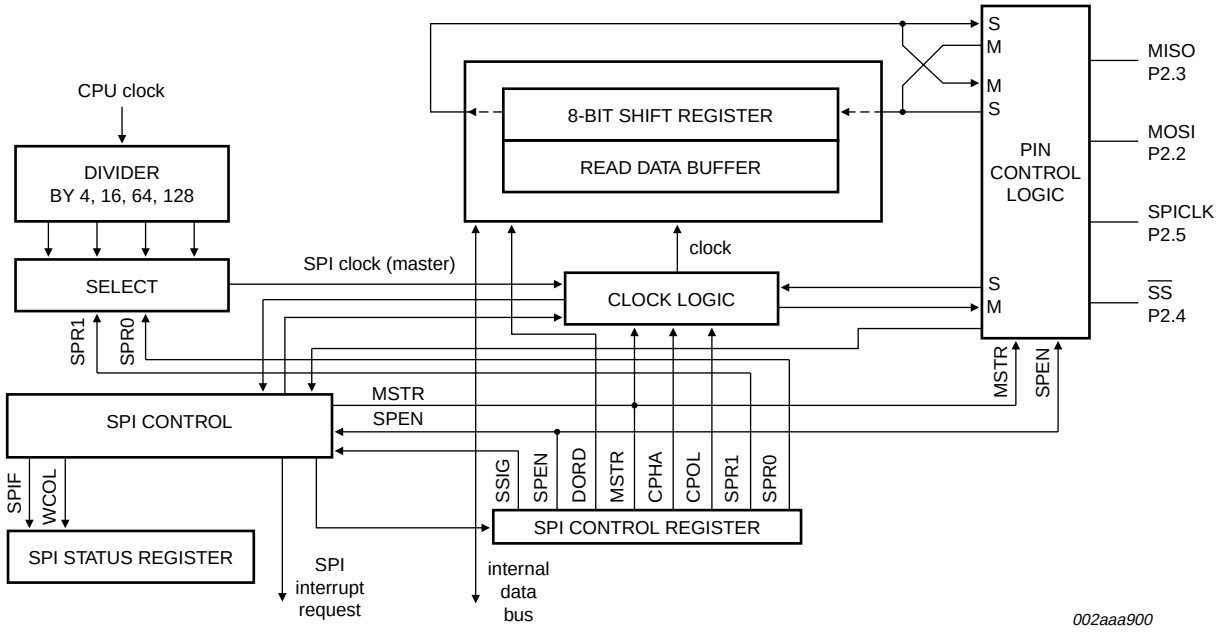

Fig 16. SPI block diagram

The SPI interface has four pins: SPICLK, MOSI, MISO and $\overline{SS}$:

- SPICLK, MOSI and MISO are typically tied together between two or more SPI devices. Data flows from master to slave on MOSI (Master Out Slave In) pin and flows from slave to master on MISO (Master In Slave Out) pin. The SPICLK signal is output in the master mode and is input in the slave mode. If the SPI system is disabled, i.e., SPEN (SPCTL.6) = 0 (reset value), these pins are configured for port functions.
- $\overline{SS}$ is the optional slave select pin. In a typical configuration, an SPI master asserts one of its port pins to select one SPI device as the current slave. An SPI slave device uses its $\overline{SS}$ pin to determine whether it is selected.

Typical connections are shown in Figure 17 through Figure 19.

8.28 User sector security bytes

There are eight User Sector Security Bytes on the P89LPC915/916/917. Each byte corresponds to one sector. Please see the P89LPC915/916/917 *User's Manual* for additional details.

9. A/D converter

9.1 General description

The P89LPC915/916/917 devices have a single 8-bit, 4-channel multiplexed analog-to-digital converter with a DAC module. A block diagram of the A/D converter is shown in Figure 22. The A/D consists of a 4-input multiplexer which feeds a sample-and-hold circuit providing an input signal to one of two comparator inputs. The control logic in combination with the SAR drives a digital-to-analog converter which provides the other input to the comparator. The output of the comparator is fed to the SAR.

9.2 Features

- Single 8-bit, 4-channel multiplexed input, successive approximation A/D converter.
- Four A/D result registers.
- Six operating modes:
  - Fixed channel, single conversion mode.
  - Fixed channel, continuous conversion mode.
  - Auto scan, single conversion mode.
  - Auto scan, continuous conversion mode.
  - Dual channel, continuous conversion mode.
  - Single step mode.
- Three conversion start modes:
  - Timer triggered start.
  - Start immediately.
  - Edge triggered.
- 8-bit conversion time of ≥3.9 μs at an A/D clock of 3.3 MHz.
- Interrupt or polled operation.
- Boundary limits interrupt.
- DAC output to a port pin with high output impedance.
- Clock divider.
- Power-down mode.

9.4.4 Auto scan, continuous conversion mode

Any combination of the four input channels can be selected for conversion. A conversion of each selected input will be performed and the result placed in the result register which corresponds to the selected input channel. An interrupt, if enabled, will be generated after all selected channels have been converted. The process will repeat starting with the first selected channel. Additional conversion results will again cycle through the four result registers, overwriting the previous results.Continous conversions continue until terminated by the user.

9.4.5 Dual channel, continuous conversion mode

This is a variation of the auto scan continuous conversion mode where conversion occurs on two user-selectable inputs. The result of the conversion of the first channel is placed in result register, AD1DAT0. The result of the conversion of the second channel is placed in result register, AD1DAT1. The first channel is again converted and its result stored in AD1DAT2. The second channel is again converted and its result placed in AD1DAT3. An interrupt is generated, if enabled, after every set of four conversions (two conversions per channel).

9.4.6 Single step mode

This special mode allows ‘single-stepping’ in an auto scan conversion mode. Any combination of the four input channels can be selected for conversion. After each channel is converted, an interrupt is generated, if enabled, and the A/D waits for the next start condition. May be used with any of the start modes.

9.5 Conversion start modes

9.5.1 Timer triggered start

An A/D conversion is started by the overflow of Timer 0. Once a conversion has started, additional Timer 0 triggers are ignored until the conversion has completed. The Timer triggered start mode is available in all A/D operating modes.

9.5.2 Start immediately

Programming this mode immediately starts a conversion.This start mode is available in all A/D operating modes.

9.5.3 Edge triggered

An A/D conversion is started by rising or falling edge of P1.4. Once a conversion has started, additional edge triggers are ignored until the conversion has completed. The edge triggered start mode is available in all A/D operating modes.

9.6 Boundary limits interrupt

The A/D converter has both a high and low boundary limit register. After the four MSBs have been converted, these four bits are compared with the four MSBs of the boundary high and low registers. If the four MSBs of the conversion are outside the limit an interrupt will be generated, if enabled. If the conversion result is within the limits, the boundary limits will again be compared after all 8 bits have been converted. An interrupt will be generated, if enabled, if the result is outside the boundary limits. The boundary limit may be disabled by clearing the boundary limit interrupt enable.

Table 17. Dynamic characteristics (18 MHz)

V_{DD} = 3.0 V to 3.6 V unless otherwise specified.
T_{amb} = −40 °C to +85 °C, or −40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.[1][2]

Symbol	Parameter	Conditions	Variable clock		f_{osc} = 18 MHz		Unit
			Min	Max	Min	Max	
$f_{osc(RC)}$	internal RC oscillator frequency	industrial	7.189	7.557	7.189	7.557	MHz
		extended	7.004	7.741	7.004	7.741	MHz
$f_{osc(WD)}$	internal watchdog oscillator frequency		320	520	320	520	kHz
f_{CLKLP}	low power select clock frequency		0	8	-	-	MHz
Glitch filter							
t_{gr}	glitch rejection time	P1.5/$\overline{RST}$ pin	-	50	-	50	ns
		any pin except P1.5/$\overline{RST}$	-	15	-	15	ns
t_{sa}	signal acceptance time	P1.5/$\overline{RST}$ pin	125	-	125	-	ns
		any pin except P1.5/$\overline{RST}$	50	-	50	-	ns
External clock							
f_{osc}	oscillator frequency		0	18	-	-	MHz
$T_{cy(clk)}$	clock cycle time	see Figure 28	55	-	-	-	ns
t_{CHCX}	clock HIGH time	see Figure 28	22	$T_{cy(CLK)} - t_{CLCX}$	22	-	ns
t_{CLCX}	clock LOW time	see Figure 28	22	$T_{cy(CLK)} - t_{CHCX}$	22	-	ns
t_{CLCH}	clock rise time	see Figure 28	-	5	-	5	ns
t_{CHCL}	clock fall time	see Figure 28	-	5	-	5	ns
Shift register (UART mode 0)							
T_{XLXL}	serial port clock cycle time	see Figure 27	$16T_{cy(CLK)}$	-	888	-	ns
t_{QVXH}	output data set-up to clock rising edge time	see Figure 27	$13T_{cy(CLK)}$	-	722	-	ns
t_{XHQX}	output data hold after clock rising edge time	see Figure 27	-	$T_{cy(CLK)}$ + 20	-	75	ns
t_{XHDX}	input data hold after clock rising edge time	see Figure 27	-	0	-	0	ns
t_{XHDV}	input data valid to clock rising edge time	see Figure 27	150	-	150	-	ns
SPI interface							
f_{SPI}	SPI operating frequency						
	slave		0	$^{CCLK}/_{6}$	0	3.0	MHz
	master		-	$^{CCLK}/_{4}$	-	4.5	MHz
T_{SPICYC}	SPI cycle time	see Figure 23, 24, 25, 26					
	slave		$^{6}/_{CCLK}$	-	333	-	ns
	master		$^{4}/_{CCLK}$	-	222	-	ns
$t_{SPILEAD}$	SPI enable lead time	see Figure 25, 26					
	slave		250	-	250	-	ns
t_{SPILAG}	SPI enable lag time	see Figure 25, 26	250	-	250	-	ns

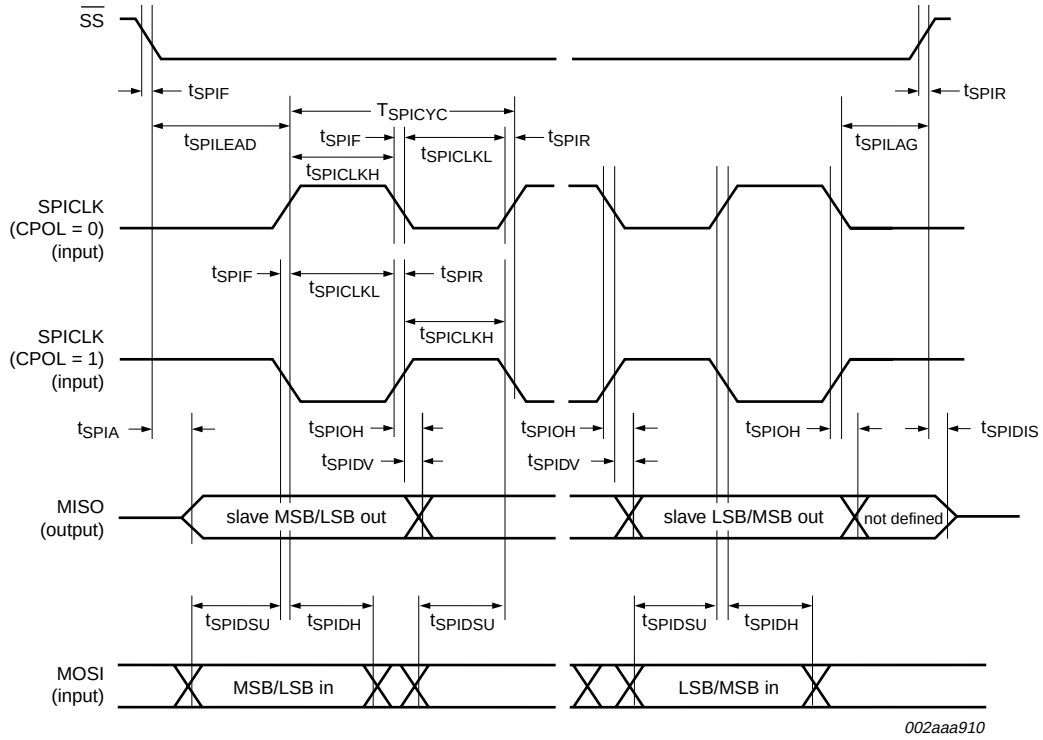

Fig 25. SPI slave timing (CPHA = 0)

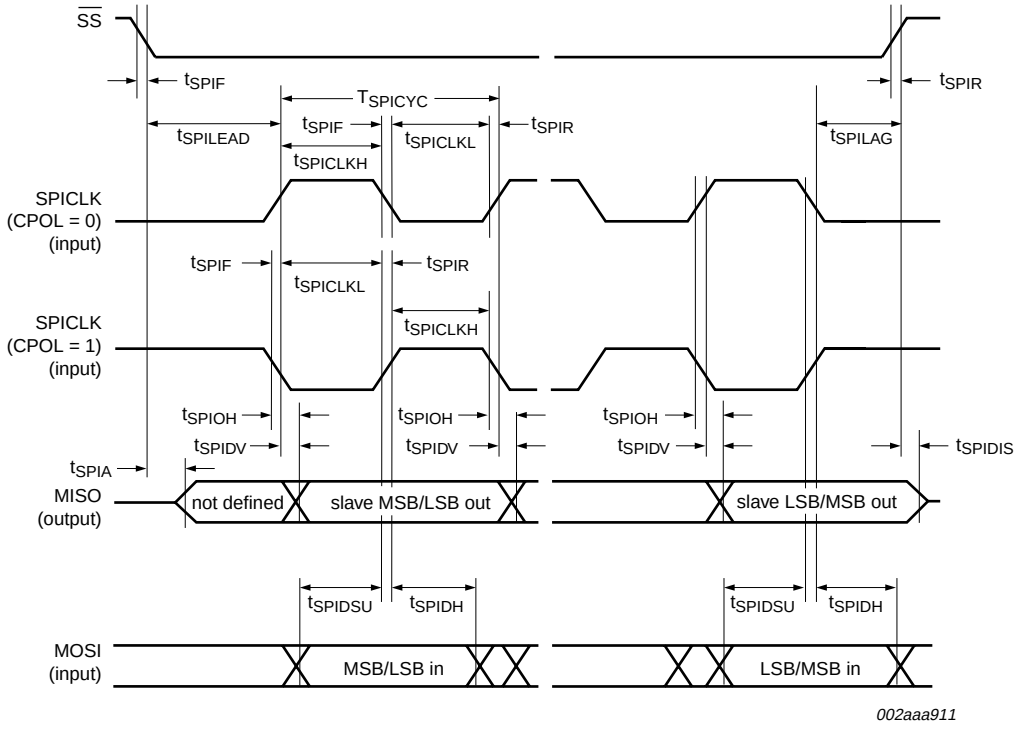

Fig 26. SPI slave timing (CPHA = 1)

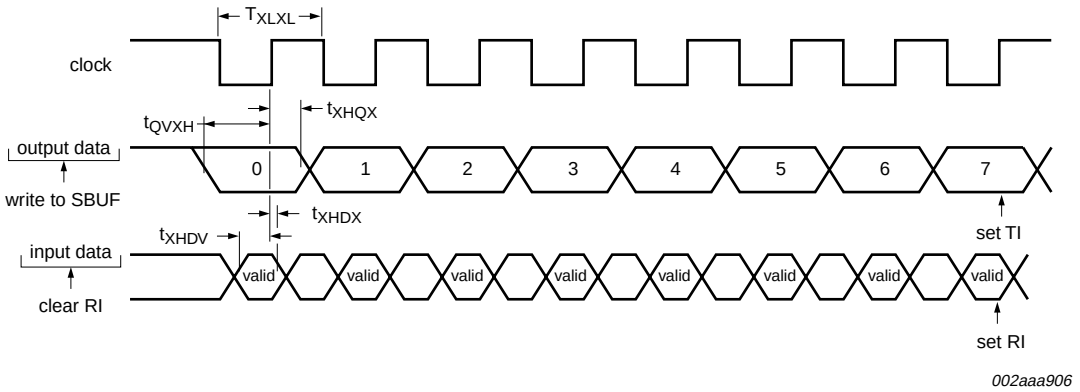

Fig 27. Shift register mode timing

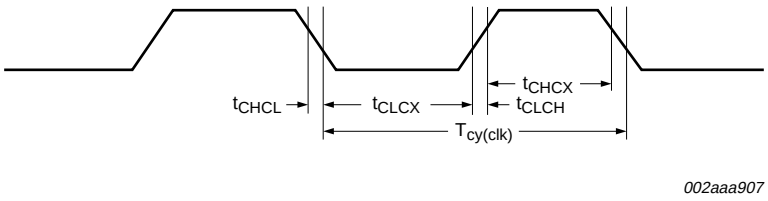

Fig 28. External clock timing

12.2 ISP entry mode

Table 18. Dynamic characteristics, ISP entry mode

V_{DD} = 2.4 V to 3.6 V, unless otherwise specified.
T_{amb} = −40 °C to +85 °C, or −40 °C to +125 °C (see Table 3 on page 3), unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{VR}	V_{DD} active to $\overline{RST}$ active delay time		50	-	-	µs
t_{RH}	$\overline{RST}$ HIGH time		1	-	32	µs
t_{RL}	$\overline{RST}$ LOW time		1	-	-	µs

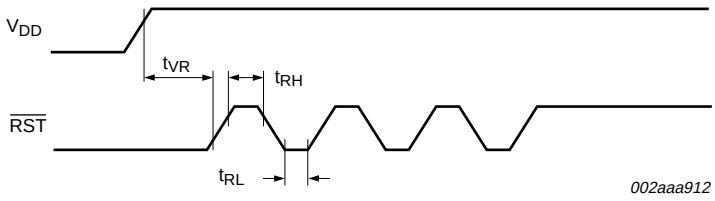

Fig 29. ISP entry timing

16. Revision history

Table 22. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
P89LPC915_916_917_5	20091215	Product data sheet	-	P89LPC915_916_917-04
Modifications:	• The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Added ADC electrical characteristics, Table 20. • Added P89LPC915FN.			
P89LPC915_916_917-04	20041217	Product data	-	P89LPC915_916_917-03
P89LPC915_916_917-03	20040701	Preliminary data	-	P89LPC915_916_917-02
P89LPC915_916_917-02	20040512	Preliminary data	-	P89LPC915_916_917-01
P89LPC915_916_917-01	20040408	Preliminary data	-	-

For more information, please visit: http://www.nxp.com
For sales office addresses, please send an email to: salesaddresses@nxp.com

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