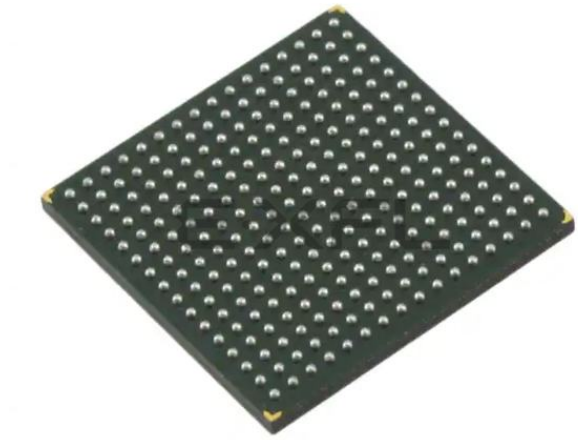

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Understanding Embedded - Microprocessors

Embedded microprocessors are specialized computing chips designed to perform specific tasks within an embedded system. Unlike general-purpose microprocessors found in personal computers, embedded microprocessors are tailored for dedicated functions within larger systems, offering optimized performance, efficiency, and reliability. These microprocessors are integral to the operation of countless electronic devices, providing the computational power necessary for controlling processes, handling data, and managing communications.

Applications of Embedded - Microprocessors

Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	266MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h435-266bcgi

Signal	Type	Name/Description
PCILOCKN	I/O	**PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	**PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	**PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.
PCIREQN[3:0]	I/O	**PCI Bus Request.** **In PCI host mode with internal arbiter:** These signals are inputs whose assertion indicates to the internal RC32435 arbiter that an agent desires ownership of the PCI bus. **In PCI host mode with external arbiter:** PCIREQN[0]: asserted by the RC32435 to request ownership of the PCI bus. PCIREQN[3:1]: unused and driven high. **In PCI satellite mode:** PCIREQN[0]: this signal is asserted by the RC32435 to request use of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions. PCIREQN[3:2]: unused and driven high.
PCIRSTN	I/O	**PCI Reset**. In host mode, this signal is asserted by the RC32435 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	**PCI System Error**. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	**PCI Stop**. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	**PCI Target Ready**. Driven by the bus target to indicate that the current data can complete.
General Purpose Input/Output		
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send.

Table 1 Pin Description (Part 3 of 6)

Signal	Type	Name/Description
EJTAG_TMS	I	**EJTAG Mode**. The value on this signal controls the test mode select of the EJTAG Controller. When using the JTAG boundary scan, this pin should be left disconnected (since there is an internal pull-up) or driven high.
JTAG_TRST_N	I	**JTAG Reset**. This active low signal asynchronously resets the boundary scan logic, JTAG TAP Controller, and the EJTAG Debug TAP Controller. An external pull-up on the board is recommended to meet the JTAG specification in cases where the tester can access this signal. However, for systems running in functional mode, one of the following should occur: 1) actively drive this signal low with control logic 2) statically drive this signal low with an external pull-down on the board 3) clock JTAG_TCK while holding EJTAG_TMS and/or JTAG_TMS high.
JTAG_TCK	I	**JTAG Clock**. This is an input test clock used to clock the shifting of data into or out of the boundary scan logic, JTAG Controller, or the EJTAG Controller. JTAG_TCK is independent of the system and the processor clock with a nominal 50% duty cycle.
JTAG_TDO	O	**JTAG Data Output**. This is the serial data shifted out from the boundary scan logic, JTAG Controller, or the EJTAG Controller. When no data is being shifted out, this signal is tri-stated.
JTAG_TDI	I	**JTAG Data Input**. This is the serial data input to the boundary scan logic, JTAG Controller, or the EJTAG Controller.
System		
CLK	I	**Master Clock.** This is the master clock input. The processor frequency is a multiple of this clock frequency. This clock is used as the system clock for all memory and peripheral bus operations.
EXTBCV	I	**Load External Boot Configuration Vector.** When this pin is asserted (i.e., high) the boot configuration vector is loaded from an externally supplied value during a cold reset. When this pin is negated, the boot configuration vector is taken from the NVRAM located on-chip.
EXTCLK	O	**External Clock.** This clock is used for all memory and peripheral bus operations.
COLDRSTN	I	**Cold Reset.** The assertion of this signal initiates a cold reset. This causes the processor state to be initialized, boot configuration to be loaded, and the internal PLL to lock onto the master clock (CLK).
RSTN	I/O	**Reset.** The assertion of this bidirectional signal initiates a warm reset. This signal is asserted by the RC32435 during a warm reset.

Table 1 Pin Description (Part 6 of 6)

Signal	Name/Description
MADDR[11]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MADDR[13:12]	**Reserved**. These pins must be driven low during boot configuration.
MADDR[15:14]	**Reserved**. Must be set to zero.

Table 3 Boot Configuration Encoding (Part 2 of 2)

System Clock Parameters

(Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 15 and 16.)

Parameter	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
PCLK[1]	Frequency	none	200	266	200	300	200	350	200	400	MHz	See Figure 3.
	Tper		3.8	5.0	3.3	5.0	2.85	5.0	2.5	5.0	ns	
ICLK[2,3,4]	Frequency	none	100	133	100	150	100	175	100	200	MHz	
	Tper		7.5	10.0	6.7	10.0	5.7	10.0	5.0	10.0	ns	
CLK[5]	Frequency	none	25	125	25	125	25	125	25	125	MHz	
	Tper_5a		8.0	40.0	8.0	40.0	8.0	40.0	8.0	40.0	ns	
	Thigh_5a, Tlow_5a		40	60	40	60	40	60	40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	—	3.0	—	3.0	—	3.0	ns	
	Tjitter_5a		—	0.1	—	0.1	—	0.1	—	0.1	ns	

Table 5 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3). Refer to Chapter 3, Clocking and Initialization, in the RC32435 User Reference Manual for the allowable frequency ranges of CLK and PCLK.
2. ICLK is the internal IPBus clock. It is always equal to PCLK divided by 2. This clock cannot be sampled externally.
3. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).
4. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.
5. The input clock (CLK) is input from the external oscillator to the internal PLL.

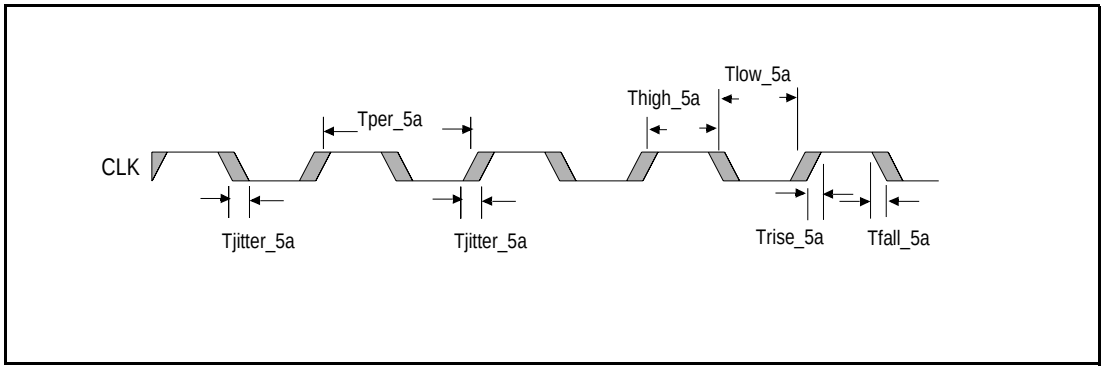


Figure 3 Clock Parameters Waveform

AC Timing Characteristics

(Values given below are based on systems running at recommended operating temperatures and supply voltages, shown in Tables 15 and 16.)

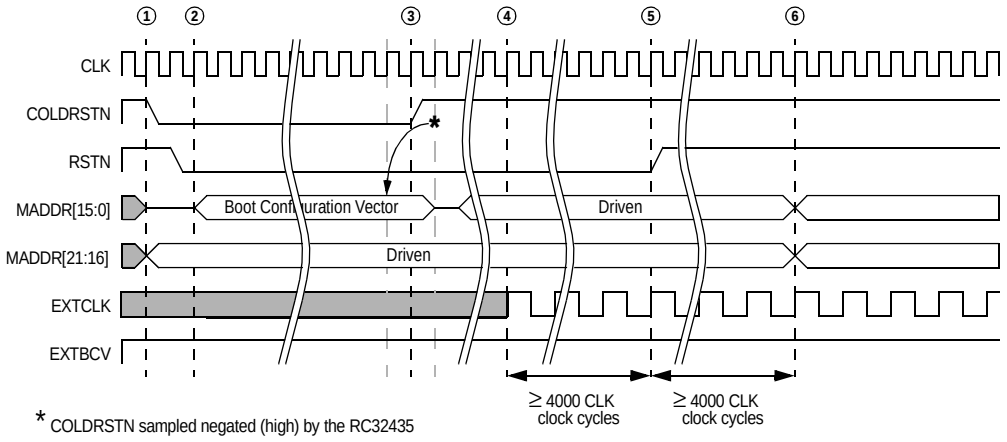
Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**			
Reset													
COLDRSTN[1]	Tpw_6a[2]	none	OSC	—	OSC	—	OSC	—	OSC	—	ms	Cold reset	See Figures 4 and 5.
	Trise_6a	none	—	5.0	—	5.0	—	5.0	—	5.0	ns	Cold reset	
RSTN[3] (input)	Tpw_6b[2]	none	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	
RSTN[3] (output)	Tdo_6c	COLDRSTN falling	—	15.0	—	15.0	—	15.0	—	15.0	ns	Cold reset	
MADDR[15:0] (boot vector)	Tdz_6d[2]	COLDRSTN falling	—	30.0	—	30.0	—	30.0	—	30.0	ns	Cold reset	
	Tdz_6d[2]	RSTN falling	—	5(CLK)	—	5(CLK)	—	5(CLK)	—	5(CLK)	ns	Warm reset	
	Tzd_6d[2]	RSTN rising	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns	Warm reset	

Table 6 Reset and System AC Timing Characteristics

1. The COLDRSTN minimum pulse width is the oscillator stabilization time (OSC) with V_{cc} stable.

2. The values for this symbol were determined by calculation, not by testing.

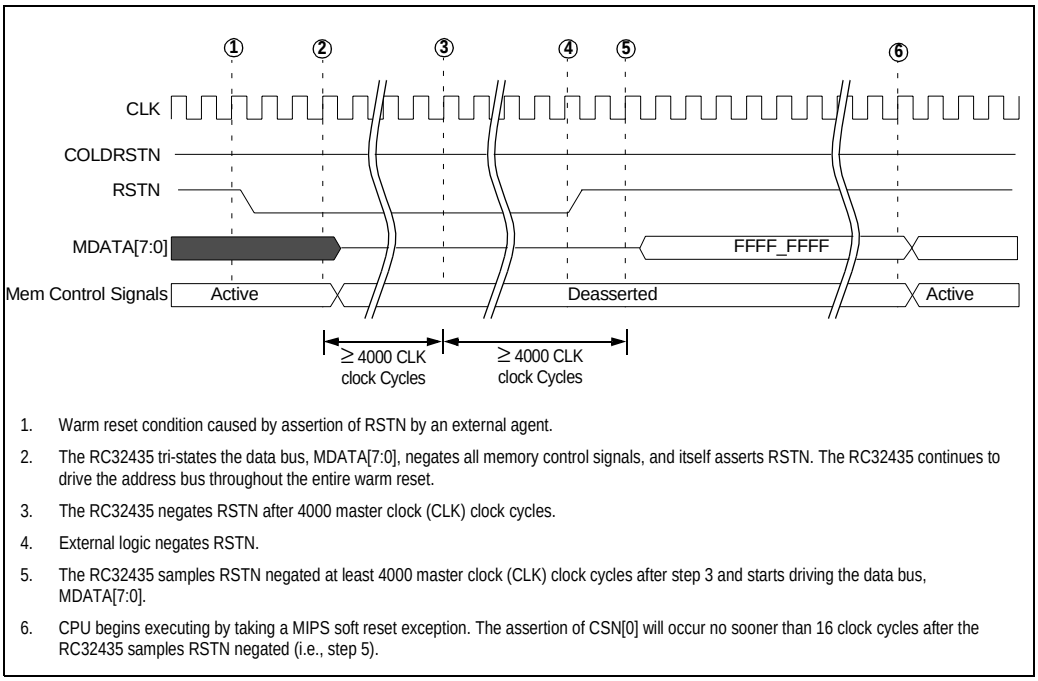
3. RSTN is a bidirectional signal. It is treated as an asynchronous input.



1. EXTBCV is asserted (i.e., pulled-up). COLDRSTN is asserted by external logic. The RC32435 responds by immediately tri-stating the bottom 16-bits of the memory and peripheral address bus (MADDR[15:0]), driving the remaining address bus signals (i.e., MADDR[21:16]), and asserting RSTN. EXTCLK is undefined at this point.
2. External logic drives the boot configuration vector on MADDR[15:0].
3. External logic negates COLDRSTN and tri-states the boot configuration vector on MADDR[15:0]. In response, the RC32435 stops sampling the boot configuration vector and retains the boot configuration vector value seen two clock cycles earlier (i.e., the value on the MADDR[15:0] lines two rising edges of CLK earlier). Within 16 CLK clock cycles after COLDRSTN is sampled negated, the RC32435 begins driving MADDR[15:0].
4. The RC32435 waits for the NVRAM to initialize (if the Disable NVRAM Initialization mode is not selected in the boot configuration vector) and for the PLL to stabilize.
5. The RC32435 then begins generating EXTCLK.
6. After at least 4000 CLK clock cycles, the RC32435 tri-states RSTN.
7. At least 4000 CLK clock cycles after negating RSTN, the RC32435 samples RSTN. If RSTN is negated, cold reset has completed and the RC32435 CPU begins executing by taking MIPS reset exception.

Figure 4 COLD Reset Operation with External Boot Configuration Vector AC Timing Waveform

Note: For a diagram showing the COLD Reset Operation with Internal Boot Configuration Vector, see Figure 3.6 in the RC32435 User Reference Manual.



1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32435 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32435 continues to drive the address bus throughout the entire warm reset.
3. The RC32435 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32435 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32435 samples RSTN negated (i.e., step 5).

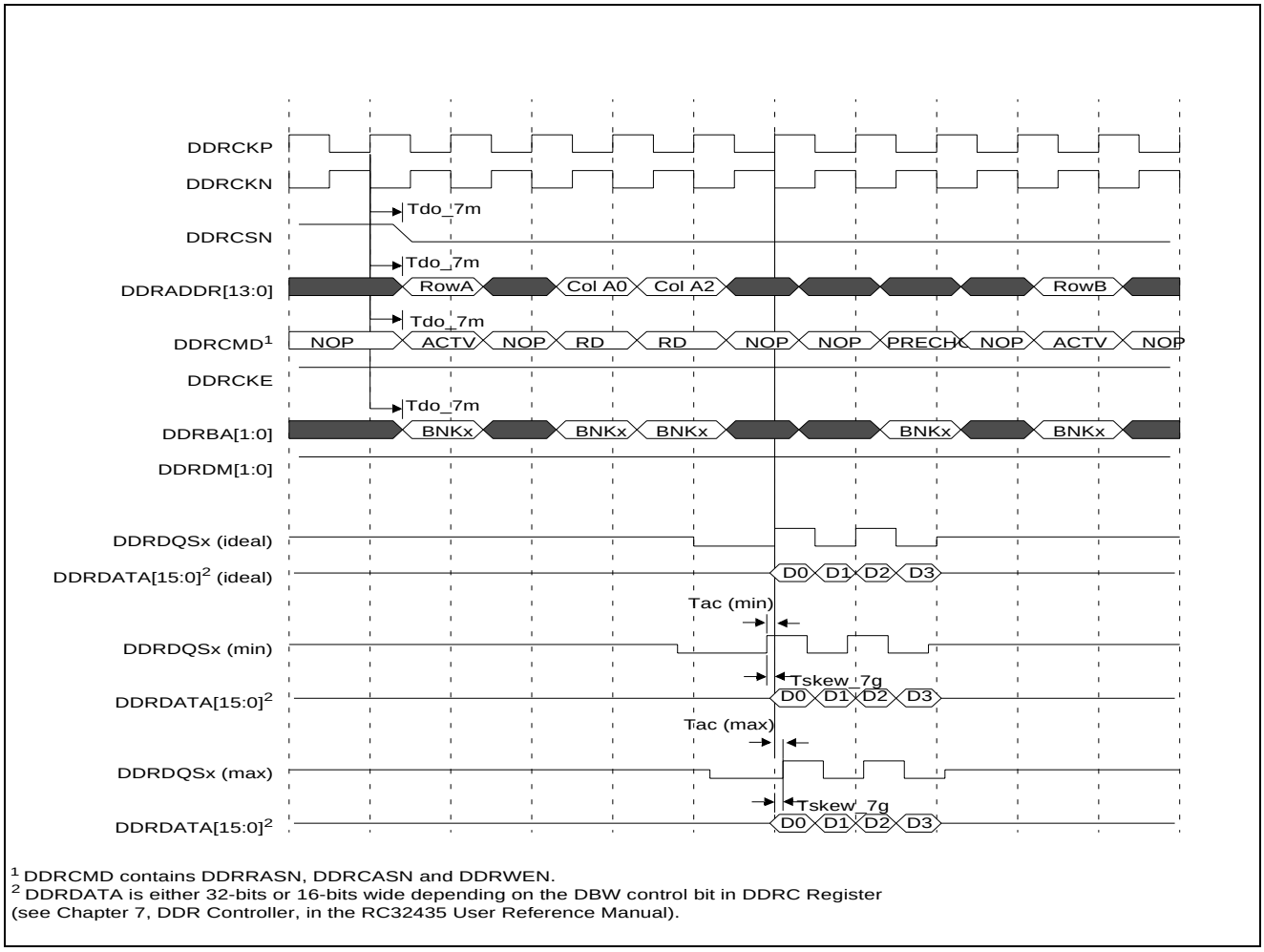
Figure 5 Externally Initiated Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

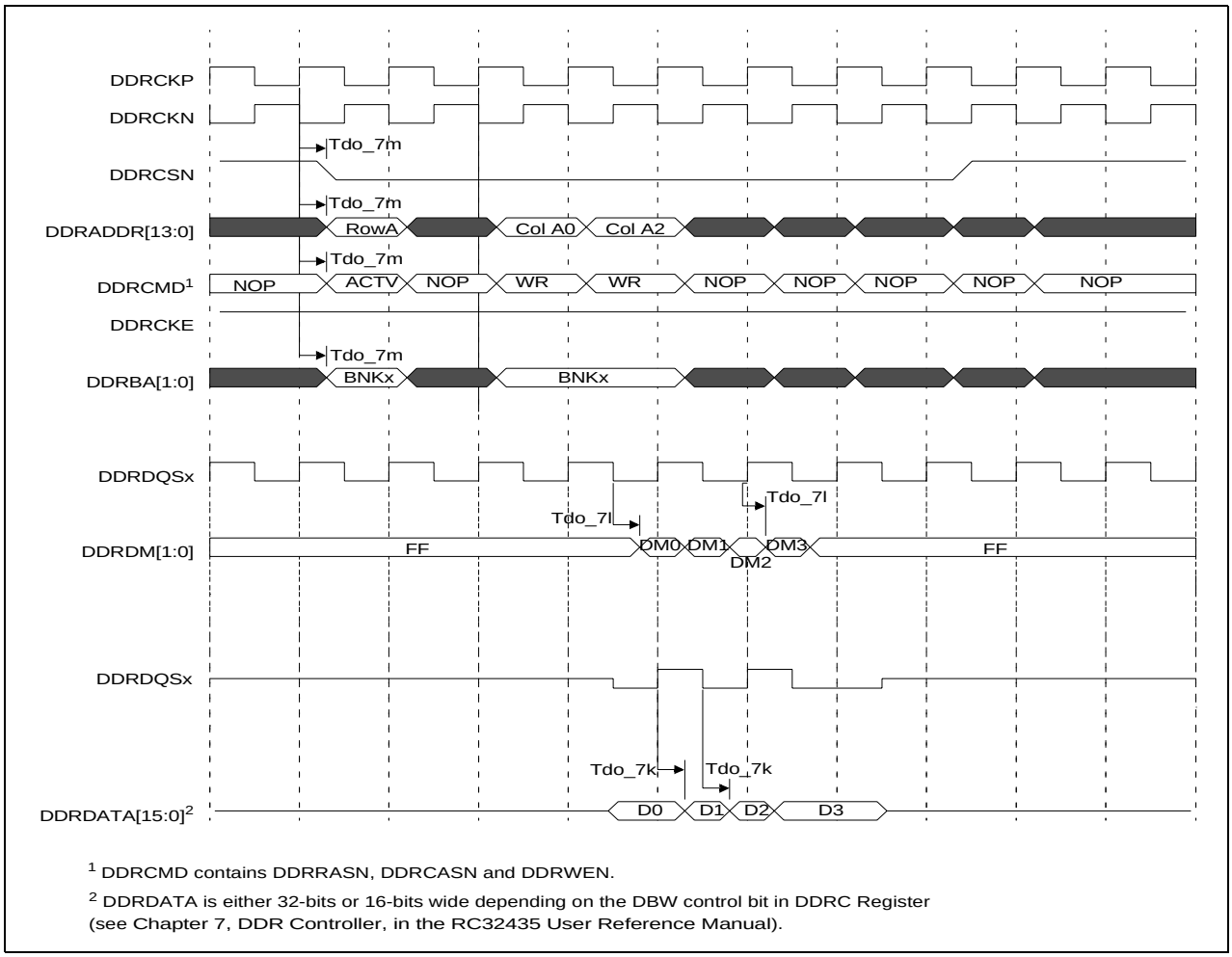
1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32435 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.
[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 6 DDR SDRAM AC Timing Waveform - SDRAM Read Access



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8a[2]		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8b[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

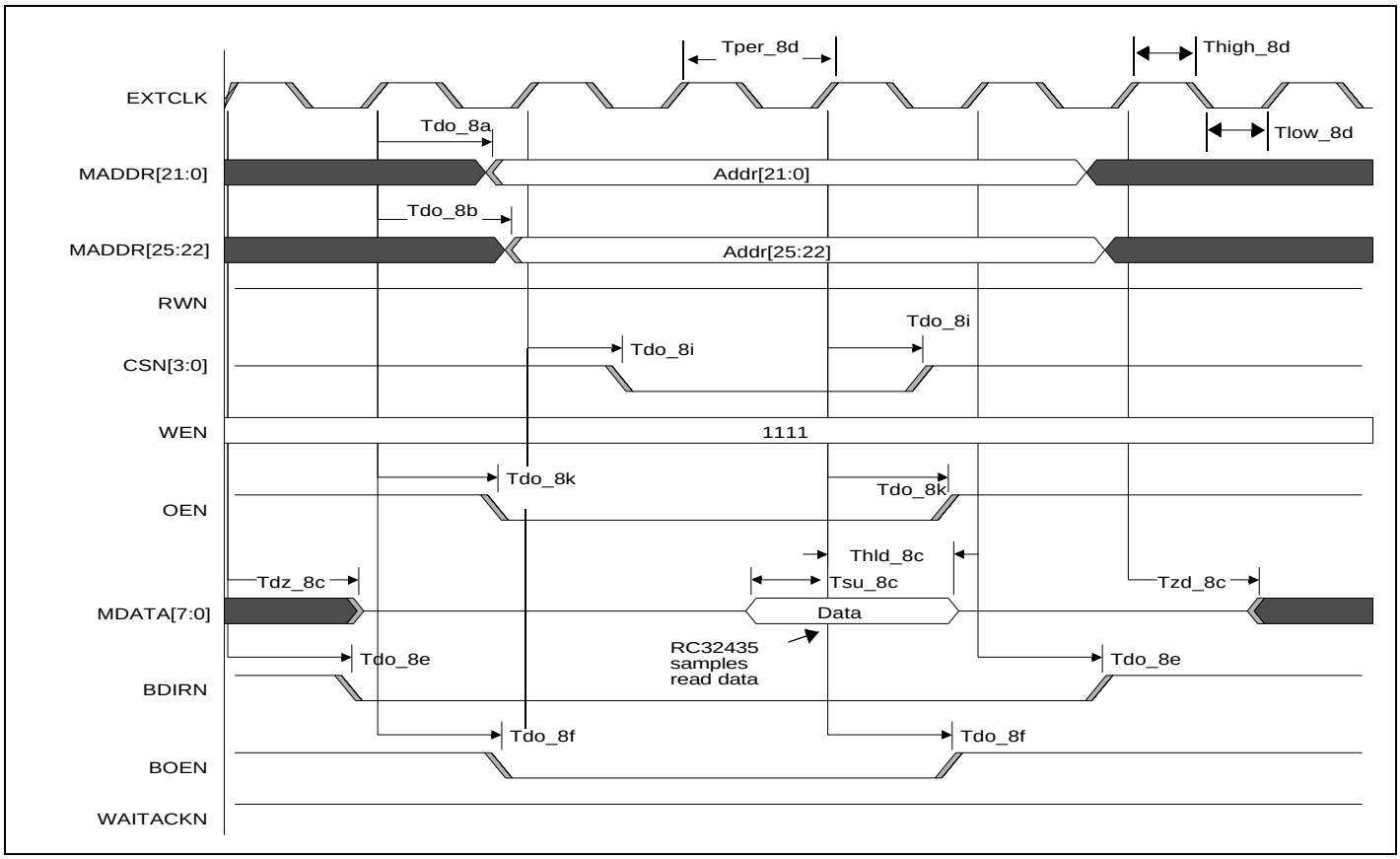


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

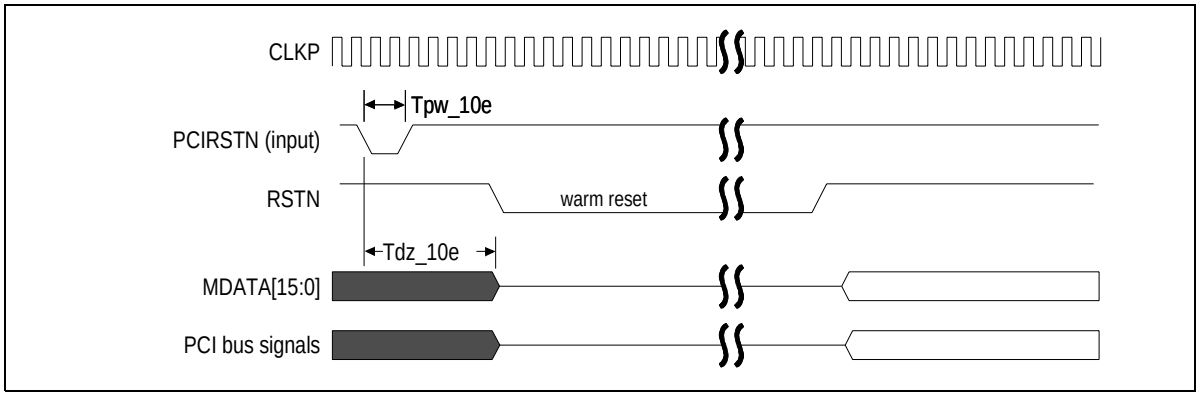


Figure 13 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
I²C[1]													
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 14.
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	µs		
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns		
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	µs		
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12b		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	µs		
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	µs		
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz	
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Trise_12a		—	300	—	300	—	300	—	300	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns		
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	µs		
	Trise_12b		—	300	—	300	—	300	—	300	ns		
	Tfall_12ba		—	300	—	300	—	300	—	300	ns		

Table 11 I²C AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Start or repeated start condition	Tsu_12c	SDA falling	0.6	—	0.6	—	0.6	—	0.6	—	µs	400 KHz	See Figure 14.
	Thld_12c		0.6	—	0.6	—	0.6	—	0.6	—	µs		
Stop condition	Tsu_12d	SDA rising	0.6	—	0.6	—	0.6	—	0.6	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		1.3	—	1.3	—	1.3	—	1.3	—	µs		

Table 11 I²C AC Timing Characteristics (Part 2 of 2)

1. For more information, see the I²C-Bus specification by Philips Semiconductor.

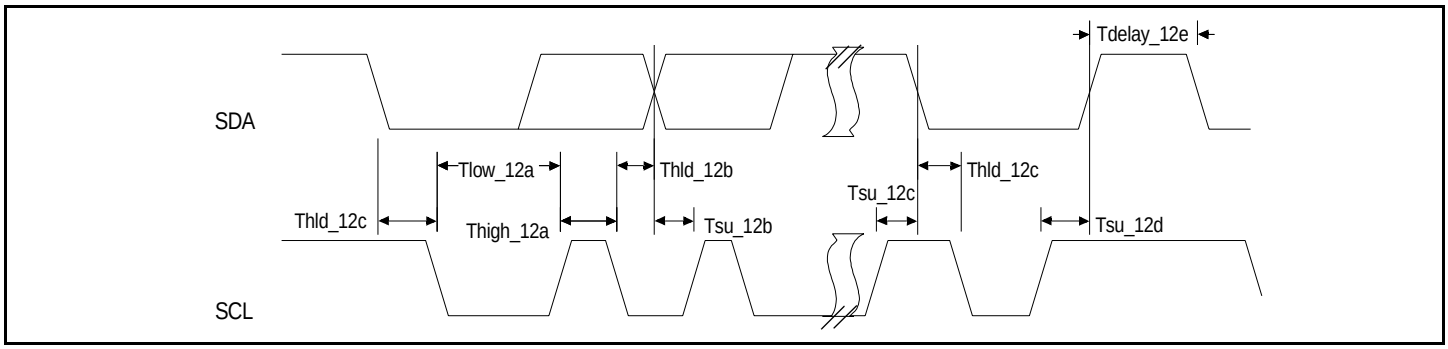


Figure 14 I2C AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
GPIO													
GPIO[13:0]	Tpw_13b[1]	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns		See Figure 15.

Table 12 GPIO AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

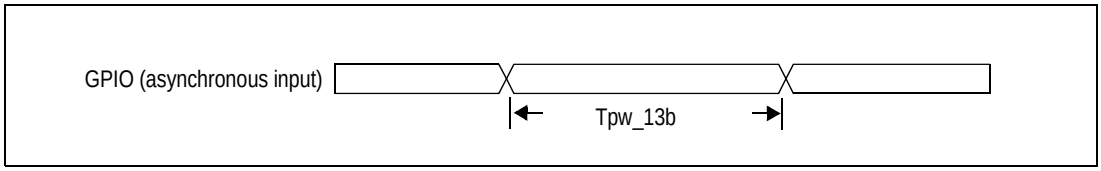


Figure 15 GPIO AC Timing Waveform

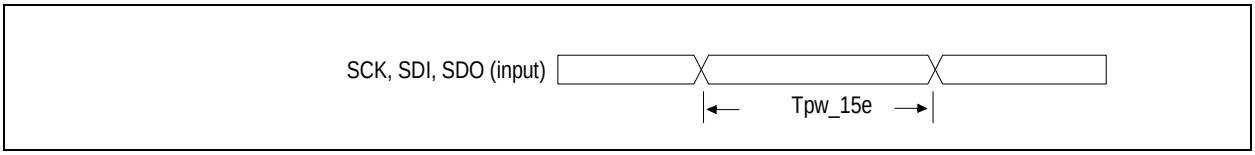


Figure 18 SPI AC Timing Waveform — Bit I/O Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
EJTAG and JTAG													
JTAG_TCK	Tper_16a	none	25.0	50.0	25.0	50.0	25.0	50.0	25.0	50.0	ns		See Figure 19.
	Thigh_16a, Tlow_16a		10.0	25.0	10.0	25.0	10.0	25.0	10.0	25.0	ns		
JTAG_TMS[1], JTAG_TDI	Tsu_16b	JTAG_TCK rising	2.4	—	2.4	—	2.4	—	2.4	—	ns		
	Thld_16b		1.0	—	1.0	—	1.0	—	1.0	—	ns		
JTAG_TDO	Tdo_16c	JTAG_TCK falling	—	11.3	—	11.3	—	11.3	—	11.3	ns		
	Tdz_16c[2]		—	11.3	—	11.3	—	11.3	—	11.3	ns		
JTAG_TRST_N	Tpw_16d[2]	none	25.0	—	25.0	—	25.0	—	25.0	—	ns		
EJTAG_TMS[1]	Tsu_16e	JTAG_TCK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
	Thld_6e		1.0	—	1.0	—	1.0	—	1.0	—	ns		

Table 14 JTAG AC Timing Characteristics

1. The JTAG specification, IEEE 1149.1, recommends that both JTAG_TMS and EJTAG_TMS should be held at 1 while the signal applied at JTAG_TRST_N changes from 0 to 1. Otherwise, a race may occur if JTAG_TRST_N is deasserted (going from low to high) on a rising edge of JTAG_TCK when either JTAG_TMS or EJTAG_TMS is low, because the TAP controller might go to either the Run-Test/Idle state or stay in the Test-Logic-Reset state.

2. The values for this symbol were determined by calculation, not by testing.

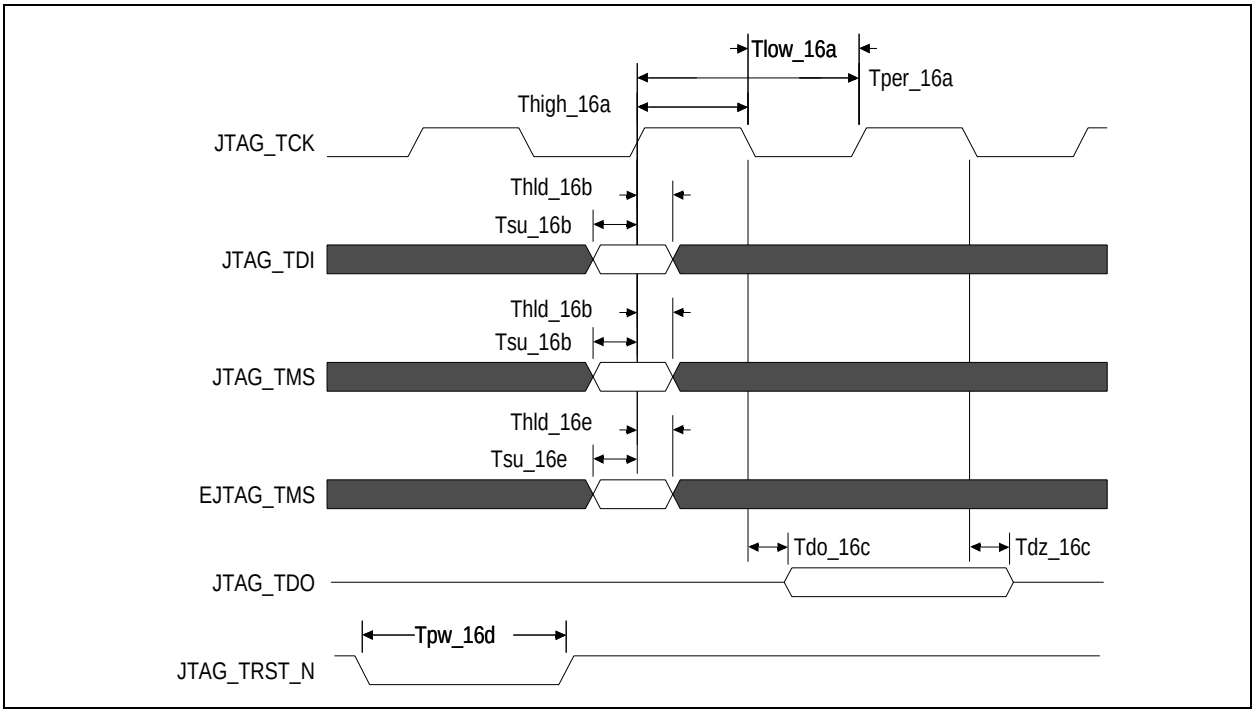


Figure 19 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32435 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 20 shows the electrical connection of the EJTAG probe target system connector.

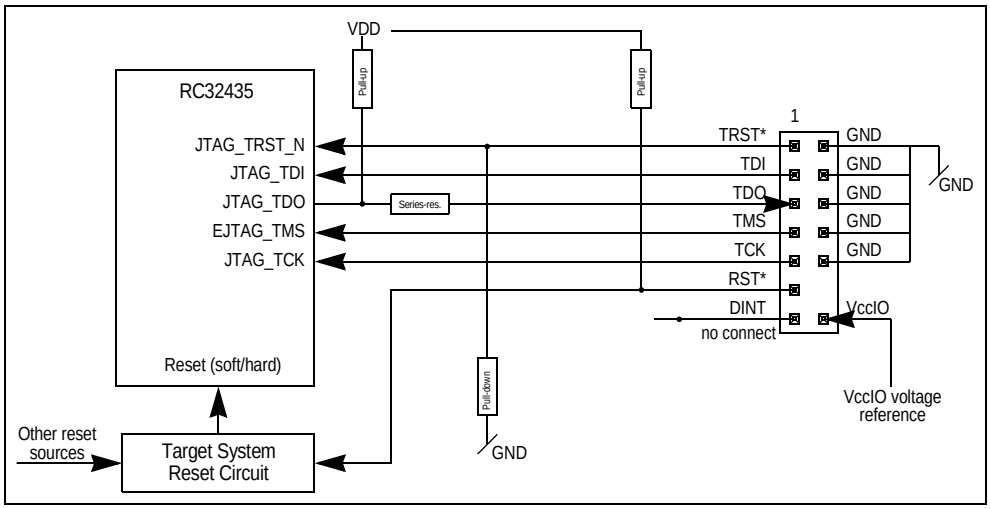


Figure 20 Target System Electrical EJTAG Connection

Power-on Sequence

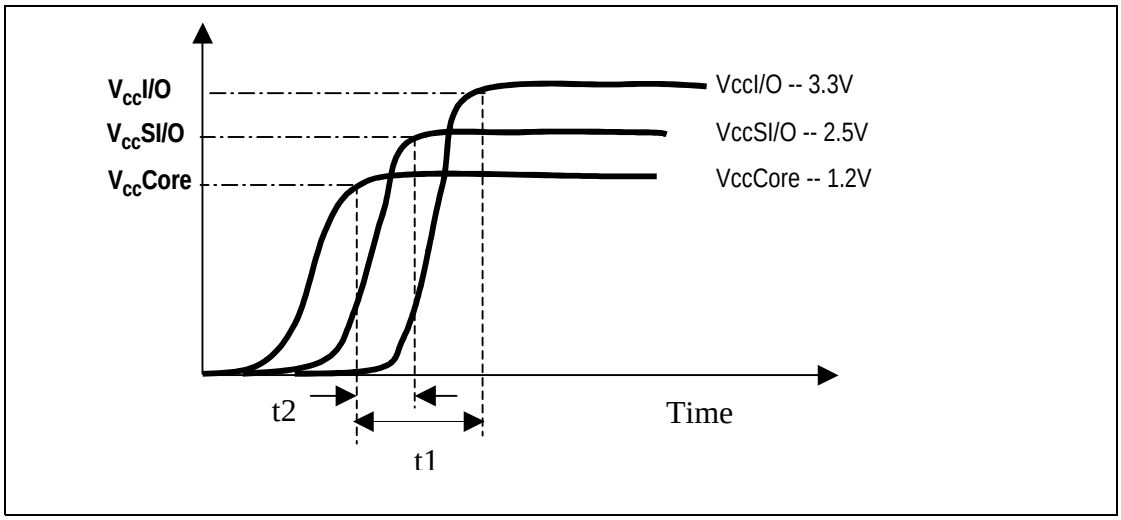
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

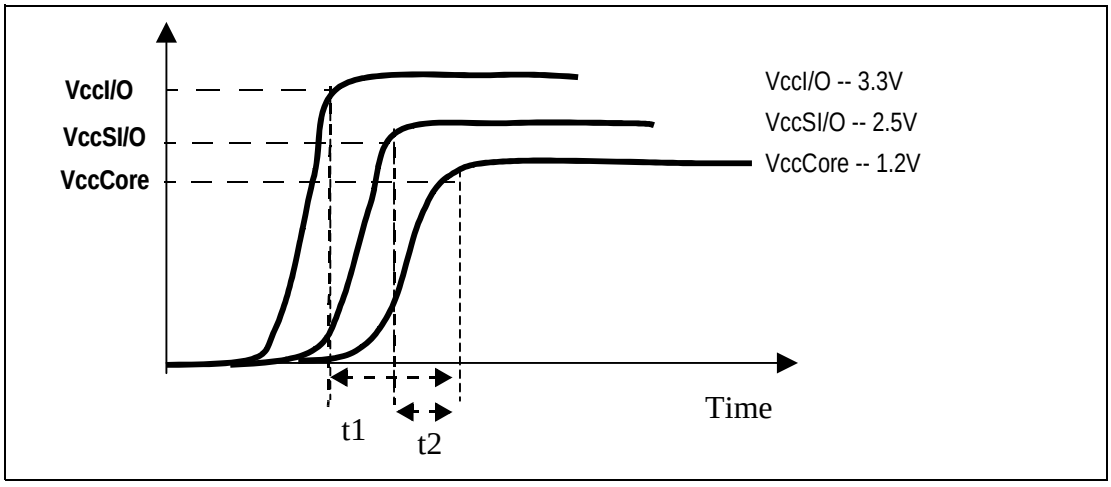
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

Note: See Table 2, Pin Characteristics, for a complete I/O listing.

I/O Type	Para-meter	Min.	Typical	Max.	Unit	Conditions
LOW Drive Output	I_{OL}	—	14.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-12.0	—	mA	V_{OH} = 1.5V
HIGH Drive Output	I_{OL}	—	41.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-42.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}	-0.3	—	0.8	V	—
	V_{IH}	2.0	—	V_{cc}I/O + 0.5	V	—
SSTL_2 (for DDR SDRAM)	I_{OL}	7.6	—	—	mA	V_{OL} = 0.5V
	I_{OH}	-7.6	—	—	mA	V_{OH} = 1.76V
	V_{IL}	-0.3	—	0.5(V_{cc}SI/O) - 0.18	V	
	V_{IH}	0.5(V_{cc}SI/O) + 0.18	—	V_{cc}SI/O + 0.3	V	
PCI	I_{OH}(AC) Switching	-12(V_{cc}I/O)	—	—	mA	0 < V_{OUT} < 0.3(V_{cc}I/O)
		-17.1(V_{cc}I/O - V_{OUT})	—	—	mA	0.3(V_{cc}I/O) < V_{OUT} < 0.9(V_{cc}I/O)
		—	—	-32(V_{cc}I/O)	—	0.7(V_{cc}I/O)
		16(V_{cc}I/O)	—	See Note 1	mA	0.7(V_{cc}I/O) < V_{OUT} < V_{cc}I/O
	I_{OL}(AC) Switching	+16(V_{cc}I/O)	—	—	mA	V_{cc}I/O > V_{OUT} > 0.6(V_{cc}I/O)
		+26.7(V_{OUT})	—	—	mA	0.6(V_{cc}I/O) > V_{OUT} > 0.1(V_{cc}I/O)
		—	—	+38(V_{cc}I/O)	mA	V_{OUT} = 0.18(V_{cc}I/O)
		—	—	See Note 2	mA	0.18(V_{cc}I/O) > V_{OUT} > 0
	V_{IL}	-0.3	—	0.3(V_{cc}I/O)	V	
	V_{IH}	0.5(V_{cc}I/O)	—	5.5	V	
Capacitance	C_{IN}	—	—	10.5	pF	—
Leakage	Inputs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/ downs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/ downs	—	—	± 80	µA	Vcc (max)

Table 18 DC Electrical Characteristics

Note 1: $I_{OH}(AC)\ max = (98/V_{CC}I/O) * (V_{OUT} - V_{CC}I/O) * (V_{OUT} + 0.4V_{CC}I/O)$

Note 2: $I_{OL}(AC)\ max = (256/V_{CC}I/O) * V_{OUT} * (V_{CC}I/O - V_{OUT})$

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[2]	-0.6	4.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply (digital)	-0.6	2.0	V
V_{CC}APLL	PLL supply (analog)	-0.6	4.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C2	BDIRN		G2	MIITXER		L2	SCL		R2	PCICBEN[3]	
C3	COLDRSTN		G3	MIIRXER		L3	GPIO[8]	1	R3	PCIAD[23]	
C4	WEN		G4	MIITXCLK		L4	SDI		R4	PCIAD[21]	
C5	MDATA[3]		G5	V_{CC} I/0		L5	V_{CC} I/0		R5	PCIAD[17]	
C6	MDATA[5]		G6	V_{SS}		L6	V_{SS}		R6	PCIRSTN	
C7	GPIO[6]	1	G7	V_{SS}		L7	V_{SS}		R7	PCICBEN[2]	
C8	MADDR[21]		G8	V_{SS}		L8	V_{CC} CORE		R8	PCITRDYN	
C9	MADDR[18]		G9	V_{SS}		L9	V_{SS}		R9	PCICBEN[1]	
C10	MADDR[14]		G10	V_{SS}		L10	V_{SS}		R10	PCIAD[12]	
C11	JTAG_TMS		G11	V_{SS}		L11	V_{SS}		R11	PCIAD[8]	
C12	V_{CC} APLL		G12	V_{CC} DDR		L12	V_{CC} DDR		R12	PCIAD[5]	
C13	CLK		G13	DDRDM[1]		L13	DDRADDR[9]		R13	PCIAD[3]	
C14	MADDR[4]		G14	DDRDQS[1]		L14	DDRWEN		R14	PCIAD[0]	
C15	MADDR[0]		G15	DDRDATA[10]		L15	DDRCASN		R15	PCIGNTN[2]	
C16	DDRDATA[0]		G16	DDRDATA[11]		L16	DDRADDR[8]		R16	DDRADDR[1]	
D1	MIIRXD[0]		H1	MIIMDIO		M1	GPIO[12]	1	T1	PCIAD[24]	
D2	MIICL		H2	MIIMDC		M2	PCIAD[31]		T2	GPIO[13]	1
D3	MIICRS		H3	GPIO[0]	1	M3	GPIO[11]	1	T3	PCIAD[22]	
D4	MIIRXD[1]		H4	GPIO[1]	1	M4	GPIO[9]	1	T4	PCIAD[19]	
D5	MDATA[7]		H5	V_{CC} CORE		M5	V_{CC} I/0		T5	PCIAD[16]	
D6	MDATA[2]		H6	V_{CC} CORE		M6	V_{CC} I/0		T6	PCICLK	
D7	MDATA[0]		H7	V_{SS}		M7	V_{CC} I/0		T7	PCIGNTN[0]	
D8	MADDR[20]		H8	V_{SS}		M8	V_{CC} CORE		T8	PCIDEVSELN	
D9	MADDR[19]		H9	V_{SS}		M9	V_{CC} CORE		T9	PCIPAR	
D10	MADDR[15]		H10	V_{SS}		M10	V_{CC} I/0		T10	PCIAD[13]	
D11	EXTBCV		H11	V_{SS}		M11	V_{CC} DDR		T11	PCIAD[9]	
D12	JTAG_TRSTN		H12	V_{CC} CORE		M12	V_{CC} DDR		T12	PCIAD[6]	
D13	WAITACKN		H13	DDRDATA[15]		M13	DDRRASN		T13	PCIAD[2]	
D14	DDRDATA[2]		H14	DDRDATA[14]		M14	DDRBA[1]		T14	PCIAD[1]	
D15	DDRDATA[3]		H15	DDRDATA[12]		M15	DDRADDR[6]		T15	PCIGNTN[1]	
D16	DDRDATA[1]		H16	DDRDATA[13]		M16	DDRADDR[7]		T16	PCIGNTN[3]	

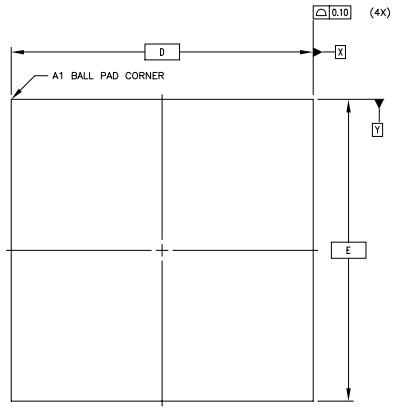
Table 20 RC32435 Pinout (Part 2 of 2)

Signal Name	I/O Type	Location	Signal Category
DDRADDR[0]	O	P14	DDR Bus
DDRADDR[1]	O	R16	
DDRADDR[2]	O	P15	
DDRADDR[3]	O	N15	
DDRADDR[4]	O	N14	
DDRADDR[5]	O	N13	
DDRADDR[6]	O	M15	
DDRADDR[7]	O	M16	
DDRADDR[8]	O	L16	
DDRADDR[9]	O	L13	
DDRADDR[10]	O	K15	
DDRADDR[11]	O	K14	
DDRADDR[12]	O	K16	
DDRADDR[13]	O	E15	
DDRBA[0]	O	N16	
DDRBA[1]	O	M14	
DDRCASN	O	L15	
DDRCKE	O	K13	
DDRCKN	O	J13	
DDRCKP	O	J15	
DDRCSN	O	P16	
DDRDATA[0]	I/O	C16	
DDRDATA[1]	I/O	D16	
DDRDATA[2]	I/O	D14	
DDRDATA[3]	I/O	D15	
DDRDATA[4]	I/O	E16	
DDRDATA[5]	I/O	E14	
DDRDATA[6]	I/O	E13	
DDRDATA[7]	I/O	F16	
DDRDATA[8]	I/O	F14	
DDRDATA[9]	I/O	F13	
DDRDATA[10]	I/O	G15	
DDRDATA[11]	I/O	G16	
DDRDATA[12]	I/O	H15	
DDRDATA[13]	I/O	H16	
DDRDATA[14]	I/O	H14	

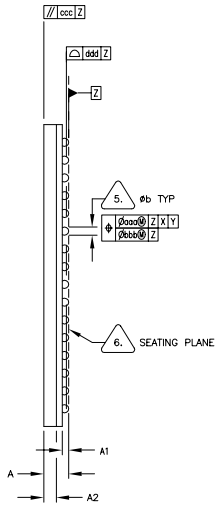
Table 24 RC32435 Alphabetical Signal List (Part 2 of 7)

RC32435 Package Drawing — 256-pin CABGA

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	



TOP VIEW



SIDE VIEW

SYMBOL	JEDEC VARIATION AAF-1 MIN	NOM	MAX	NOTE
A	1.30	1.40	1.70	
A1	.31	.36	.41	
A2	.65	.70	.75	
D		17.00 BSC		
D1		15.00 BSC		
E		17.00 BSC		
E1		15.00 BSC		
MD		16		3
ME		16		3
N		256		4
e		1.00 BSC		
b	.41	.46	.51	5
aaa	–	–	.15	
bbb	–	–	.08	
ccc	–	–	.10	
ddd	–	–	.12	

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: XX ±0.10, XXX ±0.05, XXXX ±0.08
ANGULAR: ±1°

APPROVALS	DATE
DRAWN	06/09/00
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727-6116 FAX (408) 492-8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC-4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 1 OF 2