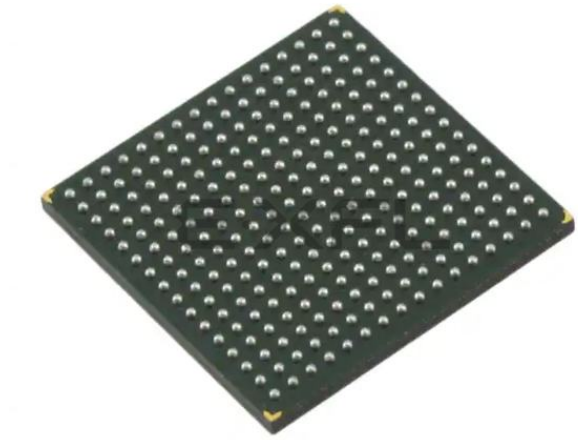

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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h435-300bc

Pin Description Table

The following table lists the functions of the pins provided on the RC32435. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32435 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

Signal	Type	Name/Description
PCILOCKN	I/O	**PCI Lock**. This signal is asserted by an external bus master to indicate that an exclusive operation is occurring.
PCIPAR	I/O	**PCI Parity**. Even parity of the PCIAD[31:0] bus. Driven by the bus master during address and write Data phases. Driven by the bus target during the read data phase.
PCIPERRN	I/O	**PCI Parity Error**. If a parity error is detected, this signal is asserted by the receiving bus agent 2 clocks after the data is received.
PCIREQN[3:0]	I/O	**PCI Bus Request.** **In PCI host mode with internal arbiter:** These signals are inputs whose assertion indicates to the internal RC32435 arbiter that an agent desires ownership of the PCI bus. **In PCI host mode with external arbiter:** PCIREQN[0]: asserted by the RC32435 to request ownership of the PCI bus. PCIREQN[3:1]: unused and driven high. **In PCI satellite mode:** PCIREQN[0]: this signal is asserted by the RC32435 to request use of the PCI bus. PCIREQN[1]: function changes to PCIIDSEL and is used as a chip select during configuration read and write transactions. PCIREQN[3:2]: unused and driven high.
PCIRSTN	I/O	**PCI Reset**. In host mode, this signal is asserted by the RC32435 to generate a PCI reset. In satellite mode, assertion of this signal initiates a warm reset.
PCISERRN	I/O	**PCI System Error**. This signal is driven by an agent to indicate an address parity error, data parity error during a special cycle command, or any other system error. Requires an external pull-up.
PCISTOPN	I/O	**PCI Stop**. Driven by the bus target to terminate the current bus transaction. For example, to indicate a retry.
PCITRDYN	I/O	**PCI Target Ready**. Driven by the bus target to indicate that the current data can complete.
General Purpose Input/Output		
GPIO[0]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SOUT Alternate function: UART channel 0 serial output.
GPIO[1]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0SINP Alternate function: UART channel 0 serial input.
GPIO[2]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0RTSN Alternate function: UART channel 0 request to send.
GPIO[3]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: U0CTSN Alternate function: UART channel 0 clear to send.

Table 1 Pin Description (Part 3 of 6)

Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32435 User Manual).
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32435 User Manual).
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

Boot Configuration Vector

The encoding of the boot configuration vector is described in Table 3, and the vector input is illustrated in Figure 4. The value of the boot configuration vector read in by the RC32435 during a cold reset may be determined by reading the Boot Configuration Vector (BCV) Register.

Signal	Name/Description
MADDR[3:0]	**CPU Pipeline Clock Multiplier**. This field specifies the value by which the PLL multiplies the master clock input (CLK) to obtain the processor clock frequency (PCLK). For master clock input frequency constraints, refer to Table 3.2 in the RC32435 User Manual. 0x0 - PLL Bypass 0x1 - Multiply by 3 0x2 - Multiply by 4 0x3 - Multiply by 5 - Reserved 0x4 - Multiply by 5 0x5 - Multiply by 6 - Reserved 0x6 - Multiply by 6 0x7 - Multiply by 8 0x8 - Multiply by 10 0x9 through 0xF - Reserved
MADDR[5:4]	**External Clock Divider**. This field specifies the value by which the IPBus clock (ICLK), which is always 1/2 PCLK, is divided in order to generate the external clock output on the EXTCLK pin. 0x0 - Divide by 1 0x1 - Divide by 2 0x2 - Divide by 4 0x3 - reserved
MADDR[6]	**Endian.** This bit specifies the endianness. 0x0 - little endian 0x1 - big endian
MADDR[7]	**Reset Mode**. This bit specifies the length of time the RSTN signal is driven. 0x0 - Normal reset: RSTN driven for minimum of 4000 clock cycles. If the internal boot configuration vector is selected, the expiration of an 18-bit counter operating at the master clock input (CLK) frequency is used as the PLL stabilization delay. 0x1 - Reserved
MADDR[10:8]	**PCI Mode**. This bit controls the operating mode of the PCI bus interface. The initial value of the EN bit in the PCIC register is determined by the PCI mode. 0x0 - Disabled (EN initial value is zero) 0x1 - PCI satellite mode with PCI target not ready (EN initial value is one) 0x2 - PCI satellite mode with suspended CPU execution (EN initial value is one) 0x3 - PCI host mode with external arbiter (EN initial value is zero) 0x4 - PCI host mode with internal arbiter using fixed priority arbitration algorithm (EN initial value is zero) 0x5 - PCI host mode with internal arbiter using round robin arbitration algorithm (EN initial value is zero) 0x6 - *reserved* 0x7 - *reserved*

Table 3 Boot Configuration Encoding (Part 1 of 2)

Logic Diagram — RC32435

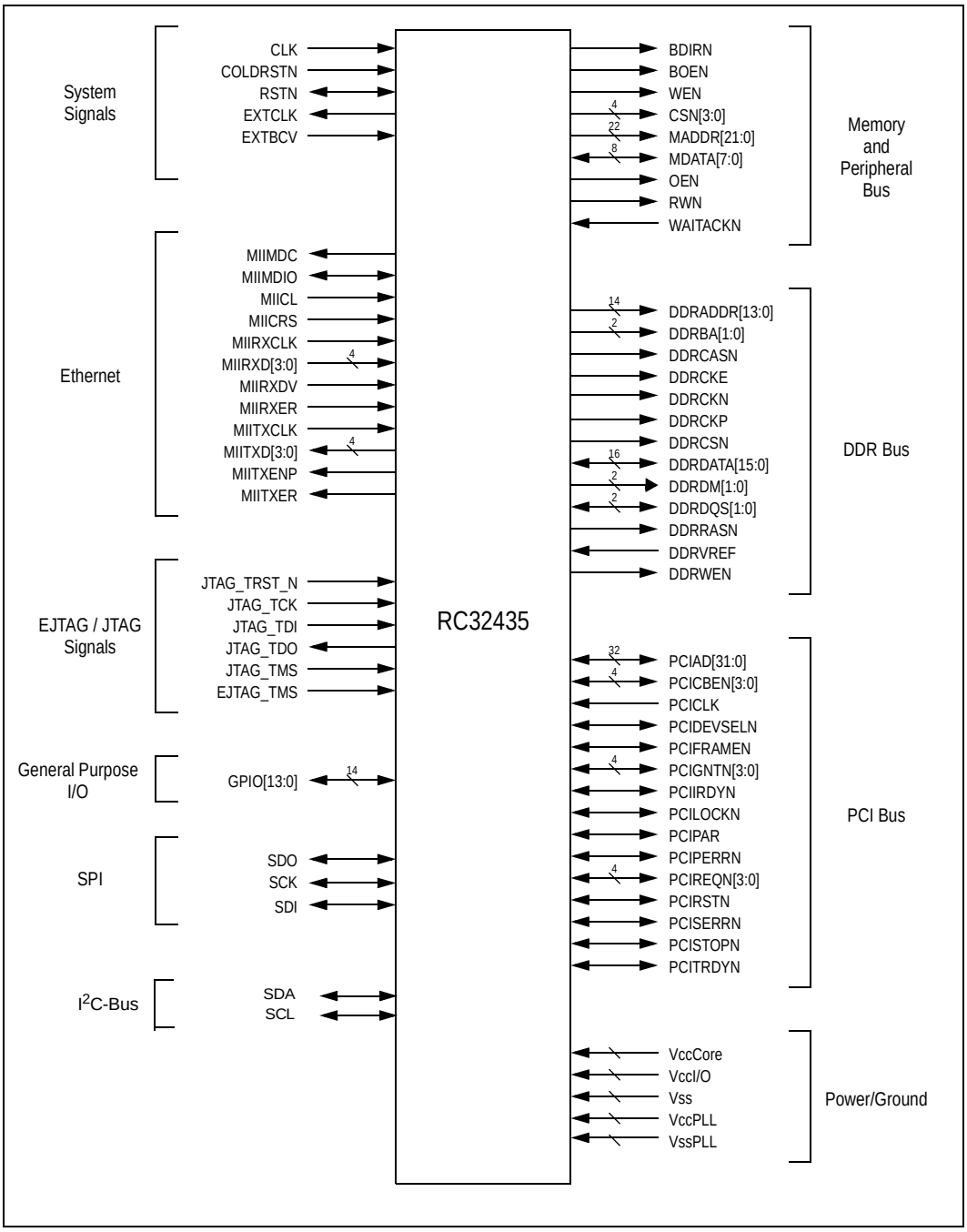


Figure 1 Logic Diagram

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

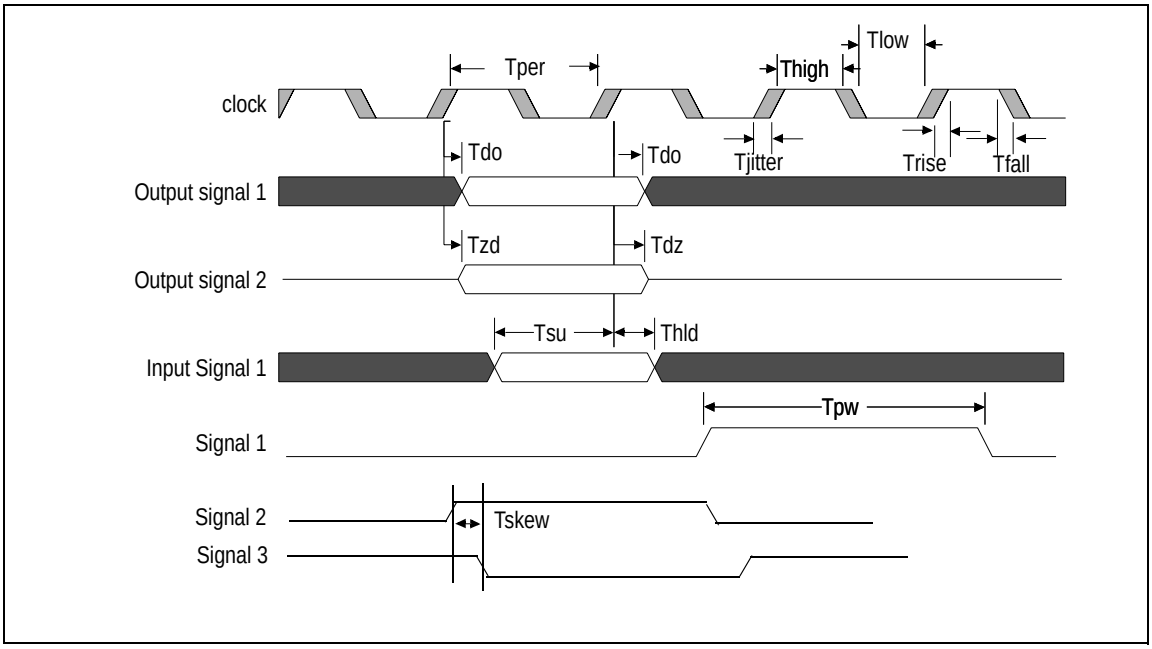
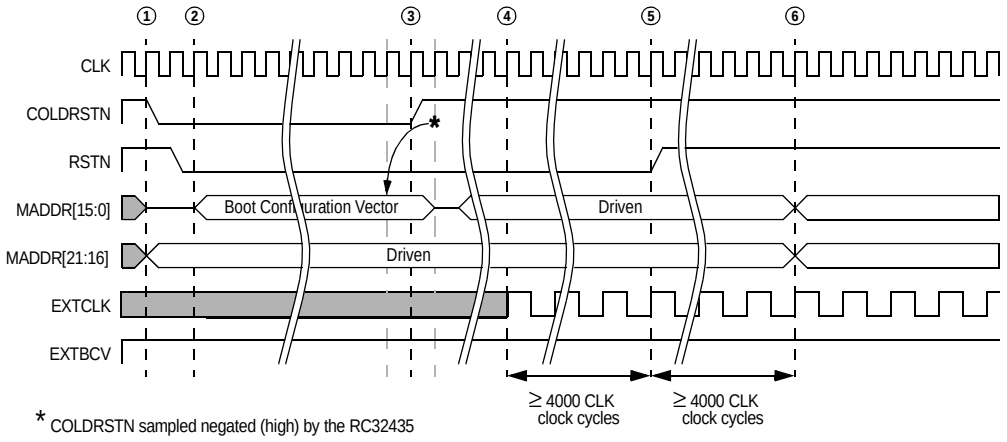


Figure 2 AC Timing Definitions Waveform

Symbol	Definition
Tper	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active for asynchronous signals.
Tslew	Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high.
X(clock)	Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200.
Tskew	Skew. The amount of time two signal edges deviate from one another.

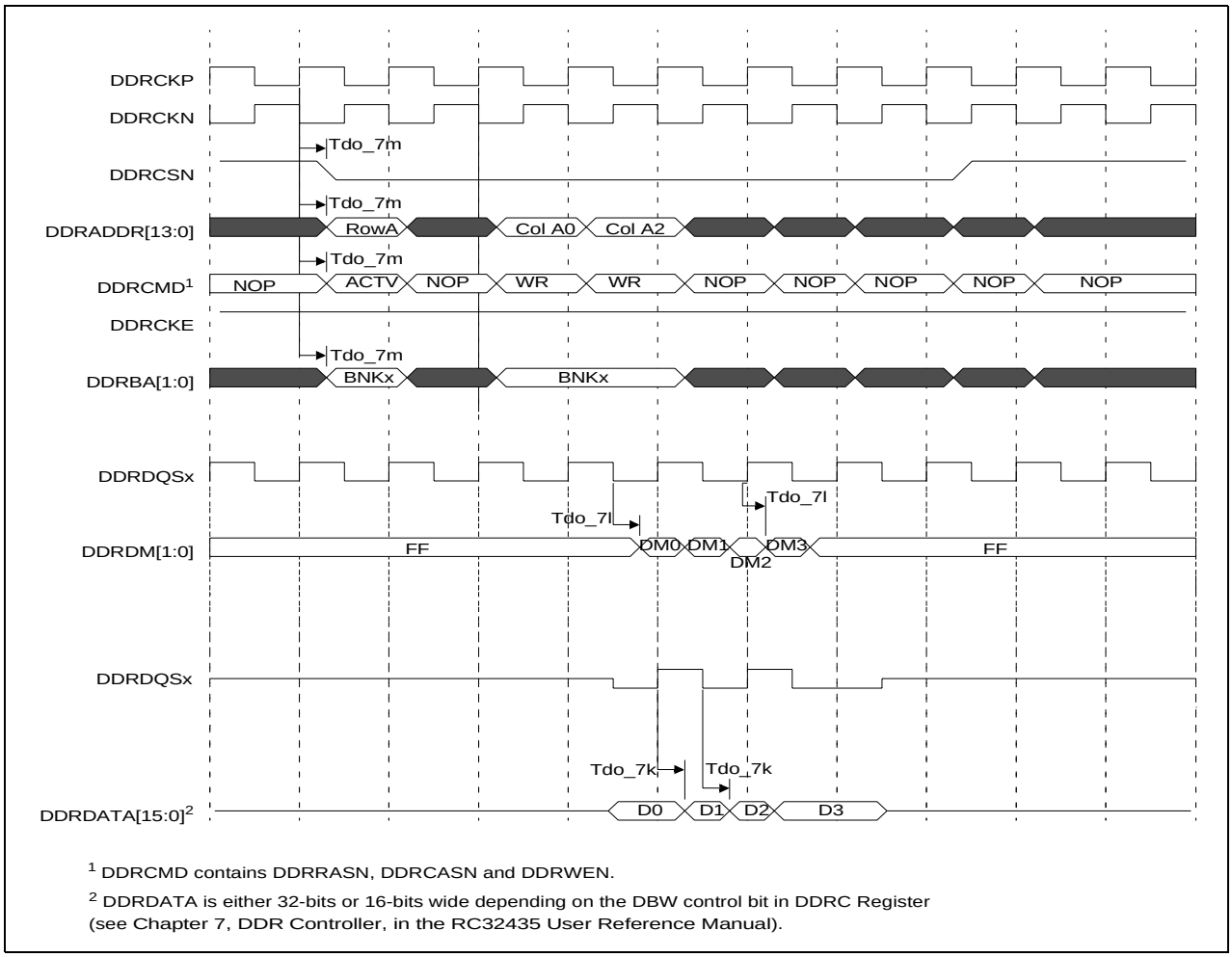
Table 4 AC Timing Definitions



1. EXTBCV is asserted (i.e., pulled-up). COLDRSTN is asserted by external logic. The RC32435 responds by immediately tri-stating the bottom 16-bits of the memory and peripheral address bus (MADDR[15:0]), driving the remaining address bus signals (i.e., MADDR[21:16]), and asserting RSTN. EXTCLK is undefined at this point.
2. External logic drives the boot configuration vector on MADDR[15:0].
3. External logic negates COLDRSTN and tri-states the boot configuration vector on MADDR[15:0]. In response, the RC32435 stops sampling the boot configuration vector and retains the boot configuration vector value seen two clock cycles earlier (i.e., the value on the MADDR[15:0] lines two rising edges of CLK earlier). Within 16 CLK clock cycles after COLDRSTN is sampled negated, the RC32435 begins driving MADDR[15:0].
4. The RC32435 waits for the NVRAM to initialize (if the Disable NVRAM Initialization mode is not selected in the boot configuration vector) and for the PLL to stabilize.
5. The RC32435 then begins generating EXTCLK.
6. After at least 4000 CLK clock cycles, the RC32435 tri-states RSTN.
7. At least 4000 CLK clock cycles after negating RSTN, the RC32435 samples RSTN. If RSTN is negated, cold reset has completed and the RC32435 CPU begins executing by taking MIPS reset exception.

Figure 4 COLD Reset Operation with External Boot Configuration Vector AC Timing Waveform

Note: For a diagram showing the COLD Reset Operation with Internal Boot Configuration Vector, see Figure 3.6 in the RC32435 User Reference Manual.



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8a[2]		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8b[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
MDATA[7:0]	Tsu_8c	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		See Figures 8 and 9 (cont.).
	Thld_8c		0	—	0	—	0	—	0	—	ns		
	Tdo_8c		0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8c[2]		0	0.5	0	0.5	0	0.5	0	0.5	ns		
	Tzd_8c[2]		0.4	3.3	0.4	3.3	0.4	3.3	0.4	3.3	ns		
EXTCLK[3]	Tper_8d	none	7.5	—	6.66	—	6.66	—	6.66	—	ns		
BDIRN	Tdo_8e	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8e[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8e[2]		—	—	—	—	—	—	—	—	ns		
BOEN	Tdo_8f	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8f[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8f[2]		—	—	—	—	—	—	—	—	ns		
WAITACKN[4]	Tsu_8h	EXTCLK rising	6.5	—	6.5	—	6.5	—	6.5	—	ns		
	Thld_8h		0	—	0	—	0	—	0	—	ns		
	Tpw_8h[2]	none	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	ns		
CSN[3:0]	Tdo_8i	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8i[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8i[2]		—	—	—	—	—	—	—	—	ns		
RWN	Tdo_8j	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8j[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8j[2]		—	—	—	—	—	—	—	—	ns		
OEN	Tdo_8k	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8k[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8k[2]		—	—	—	—	—	—	—	—	ns		
WEN	Tdo_8l	EXTCLK rising	0.4	3.7	0.4	3.7	0.4	3.7	0.4	3.7	ns		
	Tdz_8l[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8l[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

1. The RC32435 provides bus turnaround cycles to prevent bus contention when going from read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32435 are both driving. See Chapter 6, Device Controller, in the RC32435 User Reference Manual.

2. The values for this symbol were determined by calculation, not by testing.

3. The frequency of EXTCLK is programmable. See the External Clock Divider (MDATA[5:4]) description in Table 3 of this data sheet.

4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

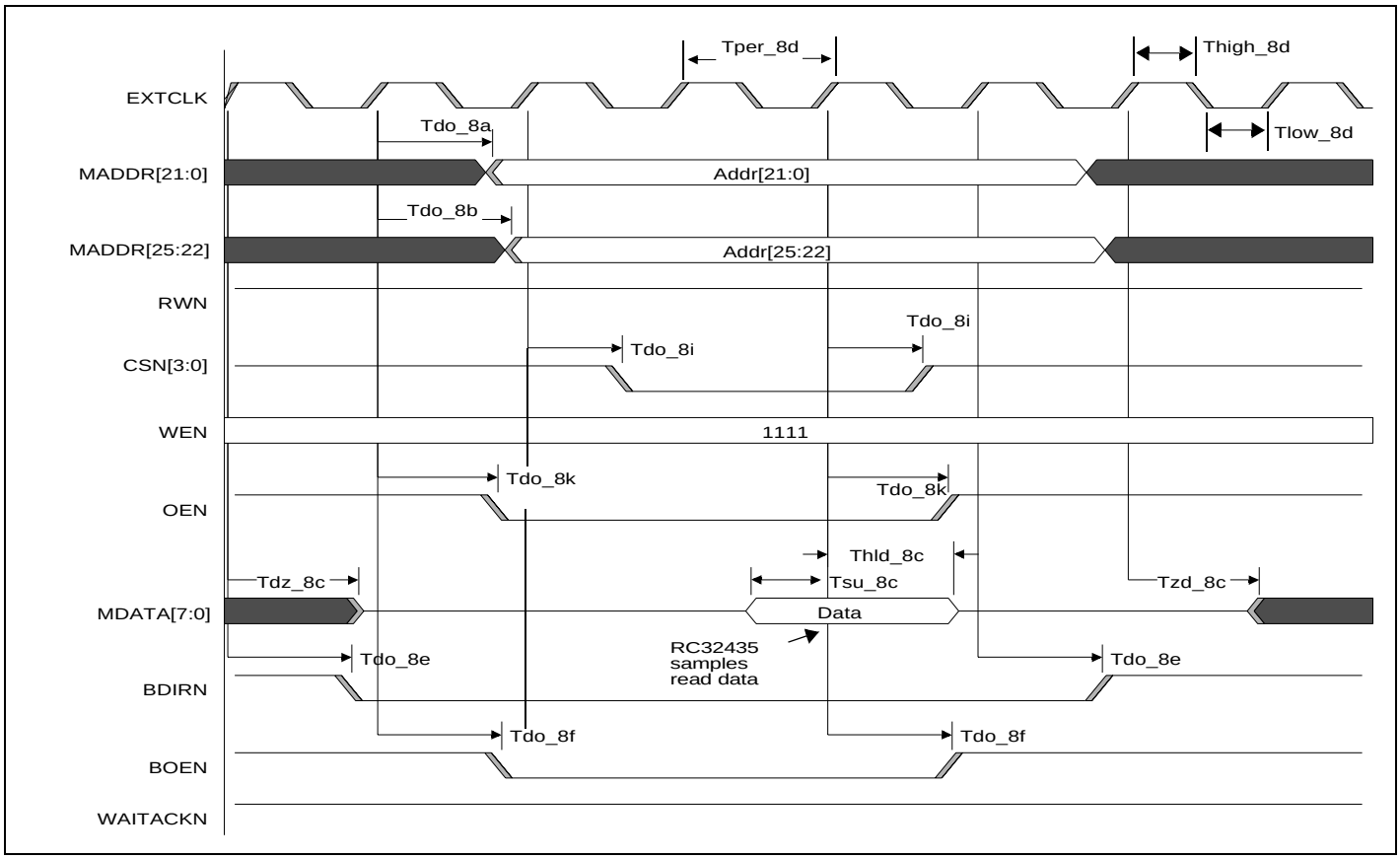


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Ethernet													
MIIMDC	Tper_9a	None	30.0	—	30.0	—	30.0	—	30.0	—	ns		See Figure 10.
	Thigh_9a, Tlow_9a		12.0	—	12.0	—	12.0	—	12.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9b		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_9b[1]		10	300	10	300	10	300	10	300	ns		
Ethernet — MII Mode													
MIIRXCLK, MIITXCLK[2]	Tper_9c	None	399.96	400.4	399.96	400.4	399.96	400.4	399.96	400.4	ns	10 Mbps	See Figure 10.
	Thigh_9c, Tlow_9c		140	260	140	260	140	260	140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	—	3.0	—	3.0	—	3.0	ns		
MIIRXCLK, MIITXCLK[2]	Tper_9d	None	39.9	40.0	39.9	40.0	39.9	40.0	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	14.0	26.0	14.0	26.0	14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	—	2.0	—	2.0	—	2.0	ns		
MIIRXD[3:0], MIIRXDV, MIIRXER	Tsu_9e	MIIxRXCLK rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9e		10.0	—	10.0	—	10.0	—	10.0	—	ns		
MIITXD[3:0], MIITXENP, MIITXER	Tdo_9f	MIIxTXCLK rising	0.0	25.0	0.0	25.0	0.0	25.0	0.0	25.0	ns		
Ethernet — RMII Mode													
RMIIREFCLK	Tper_9i	None	19.9	20.1	19.9	20.1	19.9	20.1	19.9	20.1	ns		See Figure 10.
	Thigh_9i, Tlow_9i		7.0	13.0	7.0	13.0	7.0	13.0	7.0	13.0	ns		
RMIITXEN, RMIITXD[1:0]	Tdo_9j	MIIRXCLK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
RMIICRSDV, RMIIRXER, RMIIRXD[1:0]	Tsu_9k		5.5	14.5	5.5	14.5	5.5	14.5	5.5	14.5	ns		

Table 9 Ethernet AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

2. The ethernet clock (MIIRXCLK and MIITXCLK) frequency must be equal to or less than 1/2 ICLK (MIIRXCLK and MIITXCLK <= 1/2(ICLK)).

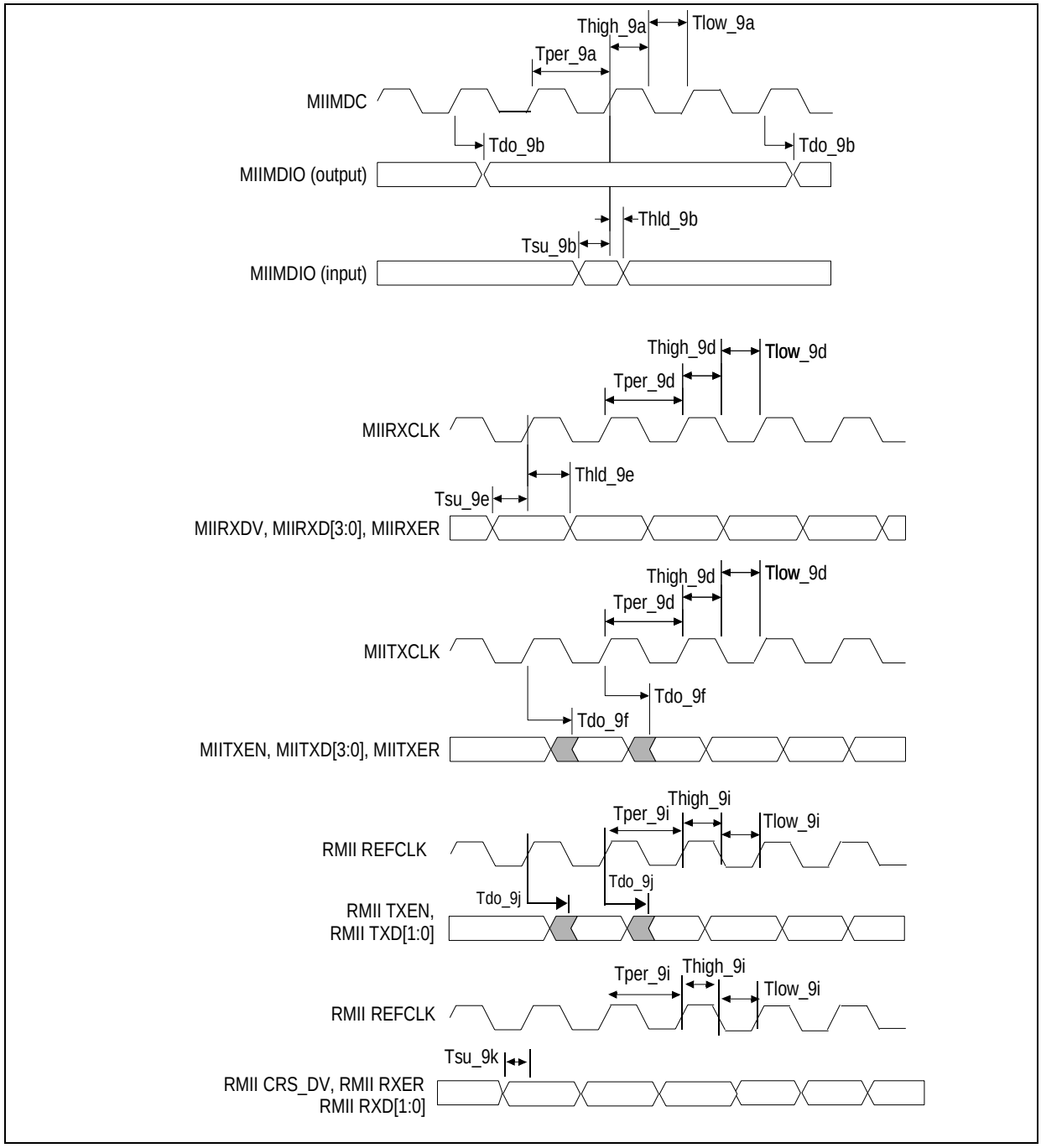


Figure 10 Ethernet AC Timing Waveform

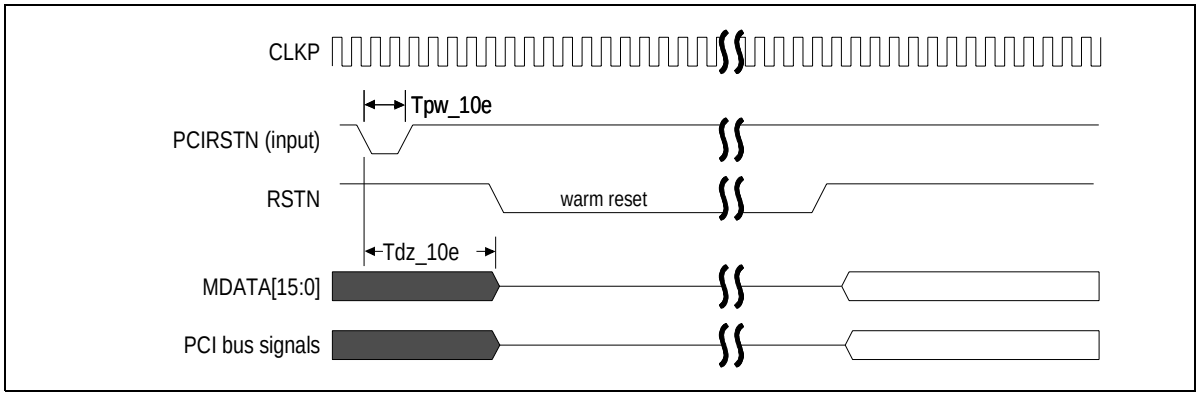


Figure 13 PCI AC Timing Waveform — PCI Reset in Satellite Mode

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
I²C[1]													
SCL	Frequency	none	0	100	0	100	0	100	0	100	kHz	100 KHz	See Figure 14.
	Thigh_12a, Tlow_12a		4.0	—	4.0	—	4.0	—	4.0	—	µs		
	Trise_12a		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	250	—	250	—	250	—	250	—	ns		
	Thld_12b		0	3.45	0	3.45	0	3.45	0	3.45	µs		
	Trise_12b		—	1000	—	1000	—	1000	—	1000	ns		
	Tfall_12b		—	300	—	300	—	300	—	300	ns		
Start or repeated start condition	Tsu_12c	SDA falling	4.7	—	4.7	—	4.7	—	4.7	—	µs		
	Thld_12c		4.0	—	4.0	—	4.0	—	4.0	—	µs		
Stop condition	Tsu_12d	SDA rising	4.0	—	4.0	—	4.0	—	4.0	—	µs		
Bus free time between a stop and start condition	Tdelay_12e		4.7	—	4.7	—	4.7	—	4.7	—	µs		
SCL	Frequency	none	0	400	0	400	0	400	0	400	kHz	400 KHz	
	Thigh_12a, Tlow_12a		0.6	—	0.6	—	0.6	—	0.6	—	µs		
	Trise_12a		—	300	—	300	—	300	—	300	ns		
	Tfall_12a		—	300	—	300	—	300	—	300	ns		
SDA	Tsu_12b	SCL rising	100	—	100	—	100	—	100	—	ns		
	Thld_12b		0	0.9	0	0.9	0	0.9	0	0.9	µs		
	Trise_12b		—	300	—	300	—	300	—	300	ns		
	Tfall_12ba		—	300	—	300	—	300	—	300	ns		

Table 11 I²C AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
SPI[1]													
SCK	Tper_15a	None	100	166667	100	166667	100	166667	100	166667	ns	SPI	See Figures 16, 17, and 18.
	Thigh_15a, Tlow_15a		40	83353	40	83353	40	83353	40	83353	ns	SPI	
SDI	Tsu_15b	SCK rising or falling	60	—	60	—	60	—	60	—	ns	SPI	See Figures 16, 17, and 18.
	Thld_15b		60	—	60	—	60	—	60	—	ns	SPI	
SDO	Tdo_15c	SCK rising or falling	0	60	0	60	0	60	0	60	ns	SPI	
SCK, SDI, SDO	Tpw_15e	None	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	2(ICLK)	—	ns	Bit I/O	

Table 13 SPI AC Timing Characteristics

1. In SPI mode, the SCK period and sampling edge are programmable. In PCI mode, the SCK period is fixed and the sampling edge is rising.

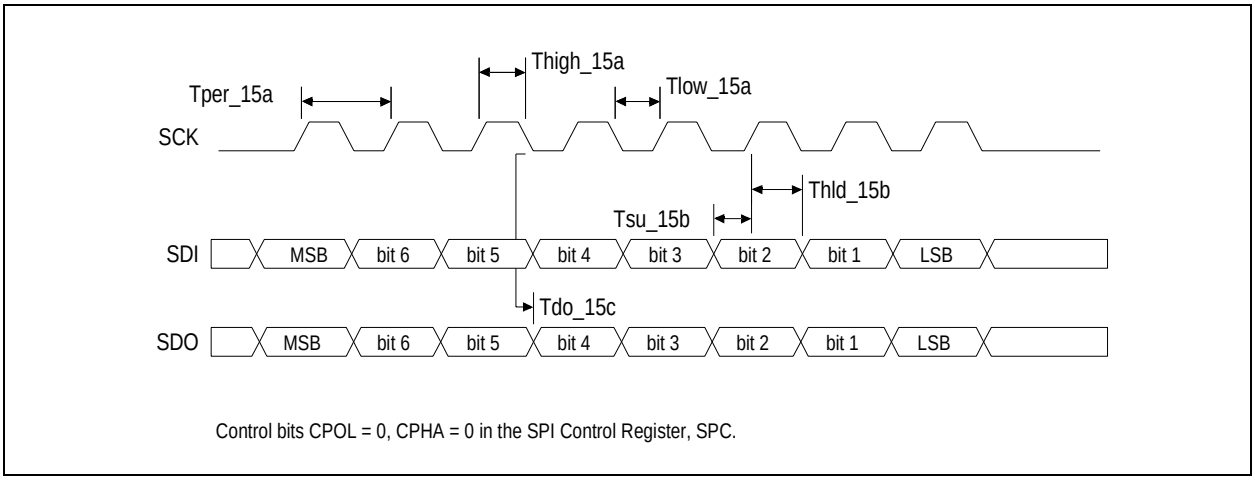


Figure 16 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 0

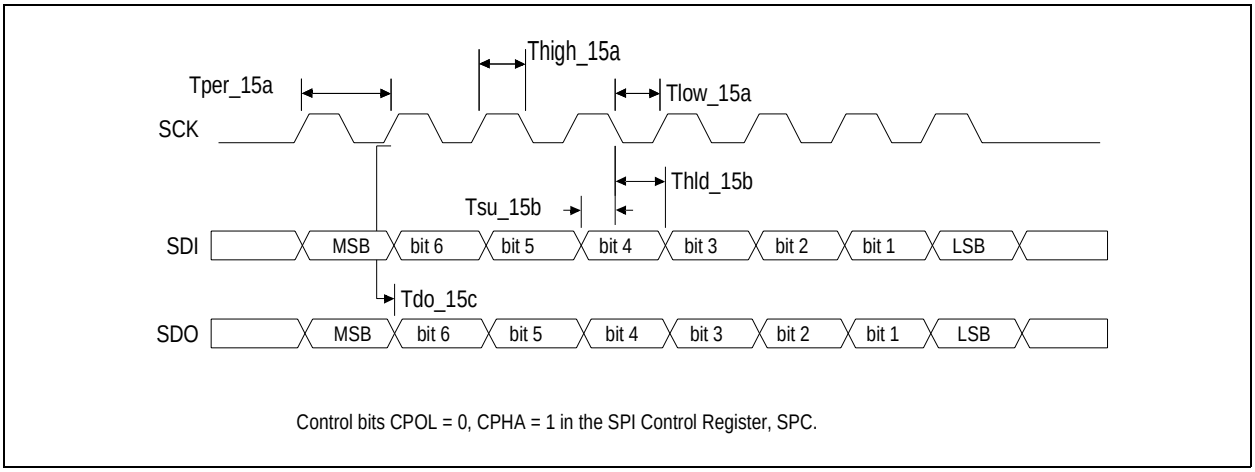


Figure 17 SPI AC Timing Waveform — Clock Polarity 0, Clock Phase 1

Power-on Sequence

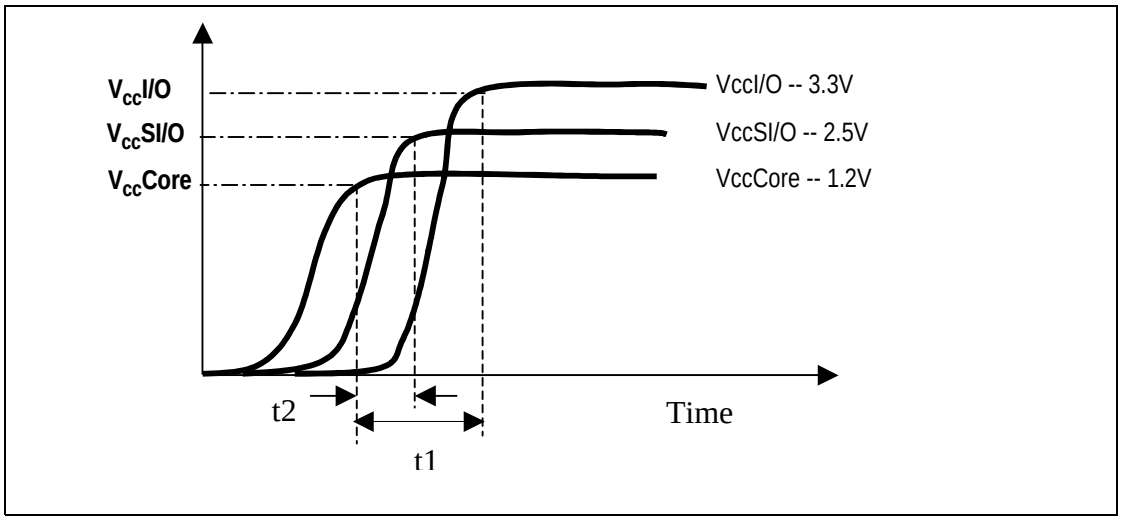
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

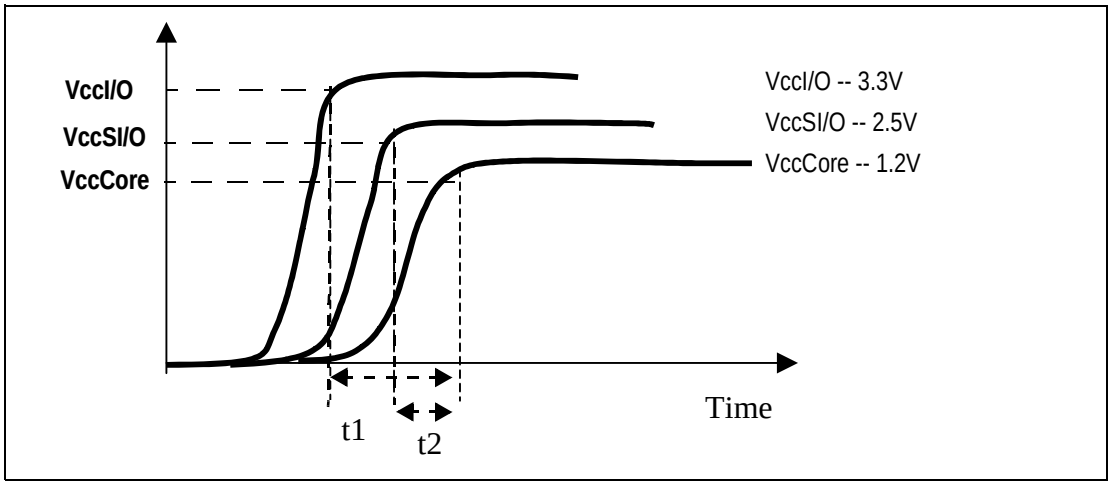
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

Absolute Maximum Ratings

Symbol	Parameter	Min[1]	Max[1]	Unit
V_{CC}I/O	I/O supply except for SSTL_2[2]	-0.6	4.0	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[2]	-0.6	4.0	V
V_{CC}Core	Core Supply Voltage	-0.6	2.0	V
V_{CC}PLL	PLL supply (digital)	-0.6	2.0	V
V_{CC}APLL	PLL supply (analog)	-0.6	4.0	V
VinI/O	I/O Input Voltage except for SSTL_2	-0.6	V_{cc}I/O+ 0.5	V
VinSI/O	I/O Input Voltage for SSTL_2	-0.6	V_{cc}SI/O+ 0.5	V
T_a Industrial	Ambient Operating Temperature	-40	+85	°C
T_a Commercial	Ambient Operating Temperature	0	+70	°C
T_s	Storage Temperature	-40	+125	°C

Table 19 Absolute Maximum Ratings

1. Functional and tested operating conditions are given in Table 15. Absolute maximum ratings are stress ratings only, and functional operation at the maximums is not guaranteed. Stresses beyond those listed may affect device reliability or cause permanent damage to the device.

2. SSTL_2 I/Os are used to connect to DDR SDRAM.

Package Pin-out — 256-BGA Signal Pinout for the RC32435

The following table lists the pin numbers, signal names, and number of alternate functions for the RC32435 device. Signal names ending with an "_n" or "n" are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	RWN		E1	MIIRXD[3]		J1	GPIO[3]	1	N1	PCIAD[29]	
A2	OEN		E2	MIIRXD[2]		J2	JTAG_TCK		N2	PCIAD[28]	
A3	CSN[2]		E3	MIITXD[0]		J3	GPIO[2]	1	N3	PCIAD[30]	
A4	CSN[0]		E4	MIITXD[1]		J4	EJTAG_TMS		N4	PCIAD[18]	
A5	MADDR[10]		E5	V_{cc} I/0		J5	V_{cc} CORE		N5	PCIREQN[1]	
A6	MDATA[6]		E6	V_{cc} I/0		J6	V_{ss}		N6	PCIREQN[2]	
A7	GPIO[7]	1	E7	V_{cc} I/0		J7	V_{ss}		N7	PCIIRDYN	
A8	GPIO[4]	1	E8	V_{cc} CORE		J8	V_{ss}		N8	PCILOCKN	
A9	MADDR[16]		E9	V_{cc} CORE		J9	V_{ss}		N9	PCIPERRN	
A10	MADDR[13]		E10	V_{cc} I/0		J10	V_{ss}		N10	PCIAD[15]	
A11	V_{ss} PLL		E11	V_{cc} DDR		J11	V_{cc} CORE		N11	PCIAD[11]	
A12	JTAG_TDI		E12	V_{cc} DDR		J12	V_{cc} CORE		N12	PCICBEN[0]	
A13	MADDR[9]		E13	DDRDATA[6]		J13	DDRCKN		N13	DDRADDR[5]	
A14	MADDR[7]		E14	DDRDATA[5]		J14	DDRVREF		N14	DDRADDR[4]	
A15	MADDR[5]		E15	DDRADDR[13]		J15	DDRCKP		N15	DDRADDR[3]	
A16	MADDR[2]		E16	DDRDATA[4]		J16	DDRDQS[0]		N16	DDRBA[0]	
B1	BOEN		F1	MIITXD[2]		K1	JTG_TDO		P1	PCIAD[27]	
B2	RSTN		F2	MIIRXCLK		K2	SCK		P2	PCIAD[26]	
B3	CSN[3]		F3	MIITXD[3]		K3	Reserved		P3	GPIO[10]	1
B4	CSN[1]		F4	MIITXENP		K4	SDO		P4	PCIAD[20]	
B5	MADDR[11]		F5	V_{cc} I/0		K5	V_{cc} I/0		P5	PCIREQN[3]	
B6	MDATA[1]		F6	V_{ss}		K6	V_{cc} I/0		P6	PCIREQN[0]	
B7	MDATA[4]		F7	V_{ss}		K7	V_{ss}		P7	PCIFRAMEN	
B8	GPIO[5]	1	F8	V_{ss}		K8	V_{ss}		P8	PCISTOPN	
B9	MADDR[17]		F9	V_{cc} CORE		K9	V_{ss}		P9	PCISERRN	
B10	MADDR[12]		F10	V_{ss}		K10	V_{ss}		P10	PCIAD[14]	
B11	V_{cc} PLL		F11	V_{ss}		K11	V_{ss}		P11	PCIAD[10]	
B12	V_{ss} APLL		F12	V_{cc} DDR		K12	V_{cc} DDR		P12	PCIAD[7]	
B13	MADDR[8]		F13	DDRDATA[9]		K13	DDRCKE		P13	PCIAD[4]	
B14	MADDR[6]		F14	DDRDATA[8]		K14	DDRADDR[11]		P14	DDRADDR[0]	
B15	MADDR[3]		F15	DDRDM[0]		K15	DDRADDR[10]		P15	DDRADDR[2]	
B16	MADDR[1]		F16	DDRDATA[7]		K16	DDRADDR[12]		P16	DDRCSN	
C1	EXTCLK		G1	MIIRXDV		L1	SDA		R1	PCIAD[25]	

Table 20 RC32435 Pinout (Part 1 of 2)

RC32435 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
A7	GPIO[7]	MADDR[25]	J3	GPIO[2]	U0RTSN
A8	GPIO[4]	MADDR[22]	L3	GPIO[8]	CPU
B8	GPIO[5]	MADDR[23]	M1	GPIO[12]	PCIGNTN[5]
C7	GPIO[6]	MADDR[24]	M3	GPIO[11]	PCIREQN[5]
H3	GPIO[0]	U0SOUT	M4	GPIO[9]	PCIREQN[4]
H4	GPIO[1]	U0SINP	P3	GPIO[10]	PCIGNTN[4]
J1	GPIO[3]	U0CTSN	T2	GPIO[13]	PCIMUINTN

Table 21 RC32435 Alternate Signal Functions

RC32435 Power Pins

V_{cc} I/O	V_{cc} DDR	V_{cc} Core	V_{cc} PLL	V_{cc} APLL
E5	E11	E8	B11	C12
E6	E12	E9		
E7	F12	F9		
E10	G12	H5		
F5	K12	H6		
G5	L12	H12		
K5	M11	J5		
K6	M12	J11		
L5		J12		
M5		L8		
M6		M8		
M7		M9		
M10				

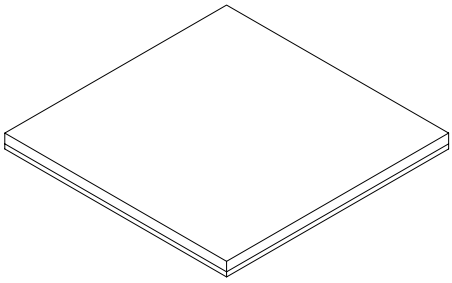
Table 22 RC32435 Power Pins

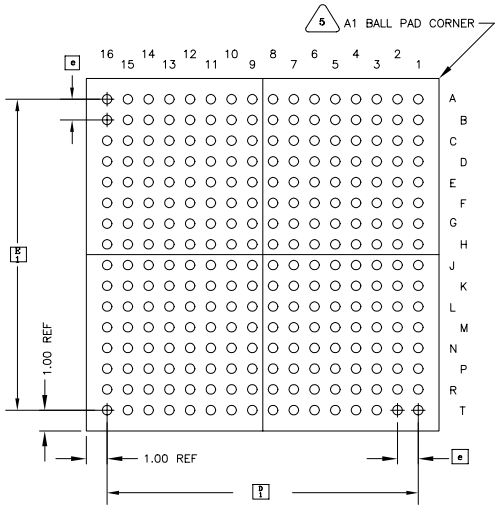
Signal Name	I/O Type	Location	Signal Category
MADDR[0]	O	C15	Memory and Peripheral Bus
MADDR[1]	O	B16	
MADDR[2]	O	A16	
MADDR[3]	O	B15	
MADDR[4]	O	C14	
MADDR[5]	O	A15	
MADDR[6]	O	B14	
MADDR[7]	O	A14	
MADDR[8]	O	B13	
MADDR[9]	O	A13	
MADDR[10]	O	A5	
MADDR[11]	O	B5	
MADDR[12]	O	B10	
MADDR[13]	O	A10	
MADDR[14]	O	C10	
MADDR[15]	O	D10	
MADDR[16]	O	A9	
MADDR[17]	O	B9	
MADDR[18]	O	C9	
MADDR[19]	O	D9	
MADDR[20]	O	D8	
MADDR[21]	O	C8	
MDATA[0]	I/O	D7	
MDATA[1]	I/O	B6	
MDATA[2]	I/O	D6	
MDATA[3]	I/O	C5	
MDATA[4]	I/O	B7	
MDATA[5]	I/O	C6	
MDATA[6]	I/O	A6	
MDATA[7]	I/O	D5	

Table 24 RC32435 Alphabetical Signal List (Part 4 of 7)

RC32435 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	





BOTTOM VIEW
256 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "D" DIRECTION.
   "ME" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "E" DIRECTION.
4. "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–192 VARIATION AAF–1
   EXCEPTIONS:
   b MIN=0.41 NOM=0.46 MAX=0.51

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: X.X ±0.10, X.XX ±0.05, X.XXX ±0.00
ANGULAR: ±1°

APPROVALS	DATE
DRAWN BX	06/09/00
CHECKED	

Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727–6116 FAX (408) 492–8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC–4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 2 OF 2