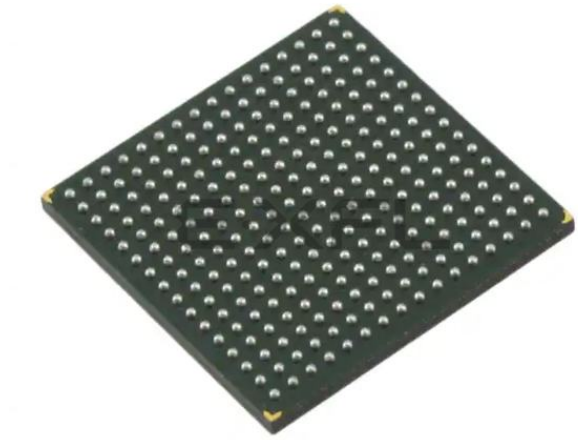

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Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	0°C ~ 70°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h435-300bcg

Pin Description Table

The following table lists the functions of the pins provided on the RC32435. Some of the functions listed may be multiplexed onto the same pin.

The active polarity of a signal is defined using a suffix. Signals ending with an “N” are defined as being active, or asserted, when at a logic zero (low) level. All other signals (including clocks, buses, and select lines) will be interpreted as being active, or asserted, when at a logic one (high) level.

Signal	Type	Name/Description
Memory and Peripheral Bus		
BDIRN	O	**External Buffer Direction.** Controls the direction of the external data bus buffer for the memory and peripheral bus. If the RC32435 memory and peripheral bus is connected to the A side of a transceiver, such as an IDT74FCT245, then this pin may be directly connected to the direction control (e.g., BDIR) pin of the transceiver.
BOEN	O	**External Buffer Enable.** This signal provides an output enable control for an external buffer on the memory and peripheral data bus.
WEN	O	**Write Enables.** This signal is the memory and peripheral bus write enable signal.
CSN[3:0]	O	**Chip Selects.** These signals are used to select an external device on the memory and peripheral bus.
MADDR[21:0]	O	**Address Bus.** 22-bit memory and peripheral bus address bus. MADDR[25:22] are available as GPIO alternate functions.
MDATA[7:0]	I/O	**Data Bus.** 8-bit memory and peripheral data bus. During a cold reset, these pins function as inputs that are used to load the boot configuration vector.
OEN	O	**Output Enable.** This signal is asserted when data should be driven by an external device on the memory and peripheral bus.
RWN	O	**Read Write.** This signal indicates whether the transaction on the memory and peripheral bus is a read transaction or a write transaction. A high level indicates a read from an external device. A low level indicates a write to an external device.
WAITACKN	I	**Wait or Transfer Acknowledge.** When configured as wait, this signal is asserted during a memory and peripheral bus transaction to extend the bus cycle. When configured as a transfer acknowledge, this signal is asserted during a transaction to signal the completion of the transaction.
DDR Bus		
DDRADDR[13:0]	O	**DDR Address Bus.** 14-bit multiplexed DDR address bus. This bus is used to transfer the addresses to the DDR devices.
DDRBA[1:0]	O	**DDR Bank Address.** These signals are used to transfer the bank address to the DDRs.
DDRCASN	O	**DDR Column Address Strobe.** This signal is asserted during DDR transactions.
DDRCKE	O	**DDR Clock Enable.** The DDR clock enable signal is asserted during normal DDR operation. This signal is negated following a cold reset or during a power down operation.
DDRCKN	O	**DDR Negative DDR clock.** This signal is the negative clock of the differential DDR clock pair.

Table 1 Pin Description (Part 1 of 6)

Signal	Type	Name/Description
DDRCKP	O	**DDR Positive DDR clock.** This signal is the positive clock of the differential DDR clock pair.
DDRCSN	O	**DDR Chip Selects.** This active low signal is used to select DDR device(s) on the DDR bus.
DDRDATA[15:0]	I/O	**DDR Data Bus.** 16-bit DDR data bus is used to transfer data between the RC32435 and the DDR devices. Data is transferred on both edges of the clock.
DDRDM[1:0]	O	**DDR Data Write Enables.** Byte data write enables are used to enable specific byte lanes during DDR writes. DDRDM[0] corresponds to DDRDATA[7:0] DDRDM[1] corresponds to DDRDATA[15:8]
DDRDQS[1:0]	I/O	**DDR Data Strobes.** DDR byte data strobes are used to clock data between DDR devices and the RC32435. These strobes are inputs during DDR reads and outputs during DDR writes. DDRDQS[0] corresponds to DDRDATA[7:0] DDRDQS[1] corresponds to DDRDATA[15:8]
DDRRASN	O	**DDR Row Address Strobe.** The DDR row address strobe is asserted during DDR transactions.
DDRVREF	I	**DDR Voltage Reference.** SSTL_2 DDR voltage reference is generated by an external source.
DDRWEN	O	**DDR Write Enable.** DDR write enable is asserted during DDR write transactions.
PCI Bus		
PCIAD[31:0]	I/O	**PCI Multiplexed Address/Data Bus**. Address is driven by a bus master during initial PCIFRAMEN assertion. Data is then driven by the bus master during writes or by the bus target during reads.
PCICBEN[3:0]	I/O	**PCI Multiplexed Command/Byte Enable Bus**. PCI commands are driven by the bus master during the initial PCIFRAMEN assertion. Byte enable signals are driven by the bus master during subsequent data phase(s).
PCICLK	I	**PCI Clock**. Clock used for all PCI bus transactions.
PCIDEVSELN	I/O	**PCI Device Select**. This signal is driven by a bus target to indicate that the target has decoded the address as one of its own address spaces.
PCIFRAMEN	I/O	**PCI Frame**. Driven by a bus master. Assertion indicates the beginning of a bus transaction. Negation indicates the last data.
PCIGNTN[3:0]	I/O	**PCI Bus Grant**. **In PCI host mode with internal arbiter:** The assertion of these signals indicates to the agent that the internal RC32435 arbiter has granted the agent access to the PCI bus. **In PCI host mode with external arbiter:** PCIGNTN[0]: asserted by an external arbiter to indicate to the RC32435 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high. **In PCI satellite mode:** PCIGNTN[0]: This signal is asserted by an external arbiter to indicate to the RC32435 that access to the PCI bus has been granted. PCIGNTN[3:1]: unused and driven high.
PCIIRDYN	I/O	**PCI Initiator Ready**. Driven by the bus master to indicate that the current datum can complete.

Table 1 Pin Description (Part 2 of 6)

Signal	Type	Name/Description
GPIO[4]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[22] Alternate function: Memory and peripheral bus address.
GPIO[5]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[23] Alternate function: Memory and peripheral bus address.
GPIO[6]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[24] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32435 User Manual).
GPIO[7]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: MADDR[25] Alternate function: Memory and peripheral bus address. The value of this pin may be used as a counter timer clock input (see Counter Timer Clock Select Register in Chapter 14, Counter/Timers, of the RC32435 User Manual).
GPIO[8]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: CPU Alternate function: CPU or DMA debug output pin.
GPIO[9]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[4] Alternate function: PCI Request 4.
GPIO[10]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[4] Alternate function: PCI Grant 4.
GPIO[11]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIREQN[5] Alternate function: PCI Request 5.
GPIO[12]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIGNTN[5] Alternate function: PCI Grant 5.
GPIO[13]	I/O	**General Purpose I/O.** This pin can be configured as a general purpose I/O pin. Alternate function pin name: PCIMUINTN Alternate function: PCI Messaging unit interrupt output.
SPI Interface		
SCK	I/O	**Serial Clock**. This signal is used as the serial clock output. This pin may be used as a bit input/output port.

Table 1 Pin Description (Part 4 of 6)

Signal	Type	Name/Description
SDI	I/O	**Serial Data Input**. This signal is used to shift in serial data. This pin may be used as a bit input/output port.
SDO	I/O	**Serial Data Output**. This signal is used shift out serial data.
I^2C Bus Interface		
SCL	I/O	**I^2C Clock.** I^2C-bus clock.
SDA	I/O	**I^2C Data Bus.** I^2C-bus data bus.
Ethernet Interfaces		
MIICL	I	**Ethernet MII Collision Detected.** This signal is asserted by the ethernet PHY when a collision is detected.
MIICRS	I	**Ethernet MII Carrier Sense.** This signal is asserted by the ethernet PHY when either the transmit or receive medium is not idle.
MIIRXCLK	I	**Ethernet MII Receive Clock.** This clock is a continuous clock that provides a timing reference for the reception of data. This pin also functions as the RMII REF_CLK input.
MIIRXD[3:0]	I	**Ethernet MII Receive Data.** This nibble wide data bus contains the data received by the ethernet PHY. This pin also functions as the RMII RXD[1:0] input.
MIIRXDV	I	**Ethernet MII Receive Data Valid.** The assertion of this signal indicates that valid receive data is in the MII receive data bus. This pin also functions as the RMII CRS_DV input.
MIIRXER	I	**Ethernet MII Receive Error.** The assertion of this signal indicates that an error was detected somewhere in the ethernet frame currently being sent in the MII receive data bus. This pin also functions as the RMII RX_ER input.
MIITXCLK	I	**Ethernet MII Transmit Clock.** This clock is a continuous clock that provides a timing reference for the transfer of transmit data.
MIITXD[3:0]	O	**Ethernet MII Transmit Data.** This nibble wide data bus contains the data to be transmitted. This pin also functions as the RMII TXD[1:0] output.
MIITXENP	O	**Ethernet MII Transmit Enable.** The assertion of this signal indicates that data is present on the MII for transmission. This pin also functions as the RMII TX_EN output.
MIITXER	O	**Ethernet MII Transmit Coding Error.** When this signal is asserted together with MIITXENP, the ethernet PHY will transmit symbols which are not valid data or delimiters.
MIIMDC	O	**MII Management Data Clock.** This signal is used as a timing reference for transmission of data on the management interface.
MIIMDIO	I/O	**MII Management Data.** This bidirectional signal is used to transfer data between the station management entity and the ethernet PHY.
EJTAG / JTAG		
JTAG_TMS	I	**JTAG Mode**. The value on this signal controls the test mode select of the boundary scan logic or JTAG Controller. When using the EJTAG debug interface, this pin should be left disconnected (since there is an internal pull-up) or driven high.

Table 1 Pin Description (Part 5 of 6)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Serial Peripheral Interface	SCK	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	High Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Use a 2.2K pull-up resistor for I2C pins.

AC Timing Definitions

Below are examples of the AC timing characteristics used throughout this document.

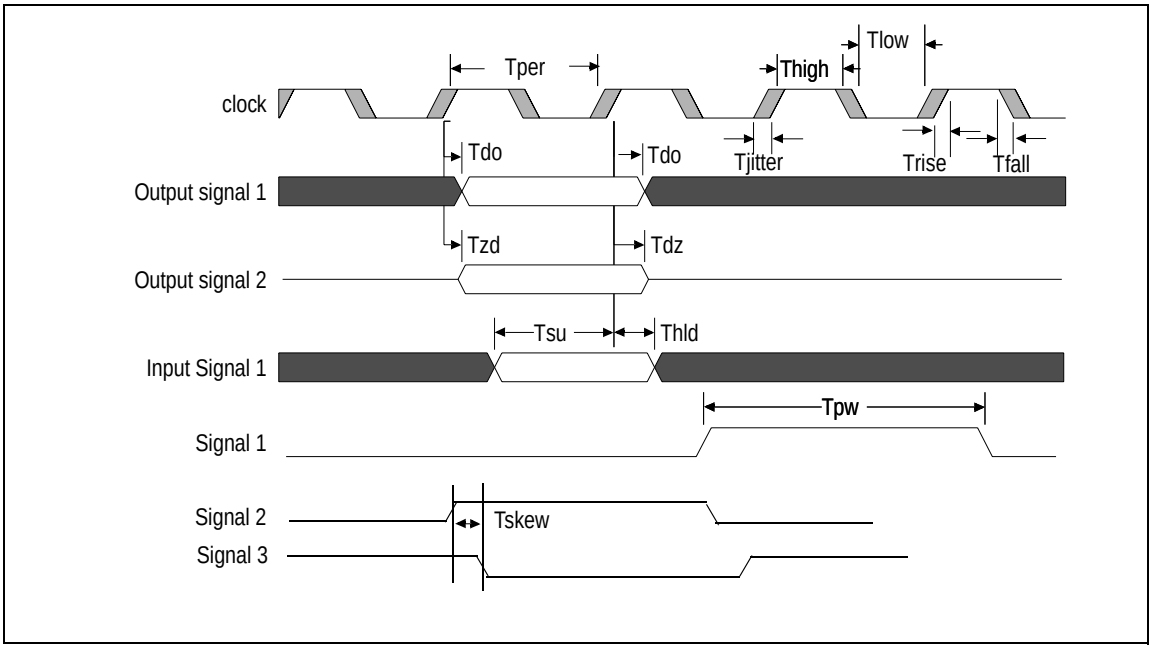
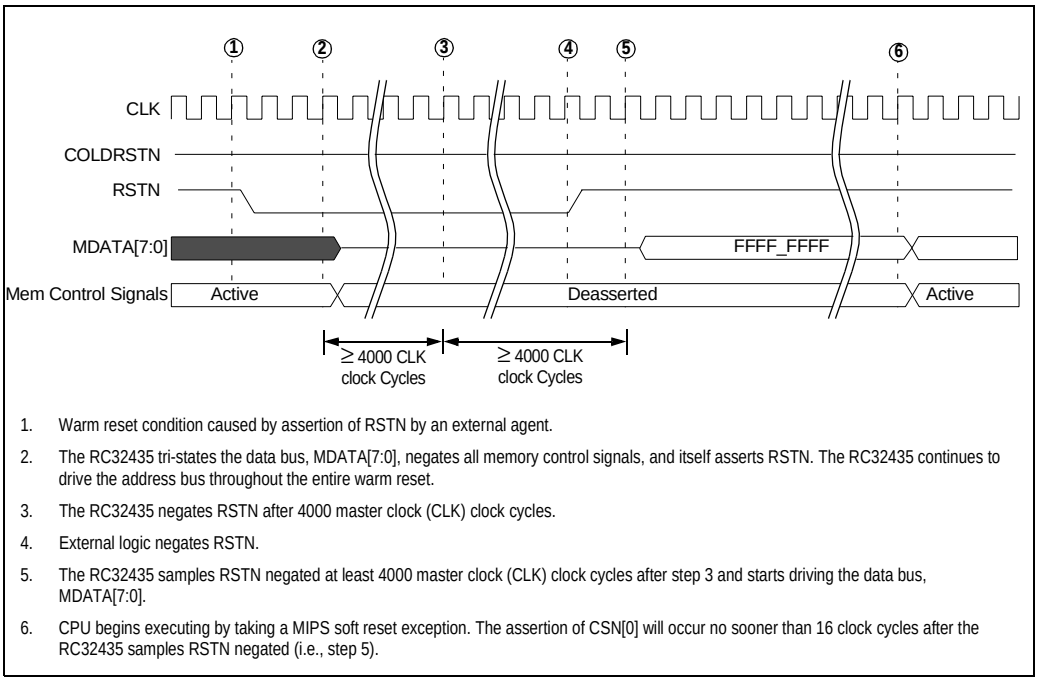


Figure 2 AC Timing Definitions Waveform

Symbol	Definition
Tper	Clock period.
Tlow	Clock low. Amount of time the clock is low in one clock period.
Thigh	Clock high. Amount of time the clock is high in one clock period.
Trise	Rise time. Low to high transition time.
Tfall	Fall time. High to low transition time.
Tjitter	Jitter. Amount of time the reference clock (or signal) edge can vary on either the rising or falling edges.
Tdo	Data out. Amount of time after the reference clock edge that the output will become valid. The minimum time represents the data output hold. The maximum time represents the earliest time the designer can use the data.
Tzd	Z state to data valid. Amount of time after the reference clock edge that the tri-stated output takes to become valid.
Tdz	Data valid to Z state. Amount of time after the reference clock edge that the valid output takes to become tri-stated.
Tsu	Input set-up. Amount of time before the reference clock edge that the input must be valid.
Thld	Input hold. Amount of time after the reference clock edge that the input must remain valid.
Tpw	Pulse width. Amount of time the input or output is active for asynchronous signals.
Tslew	Slew rate. The rise or fall rate for a signal to go from a high to low, or low to high.
X(clock)	Timing value. This notation represents a value of 'X' multiplied by the clock time period of the specified clock. Using 5(CLK) as an example: X = 5 and the oscillator clock (CLK) = 25MHz, then the timing value is 200.
Tskew	Skew. The amount of time two signal edges deviate from one another.

Table 4 AC Timing Definitions



1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32435 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32435 continues to drive the address bus throughout the entire warm reset.
3. The RC32435 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32435 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32435 samples RSTN negated (i.e., step 5).

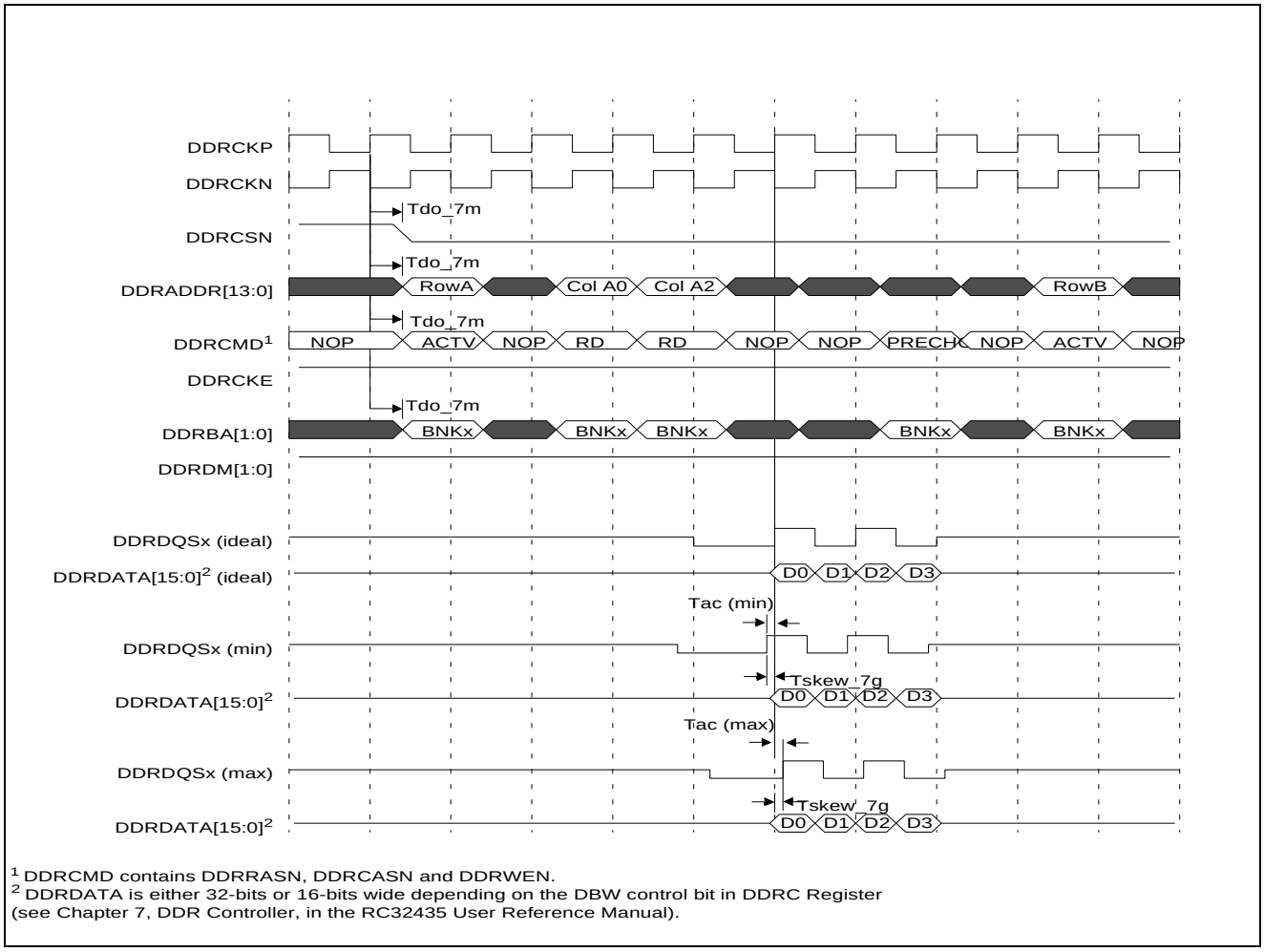
Figure 5 Externally Initiated Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

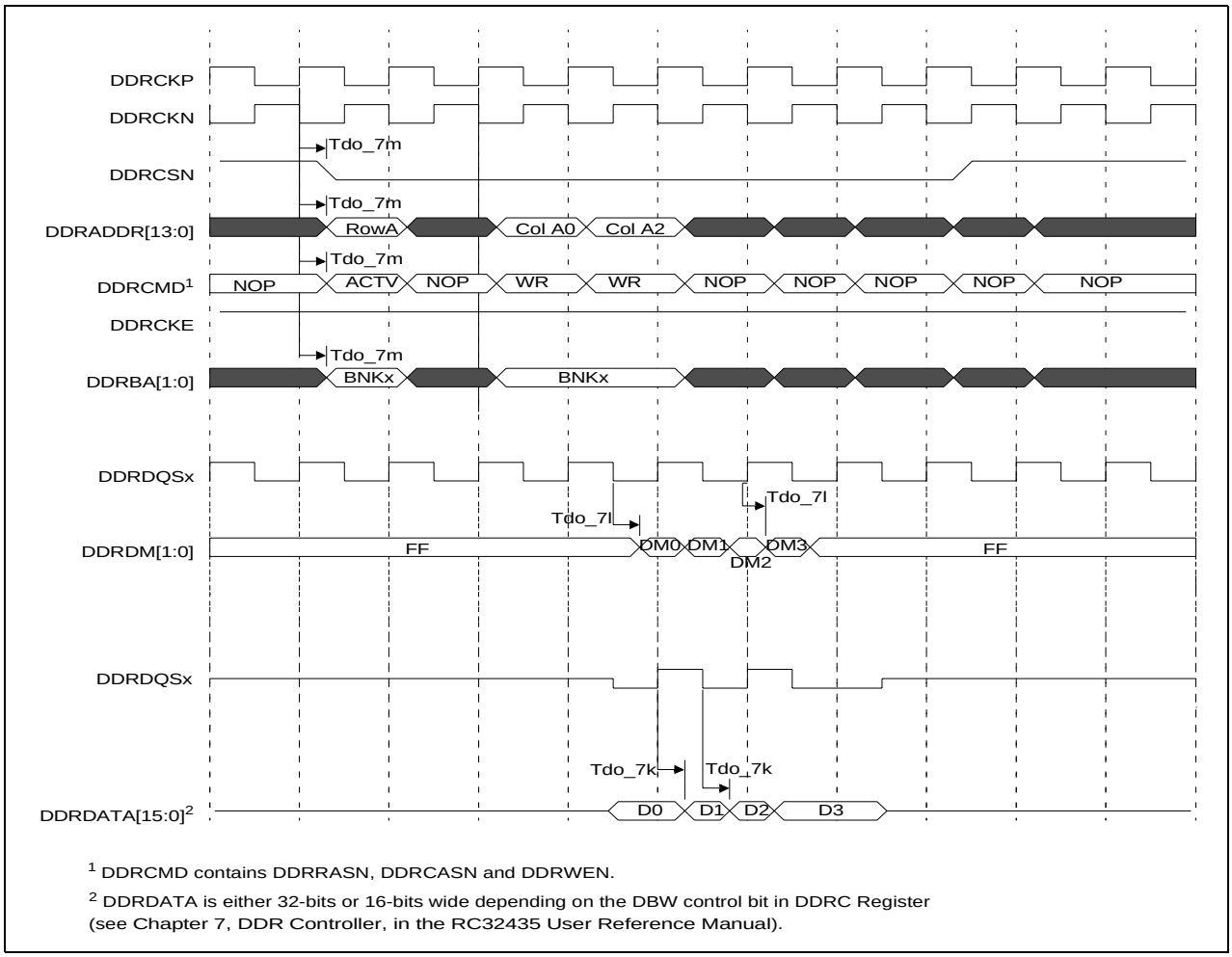
1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32435 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.
[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 6 DDR SDRAM AC Timing Waveform - SDRAM Read Access



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8a[2]		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8b[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Ethernet													
MIIMDC	Tper_9a	None	30.0	—	30.0	—	30.0	—	30.0	—	ns		See Figure 10.
	Thigh_9a, Tlow_9a		12.0	—	12.0	—	12.0	—	12.0	—	ns		
MIIMDIO	Tsu_9b	MIIMDC rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9b		0.0	—	0.0	—	0.0	—	0.0	—	ns		
	Tdo_9b[1]		10	300	10	300	10	300	10	300	ns		
Ethernet — MII Mode													
MIIRXCLK, MIITXCLK[2]	Tper_9c	None	399.96	400.4	399.96	400.4	399.96	400.4	399.96	400.4	ns	10 Mbps	See Figure 10.
	Thigh_9c, Tlow_9c		140	260	140	260	140	260	140	260	ns		
	Trise_9c, Tfall_9c		—	3.0	—	3.0	—	3.0	—	3.0	ns		
MIIRXCLK, MIITXCLK[2]	Tper_9d	None	39.9	40.0	39.9	40.0	39.9	40.0	39.9	40.0	ns	100 Mbps	
	Thigh_9d, Tlow_9d		14.0	26.0	14.0	26.0	14.0	26.0	14.0	26.0	ns		
	Trise_9d, Tfall_9d		—	2.0	—	2.0	—	2.0	—	2.0	ns		
MIIRXD[3:0], MIIRXDV, MIIRXER	Tsu_9e	MIIxRXCLK rising	10.0	—	10.0	—	10.0	—	10.0	—	ns		
	Thld_9e		10.0	—	10.0	—	10.0	—	10.0	—	ns		
MIITXD[3:0], MIITXENP, MIITXER	Tdo_9f	MIIxTXCLK rising	0.0	25.0	0.0	25.0	0.0	25.0	0.0	25.0	ns		
Ethernet — RMII Mode													
RMIIREFCLK	Tper_9i	None	19.9	20.1	19.9	20.1	19.9	20.1	19.9	20.1	ns		See Figure 10.
	Thigh_9i, Tlow_9i		7.0	13.0	7.0	13.0	7.0	13.0	7.0	13.0	ns		
RMIITXEN, RMIITXD[1:0]	Tdo_9j	MIIRXCLK rising	2.0	—	2.0	—	2.0	—	2.0	—	ns		
RMIICRSDV, RMIIRXER, RMIIRXD[1:0]	Tsu_9k		5.5	14.5	5.5	14.5	5.5	14.5	5.5	14.5	ns		

Table 9 Ethernet AC Timing Characteristics

1. The values for this symbol were determined by calculation, not by testing.

2. The ethernet clock (MIIRXCLK and MIITXCLK) frequency must be equal to or less than 1/2 ICLK (MIIRXCLK and MIITXCLK <= 1/2(ICLK)).

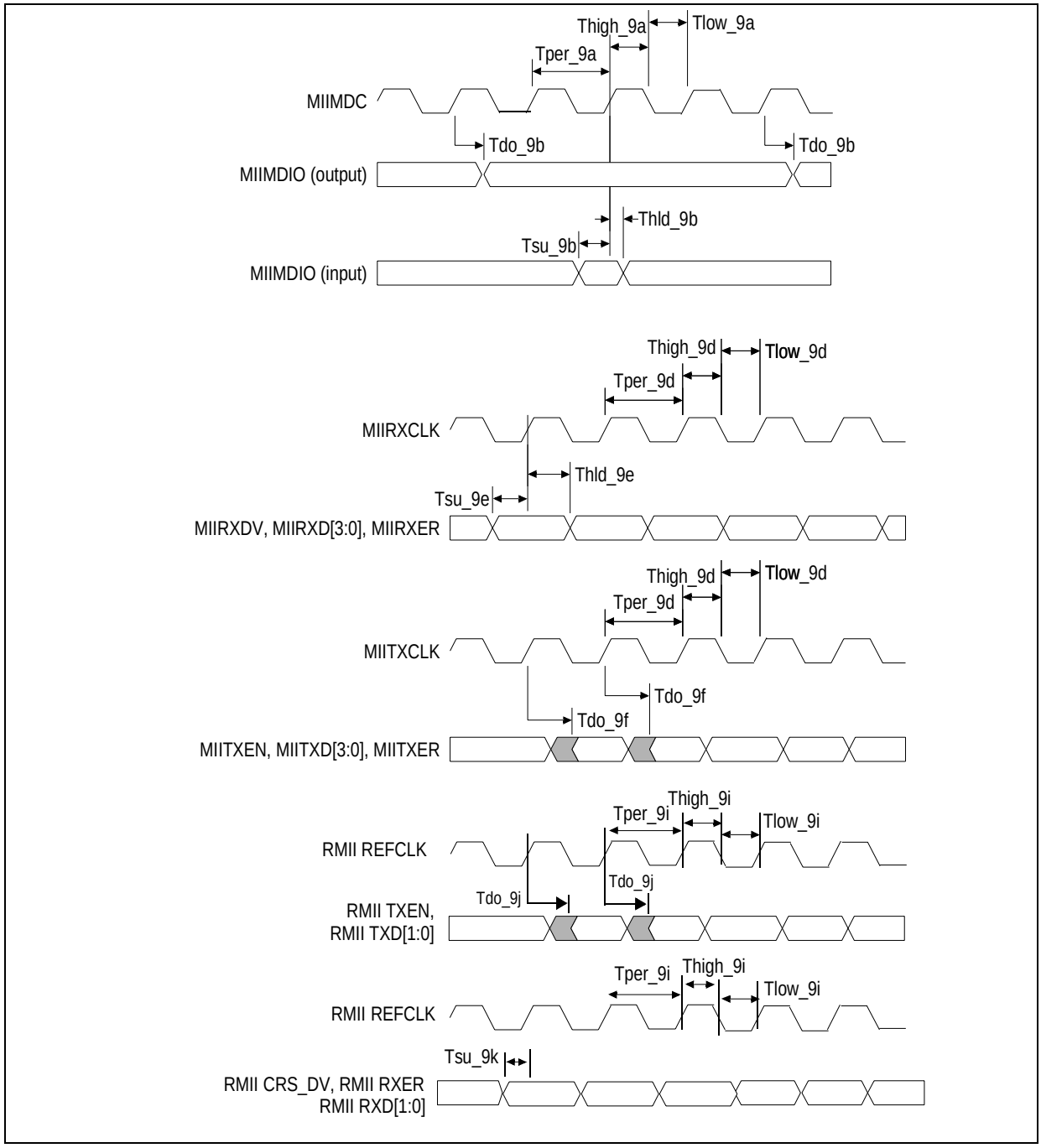


Figure 10 Ethernet AC Timing Waveform

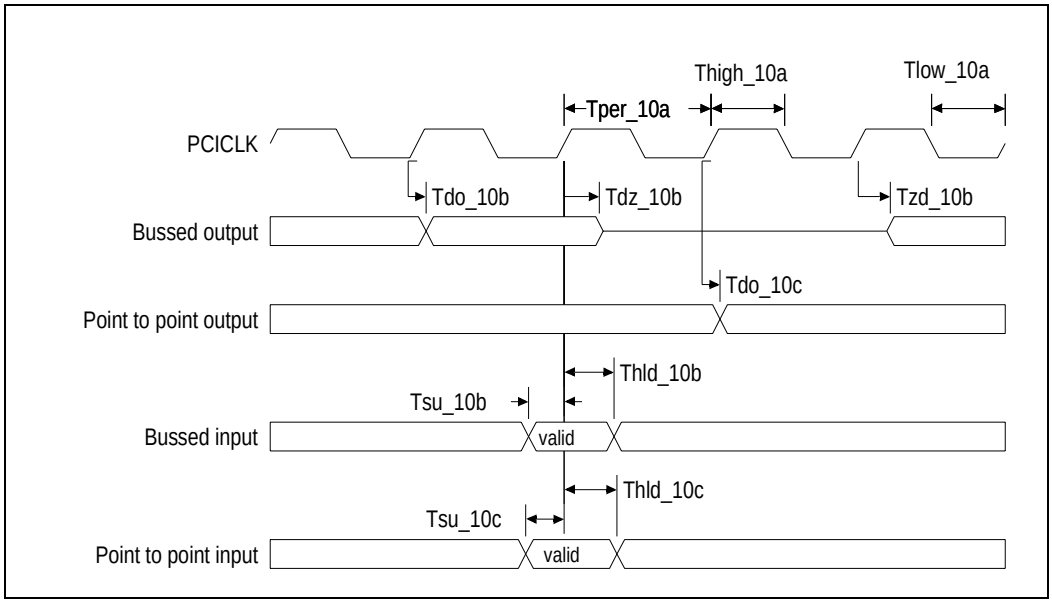
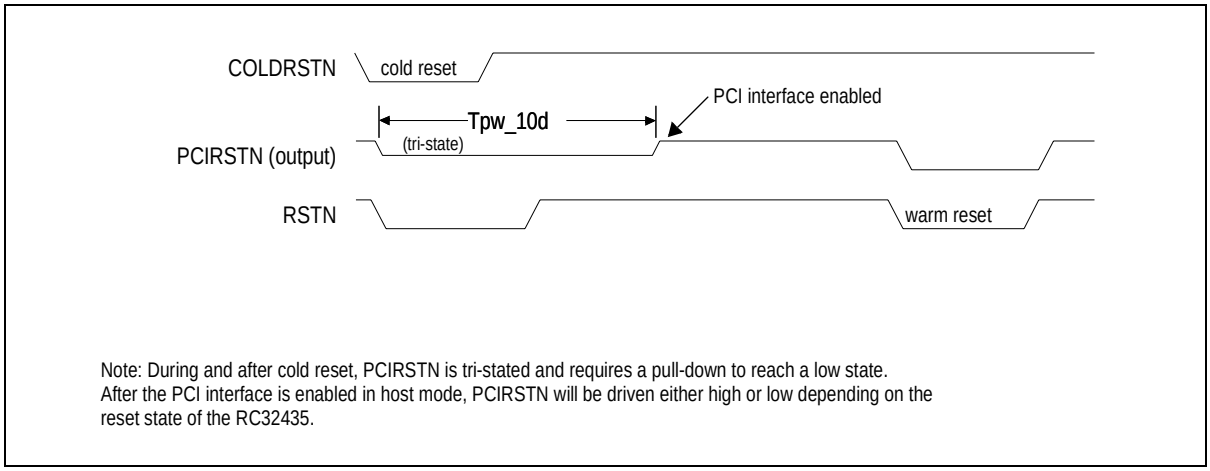


Figure 11 PCI AC Timing Waveform



Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32435.

Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode

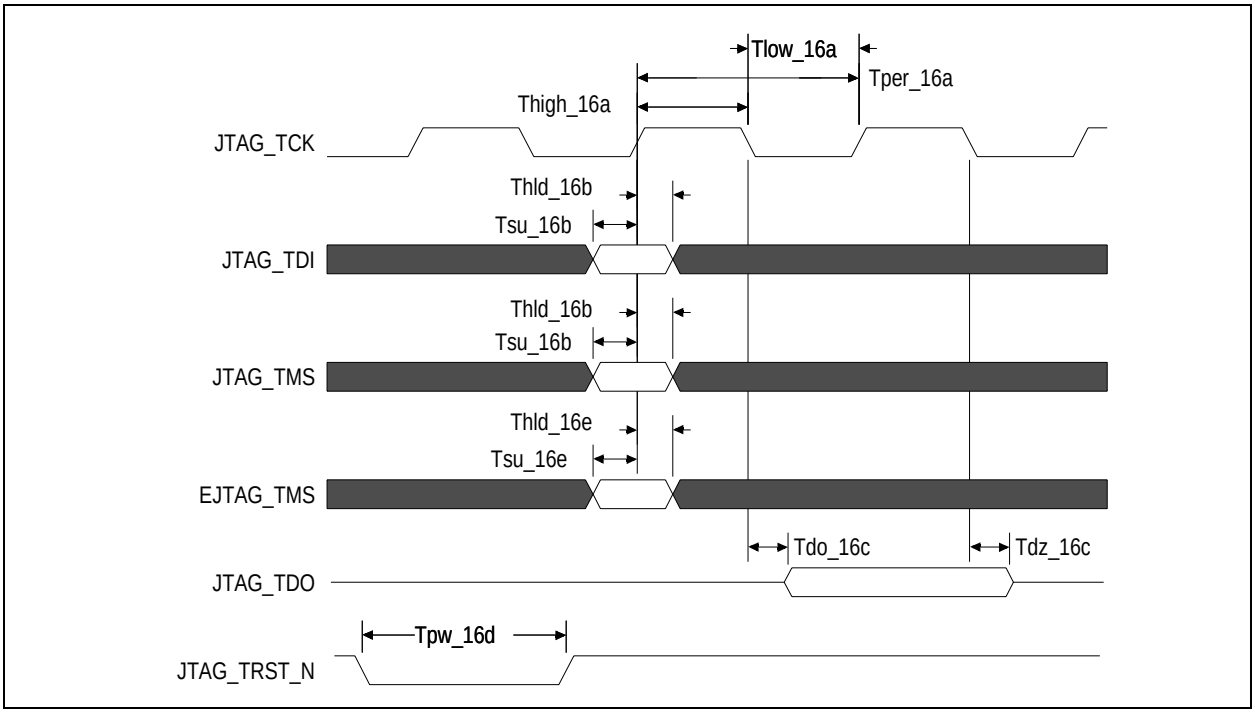


Figure 19 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32435 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 20 shows the electrical connection of the EJTAG probe target system connector.

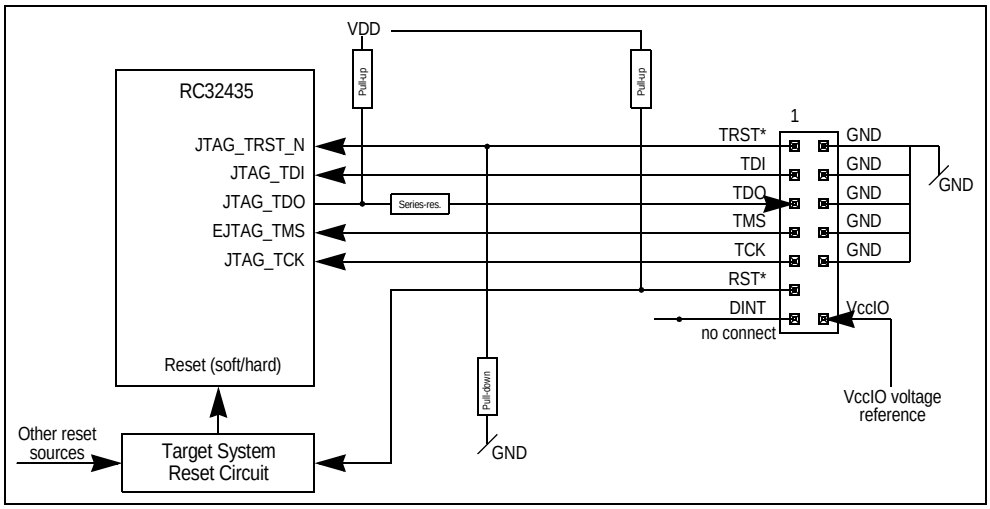


Figure 20 Target System Electrical EJTAG Connection

DC Electrical Characteristics

Values based on systems running at recommended supply voltages, as shown in Table 15.

Note: See Table 2, Pin Characteristics, for a complete I/O listing.

I/O Type	Para-meter	Min.	Typical	Max.	Unit	Conditions
LOW Drive Output	I_{OL}	—	14.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-12.0	—	mA	V_{OH} = 1.5V
HIGH Drive Output	I_{OL}	—	41.0	—	mA	V_{OL} = 0.4V
	I_{OH}	—	-42.0	—	mA	V_{OH} = 1.5V
Schmitt Trigger Input (STI)	V_{IL}	-0.3	—	0.8	V	—
	V_{IH}	2.0	—	V_{cc}I/O + 0.5	V	—
SSTL_2 (for DDR SDRAM)	I_{OL}	7.6	—	—	mA	V_{OL} = 0.5V
	I_{OH}	-7.6	—	—	mA	V_{OH} = 1.76V
	V_{IL}	-0.3	—	0.5(V_{cc}SI/O) - 0.18	V	
	V_{IH}	0.5(V_{cc}SI/O) + 0.18	—	V_{cc}SI/O + 0.3	V	
PCI	I_{OH}(AC) Switching	-12(V_{cc}I/O)	—	—	mA	0 < V_{OUT} < 0.3(V_{cc}I/O)
		-17.1(V_{cc}I/O - V_{OUT})	—	—	mA	0.3(V_{cc}I/O) < V_{OUT} < 0.9(V_{cc}I/O)
		—	—	-32(V_{cc}I/O)	—	0.7(V_{cc}I/O)
		16(V_{cc}I/O)	—	See Note 1	mA	0.7(V_{cc}I/O) < V_{OUT} < V_{cc}I/O
	I_{OL}(AC) Switching	+16(V_{cc}I/O)	—	—	mA	V_{cc}I/O > V_{OUT} > 0.6(V_{cc}I/O)
		+26.7(V_{OUT})	—	—	mA	0.6(V_{cc}I/O) > V_{OUT} > 0.1(V_{cc}I/O)
		—	—	+38(V_{cc}I/O)	mA	V_{OUT} = 0.18(V_{cc}I/O)
		—	—	See Note 2	mA	0.18(V_{cc}I/O) > V_{OUT} > 0
	V_{IL}	-0.3	—	0.3(V_{cc}I/O)	V	
	V_{IH}	0.5(V_{cc}I/O)	—	5.5	V	
Capacitance	C_{IN}	—	—	10.5	pF	—
Leakage	Inputs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ W/O}$ Pull-ups/ downs	—	—	± 10	µA	Vcc (max)
	$I/O_{LEAK\ WITH}$ Pull-ups/ downs	—	—	± 80	µA	Vcc (max)

Table 18 DC Electrical Characteristics

Note 1: $I_{OH}(AC)\ max = (98/V_{CC}I/O) * (V_{OUT} - V_{CC}I/O) * (V_{OUT} + 0.4V_{CC}I/O)$

Note 2: $I_{OL}(AC)\ max = (256/V_{CC}I/O) * V_{OUT} * (V_{CC}I/O - V_{OUT})$

Package Pin-out — 256-BGA Signal Pinout for the RC32435

The following table lists the pin numbers, signal names, and number of alternate functions for the RC32435 device. Signal names ending with an "_n" or "n" are active when low.

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
A1	RWN		E1	MIIRXD[3]		J1	GPIO[3]	1	N1	PCIAD[29]	
A2	OEN		E2	MIIRXD[2]		J2	JTAG_TCK		N2	PCIAD[28]	
A3	CSN[2]		E3	MIITXD[0]		J3	GPIO[2]	1	N3	PCIAD[30]	
A4	CSN[0]		E4	MIITXD[1]		J4	EJTAG_TMS		N4	PCIAD[18]	
A5	MADDR[10]		E5	V_{cc} I/0		J5	V_{cc} CORE		N5	PCIREQN[1]	
A6	MDATA[6]		E6	V_{cc} I/0		J6	V_{ss}		N6	PCIREQN[2]	
A7	GPIO[7]	1	E7	V_{cc} I/0		J7	V_{ss}		N7	PCIIRDYN	
A8	GPIO[4]	1	E8	V_{cc} CORE		J8	V_{ss}		N8	PCILOCKN	
A9	MADDR[16]		E9	V_{cc} CORE		J9	V_{ss}		N9	PCIPERRN	
A10	MADDR[13]		E10	V_{cc} I/0		J10	V_{ss}		N10	PCIAD[15]	
A11	V_{ss} PLL		E11	V_{cc} DDR		J11	V_{cc} CORE		N11	PCIAD[11]	
A12	JTAG_TDI		E12	V_{cc} DDR		J12	V_{cc} CORE		N12	PCICBEN[0]	
A13	MADDR[9]		E13	DDRDATA[6]		J13	DDRCKN		N13	DDRADDR[5]	
A14	MADDR[7]		E14	DDRDATA[5]		J14	DDRVREF		N14	DDRADDR[4]	
A15	MADDR[5]		E15	DDRADDR[13]		J15	DDRCKP		N15	DDRADDR[3]	
A16	MADDR[2]		E16	DDRDATA[4]		J16	DDRDQS[0]		N16	DDRBA[0]	
B1	BOEN		F1	MIITXD[2]		K1	JTG_TDO		P1	PCIAD[27]	
B2	RSTN		F2	MIIRXCLK		K2	SCK		P2	PCIAD[26]	
B3	CSN[3]		F3	MIITXD[3]		K3	Reserved		P3	GPIO[10]	1
B4	CSN[1]		F4	MIITXENP		K4	SDO		P4	PCIAD[20]	
B5	MADDR[11]		F5	V_{cc} I/0		K5	V_{cc} I/0		P5	PCIREQN[3]	
B6	MDATA[1]		F6	V_{ss}		K6	V_{cc} I/0		P6	PCIREQN[0]	
B7	MDATA[4]		F7	V_{ss}		K7	V_{ss}		P7	PCIFRAMEN	
B8	GPIO[5]	1	F8	V_{ss}		K8	V_{ss}		P8	PCISTOPN	
B9	MADDR[17]		F9	V_{cc} CORE		K9	V_{ss}		P9	PCISERRN	
B10	MADDR[12]		F10	V_{ss}		K10	V_{ss}		P10	PCIAD[14]	
B11	V_{cc} PLL		F11	V_{ss}		K11	V_{ss}		P11	PCIAD[10]	
B12	V_{ss} APLL		F12	V_{cc} DDR		K12	V_{cc} DDR		P12	PCIAD[7]	
B13	MADDR[8]		F13	DDRDATA[9]		K13	DDRCKE		P13	PCIAD[4]	
B14	MADDR[6]		F14	DDRDATA[8]		K14	DDRADDR[11]		P14	DDRADDR[0]	
B15	MADDR[3]		F15	DDRDM[0]		K15	DDRADDR[10]		P15	DDRADDR[2]	
B16	MADDR[1]		F16	DDRDATA[7]		K16	DDRADDR[12]		P16	DDRCSN	
C1	EXTCLK		G1	MIIRXDV		L1	SDA		R1	PCIAD[25]	

Table 20 RC32435 Pinout (Part 1 of 2)

RC32435 Ground Pins

V_{ss}	V_{ss}	V_{ss} PLL
F6	J6	A11, B12
F7	J7	
F8	J8	
F10	J9	
F11	J10	
G6	K7	
G7	K8	
G8	K9	
G9	K10	
G10	K11	
G11	L6	
H7	L7	
H8	L9	
H9	L10	
H10	L11	
H11		

Table 23 RC32435 Ground Pins

RC32435 Signals Listed Alphabetically

The following table lists the RC32435 pins in alphabetical order.

Signal Name	I/O Type	Location	Signal Category
BDIRN	O	C2	Memory and Peripheral Bus
BOEN	O	B1	
CLK	I	C13	System
COLDRSTN	I	C3	
CSN[0]	O	A4	Memory and Peripheral Bus
CSN[1]	O	B4	
CSN[2]	O	A3	
CSN[3]	O	B3	

Table 24 RC32435 Alphabetical Signal List (Part 1 of 7)

Signal Name	I/O Type	Location	Signal Category
MIICL	I	D2	Ethernet Interface
MIICRS	I	D3	
MIIMDC	O	H2	
MIIMDIO	I/O	H1	
MIIRXCLK	I	F2	
MIIRXD[0]	I	D1	
MIIRXD[1]	I	D4	
MIIRXD[2]	I	E2	
MIIRXD[3]	I	E1	
MIIRXDV	I	G1	
MIIRXER	I	G3	
MIITXCLK	I	G4	
MIITXD[0]	O	E3	
MIITXD[1]	O	E4	
MIITXD[2]	O	F1	
MIITXD[3]	O	F3	
MIITXENP	O	F4	
MIITXER	O	G2	
OEN	O	A2	Memory and Peripheral Bus
PCIAD[0]	I/O	R14	PCI Bus Interface
PCIAD[1]	I/O	T14	
PCIAD[2]	I/O	T13	
PCIAD[3]	I/O	R13	
PCIAD[4]	I/O	P13	
PCIAD[5]	I/O	R12	
PCIAD[6]	I/O	T12	
PCIAD[7]	I/O	P12	
PCIAD[8]	I/O	R11	
PCIAD[9]	I/O	T11	
PCIAD[10]	I/O	P11	
PCIAD[11]	I/O	N11	
PCIAD[12]	I/O	R10	
PCIAD[13]	I/O	T10	
PCIAD[14]	I/O	P10	
PCIAD[15]	I/O	N10	
PCIAD[16]	I/O	T5	

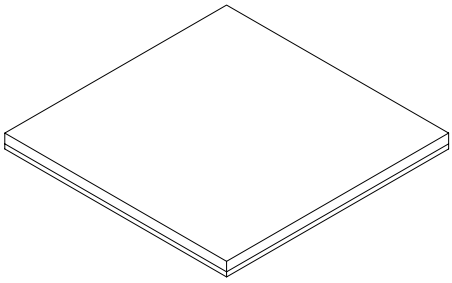
Table 24 RC32435 Alphabetical Signal List (Part 5 of 7)

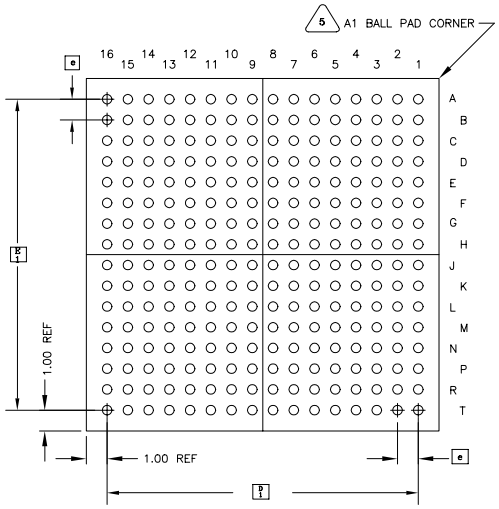
Signal Name	I/O Type	Location	Signal Category
PCIAD[17]	I/O	R5	PCI Bus Interface
PCIAD[18]	I/O	N4	
PCIAD[19]	I/O	T4	
PCIAD[20]	I/O	P4	
PCIAD[21]	I/O	R4	
PCIAD[22]	I/O	T3	
PCIAD[23]	I/O	R3	
PCIAD[24]	I/O	T1	
PCIAD[25]	I/O	R1	
PCIAD[26]	I/O	P2	
PCIAD[27]	I/O	P1	
PCIAD[28]	I/O	N2	
PCIAD[29]	I/O	N1	
PCIAD[30]	I/O	N3	
PCIAD[31]	I/O	M2	
PCIBEN[0]	I/O	N12	
PCIBEN[1]	I/O	R9	
PCIBEN[2]	I/O	R7	
PCIBEN[3]	I/O	R2	
PCICLK	I	T6	
PCIDEVSELN	I/O	T8	
PCIFRAMEN	I/O	P7	
PCIGNTN[0]	I/O	T7	
PCIGNTN[1]	I/O	T15	
PCIGNTN[2]	I/O	R15	
PCIGNTN[3]	I/O	T16	
PCIIRDYN	I/O	N7	
PCILOCKN	I/O	N8	
PCIPAR	I/O	T9	
PCIPERRN	I/O	N9	
PCIREQN[0]	I/O	P6	
PCIREQN[1]	I/O	N5	
PCIREQN[2]	I/O	N6	
PCIREQN[3]	I/O	P5	
PCIRSTN	I/O	R6	
PCISERRN	I/O	P9	

Table 24 RC32435 Alphabetical Signal List (Part 6 of 7)

RC32435 Package Drawing — Page Two

REVISIONS				
DCN	REV	DESCRIPTION	DATE	APPROVED
	00	INITIAL RELEASE	06/09/00	D.G
	01	JEDEC VARIATION MODIFICATION	07/11/00	D.G
	02	UPDATE MAX. THICKNESS A	10/02/02	





BOTTOM VIEW
256 SOLDER BALLS

NOTES: UNLESS OTHERWISE SPECIFIED

1. ALL DIMENSIONS AND TOLERANCES CONFORM TO ASME Y14.5M–1994.
2. "e" REPRESENTS THE BASIC SOLDER BALL GRID PITCH.
3. "MD" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "D" DIRECTION.
   "ME" IS THE MAXIMUM SOLDER BALL MATRIX SIZE IN THE "E" DIRECTION.
4. "N" IS THE MAXIMUM ALLOWABLE NUMBER OF SOLDER BALLS.
5. DIMENSION "b" IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM Z.
6. PRIMARY DATUM Z AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
7. "A1" ID CORNER MUST BE IDENTIFIED. IDENTIFICATION MAY BE BY MEANS OF CHAMFER, METALLIZED OR INK MARK, INDENTATION OR OTHER FEATURE OF THE PACKAGE BODY.
8. ALL DIMENSIONS ARE IN MILLIMETERS.
9. THIS DRAWING CONFORMS TO JEDEC PUBLICATION 95 REGISTRATION MO–192 VARIATION AAF–1
   EXCEPTIONS:
   b MIN=0.41 NOM=0.46 MAX=0.51

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN MILLIMETERS
DECIMAL: X.X ±0.10, X.XX ±0.05, X.XXX ±0.00
ANGULAR: ±1°

APPROVALS	DATE
DRAWN BX	06/09/00
CHECKED	

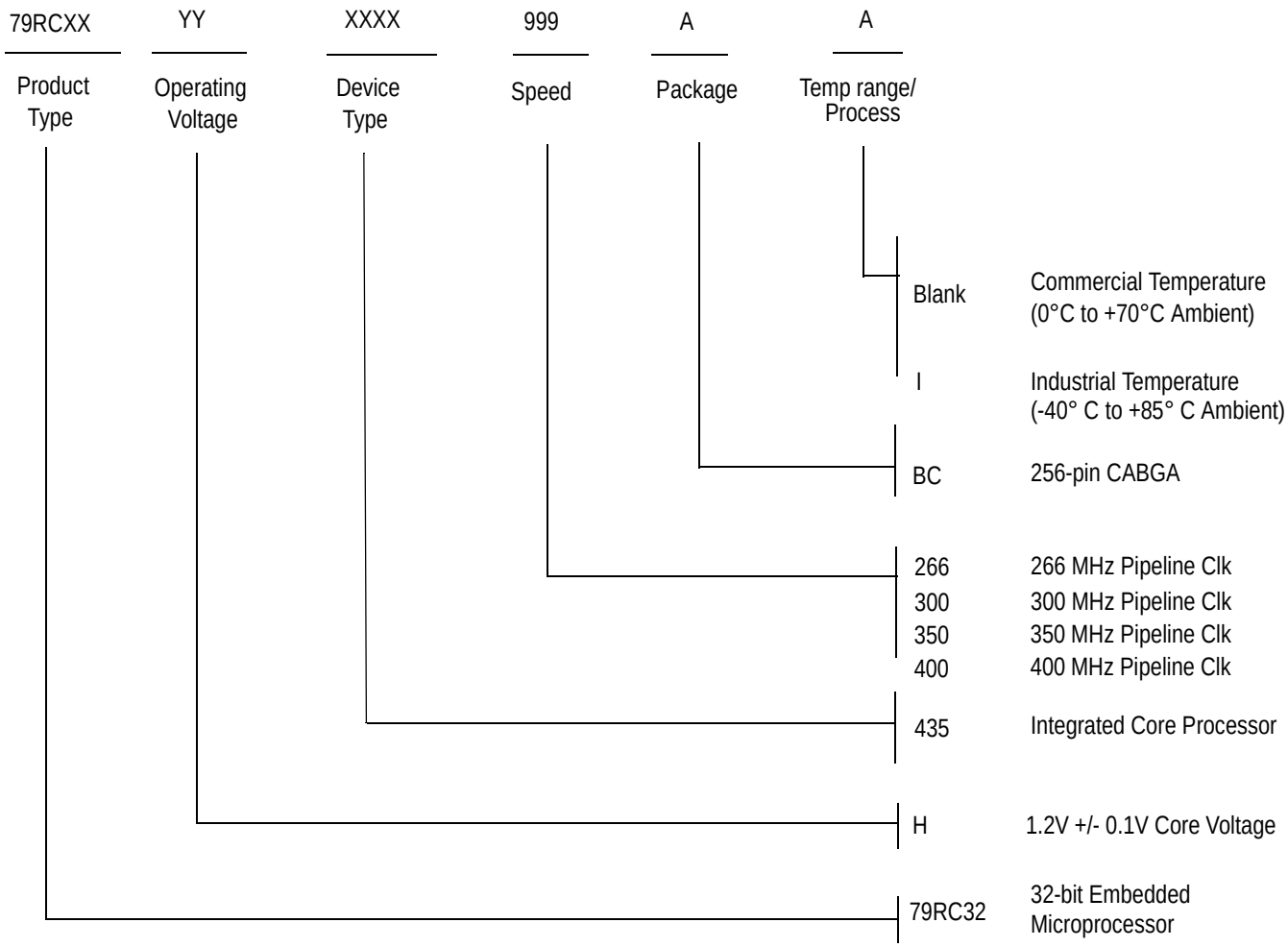
Integrated Device Technology, Inc.
2975 Stender Way, Santa Clara, CA 95054
(408) 727–6116 FAX (408) 492–8074

BC256 PACKAGE OUTLINE
17.0 X 17.0 mm BODY CABGA

DRAWING No.	SIZE	SCALE	REV
PSC–4093	C	N/A	02

DO NOT SCALE DRAWING — SHEET 2 OF 2

Ordering Information



Valid Combinations

79RC32H435 - 266BC, 300BC, 350BC, 400BC	256-pin CABGA package, Commercial Temperature
79RC32H435 - 266BCI, 300BCI, 350BCI	256-pin CABGA package, Industrial Temperature

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