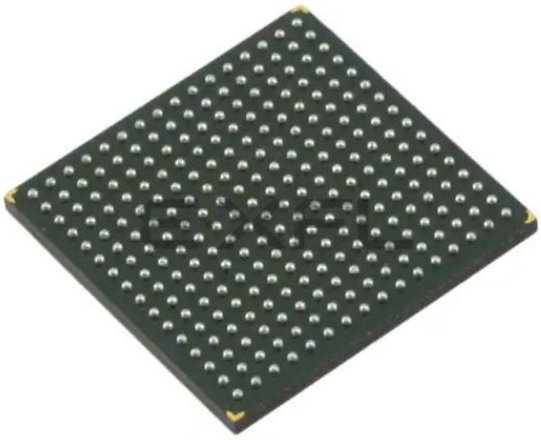
Renesas Electronics America Inc - 79RC32H435-300BCI Datasheet



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Embedded microprocessors are utilized across a broad spectrum of applications, making them indispensable in

Details	
Product Status	Obsolete
Core Processor	MIPS32
Number of Cores/Bus Width	1 Core, 32-Bit
Speed	300MHz
Co-Processors/DSP	-
RAM Controllers	DDR
Graphics Acceleration	No
Display & Interface Controllers	-
Ethernet	10/100Mbps (1)
SATA	-
USB	-
Voltage - I/O	3.3V
Operating Temperature	-40°C ~ 85°C (TA)
Security Features	-
Package / Case	256-LBGA
Supplier Device Package	256-CABGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/renesas-electronics-america/79rc32h435-300bci

Pin Characteristics

Note: Some input pads of the RC32435 do not contain internal pull-ups or pull-downs. Unused inputs should be tied off to appropriate levels. This is especially critical for unused control signal inputs (such as WAITACKN) which, if left floating, could adversely affect the RC32435's operation. Also, any input pin left floating can cause a slight increase in power consumption.

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Memory and Peripheral Bus	BDIRN	O	LVTTL	High Drive		
	BOEN	O	LVTTL	High Drive		
	WEN	O	LVTTL	High Drive		
	CSN[3:0]	O	LVTTL	High Drive		
	MADDR[21:0]	I/O	LVTTL	High Drive		
	MDATA[7:0]	I/O	LVTTL	High Drive		
	OEN	O	LVTTL	High Drive		
	RWN	O	LVTTL	High Drive		
	WAITACKN	I	LVTTL	STI	pull-up	
DDR Bus	DDRADDR[13:0]	O	SSTL_2			
	DDRBA[1:0]	O	SSTL_2			
	DDRCASN	O	SSTL_2			
	DDRCKE	O	SSTL_2 / LVC-MOS			
	DDRCKN	O	SSTL_2			
	DDRCKP	O	SSTL_2			
	DDRCSN	O	SSTL_2			
	DDRDATA[15:0]	I/O	SSTL_2			
	DDRDM[1:0]	O	SSTL_2			
	DDRDQS[1:0]	I/O	SSTL_2			
	DDRRASN	O	SSTL_2			
	DDRVREF	I	Analog			
	DDRWEN	O	SSTL_2			
PCI Bus Interface	PCIAD[31:0]	I/O	PCI			
	PCICBEN[3:0]	I/O	PCI			
	PCICLK	I	PCI			
	PCIDEVSELN	I/O	PCI			pull-up on board
	PCIFRAMEN	I/O	PCI			pull-up on board
	PCIGNTN[3:0]	I/O	PCI			pull-up on board
	PCIIRDYN	I/O	PCI			pull-up on board
	PCILOCKN	I/O	PCI			
	PCIPAR	I/O	PCI			
	PCIPERRN	I/O	PCI			
	PCIREQN[3:0]	I/O	PCI			pull-up on board
	PCIRSTN	I/O	PCI			pull-down on board
	PCISERRN	I/O	PCI	Open Collector		pull-up on board
	PCISTOPN	I/O	PCI			pull-up on board
	PCITRDYN	I/O	PCI			pull-up on board
General Purpose I/O	GPIO[8:0]	I/O	LVTTL	High Drive	pull-up	
	GPIO[13:9]	I/O	PCI			pull-up on board

Table 2 Pin Characteristics (Part 1 of 2)

Function	Pin Name	Type	Buffer	I/O Type	Internal Resistor	Notes[1]
Serial Peripheral Interface	SCK	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDI	I/O	LVTTL	High Drive	pull-up	pull-up on board
	SDO	I/O	LVTTL	High Drive	pull-up	pull-up on board
I^2C-Bus Interface	SCL	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
	SDA	I/O	LVTTL	Low Drive/STI		pull-up on board[2]
Ethernet Interfaces	MIICL	I	LVTTL	STI	pull-down	
	MIICRS	I	LVTTL	STI	pull-down	
	MIIRXCLK	I	LVTTL	STI	pull-up	
	MIIRXD[3:0]	I	LVTTL	STI	pull-up	
	MIIRXDV	I	LVTTL	STI	pull-down	
	MIIRXER	I	LVTTL	STI	pull-down	
	MIITXCLK	I	LVTTL	STI	pull-up	
	MIITXD[3:0]	O	LVTTL	Low Drive		
	MIITXENP	O	LVTTL	Low Drive		
	MIITXER	O	LVTTL	Low Drive		
	MIIMDC	O	LVTTL	Low Drive		
	MIIMDIO	I/O	LVTTL	Low Drive	pull-up	
EJTAG / JTAG	JTAG_TMS	I	LVTTL	STI	pull-up	
	EJTAG_TMS	I	LVTTL	STI	pull-up	
	JTAG_TRST_N	I	LVTTL	STI	pull-up	
	JTAG_TCK	I	LVTTL	STI	pull-up	
	JTAG_TDO	O	LVTTL	Low Drive		
	JTAG_TDI	I	LVTTL	STI	pull-up	
System	CLK	I	LVTTL	STI		
	EXTBCV	I	LVTTL	STI	pull-down	
	EXTCLK	O	LVTTL	High Drive		
	COLDRSTN	I	LVTTL	STI		
	RSTN	I/O	LVTTL	Low Drive / STI	pull-up	pull-up on board

Table 2 Pin Characteristics (Part 2 of 2)

1. External pull-up required in most system applications. Some applications may require additional pull-ups not identified in this table.

2. Use a 2.2K pull-up resistor for I2C pins.

Signal	Name/Description
MADDR[11]	**Disable Watchdog Timer**. When this bit is set, the watchdog timer is disabled following a cold reset. 0x0 - Watchdog timer enabled 0x1 - Watchdog timer disabled
MADDR[13:12]	**Reserved**. These pins must be driven low during boot configuration.
MADDR[15:14]	**Reserved**. Must be set to zero.

Table 3 Boot Configuration Encoding (Part 2 of 2)

System Clock Parameters

(Values based on systems running at recommended supply voltages and operating temperatures, as shown in Tables 15 and 16.)

Parameter	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Units	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
PCLK[1]	Frequency	none	200	266	200	300	200	350	200	400	MHz	See Figure 3.
	Tper		3.8	5.0	3.3	5.0	2.85	5.0	2.5	5.0	ns	
ICLK[2,3,4]	Frequency	none	100	133	100	150	100	175	100	200	MHz	
	Tper		7.5	10.0	6.7	10.0	5.7	10.0	5.0	10.0	ns	
CLK[5]	Frequency	none	25	125	25	125	25	125	25	125	MHz	
	Tper_5a		8.0	40.0	8.0	40.0	8.0	40.0	8.0	40.0	ns	
	Thigh_5a, Tlow_5a		40	60	40	60	40	60	40	60	% of Tper_5a	
	Trise_5a, Tfall_5a		—	3.0	—	3.0	—	3.0	—	3.0	ns	
	Tjitter_5a		—	0.1	—	0.1	—	0.1	—	0.1	ns	

Table 5 Clock Parameters

1. The CPU pipeline clock (PCLK) speed is selected during cold reset by the boot configuration vector (see Table 3). Refer to Chapter 3, Clocking and Initialization, in the RC32435 User Reference Manual for the allowable frequency ranges of CLK and PCLK.
2. ICLK is the internal IPBus clock. It is always equal to PCLK divided by 2. This clock cannot be sampled externally.
3. The ethernet clock (MIIxRXCLK and MIIxTXCLK) frequency must be equal to or less than 1/2 ICLK (MIIxRXCLK and MIIxTXCLK <= 1/2(ICLK)).
4. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.
5. The input clock (CLK) is input from the external oscillator to the internal PLL.

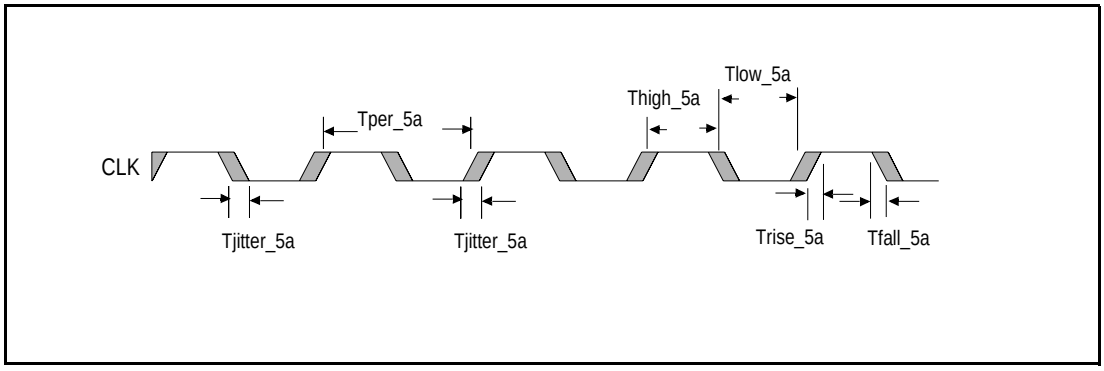
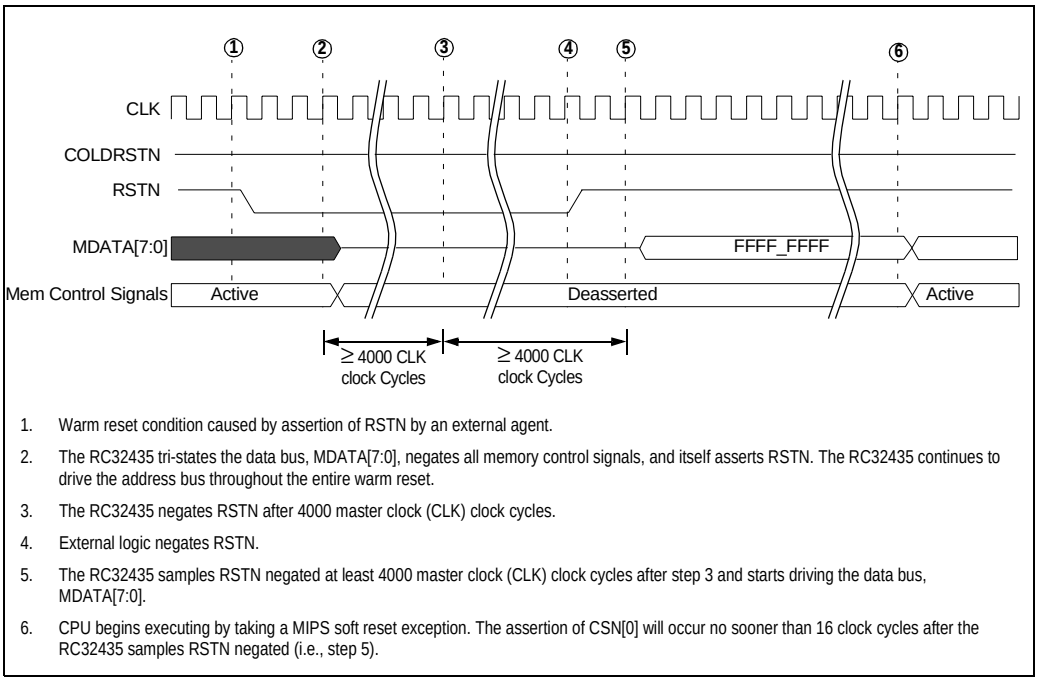


Figure 3 Clock Parameters Waveform



1. Warm reset condition caused by assertion of RSTN by an external agent.
2. The RC32435 tri-states the data bus, MDATA[7:0], negates all memory control signals, and itself asserts RSTN. The RC32435 continues to drive the address bus throughout the entire warm reset.
3. The RC32435 negates RSTN after 4000 master clock (CLK) clock cycles.
4. External logic negates RSTN.
5. The RC32435 samples RSTN negated at least 4000 master clock (CLK) clock cycles after step 3 and starts driving the data bus, MDATA[7:0].
6. CPU begins executing by taking a MIPS soft reset exception. The assertion of CSN[0] will occur no sooner than 16 clock cycles after the RC32435 samples RSTN negated (i.e., step 5).

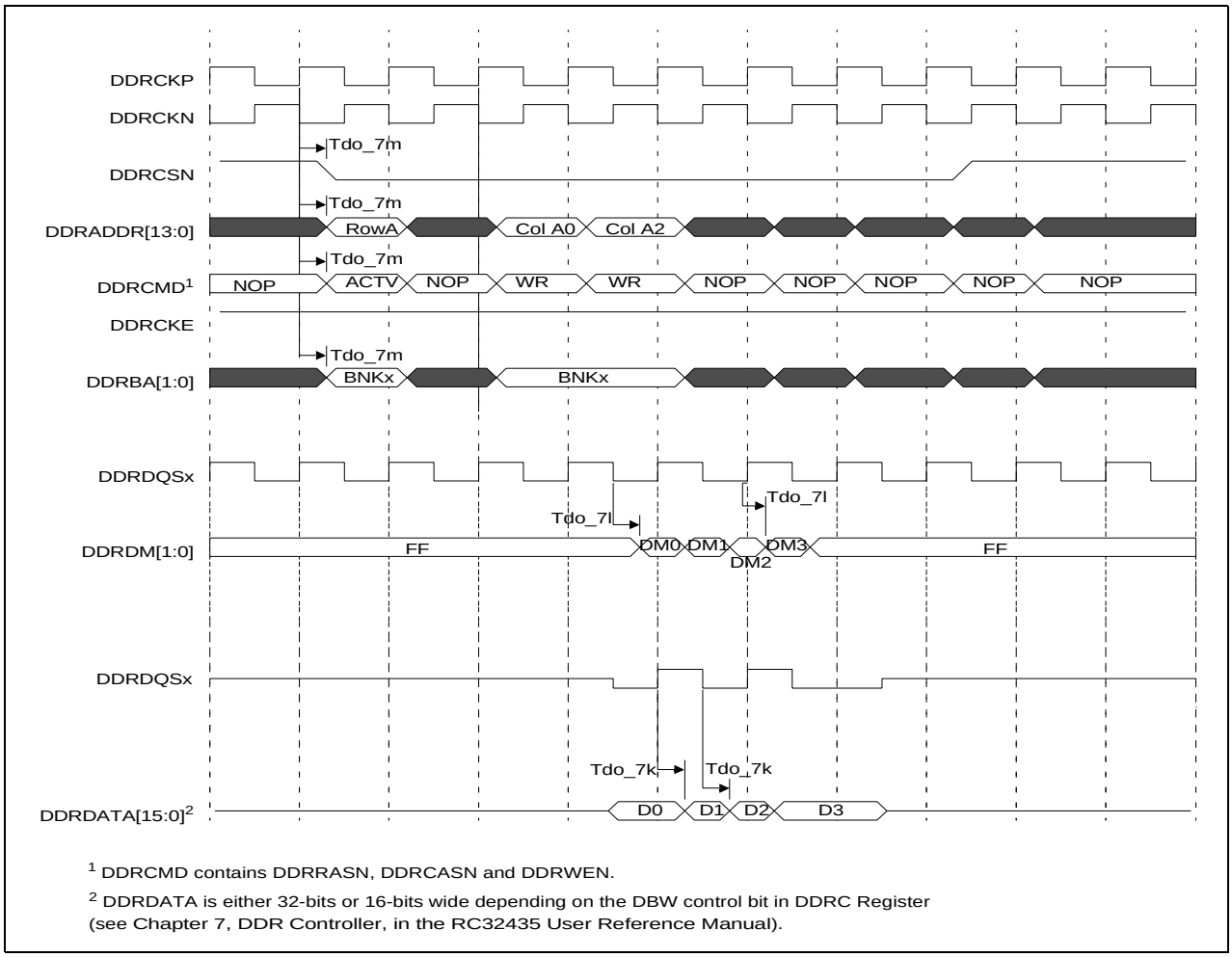
Figure 5 Externally Initiated Warm Reset AC Timing Waveform

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max		
Memory Bus - DDR Access												
DDRDATA[15:0]	Tskew_7g	DDRDQSx	0	0.9	0	0.8[1]	0	0.7	0.0	0.6	ns	See Figures 6 and 7.
	Tdo_7k[2]		1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDM[1:0]	Tdo_7l	DDRDQSx	1.2	1.9	1.0	1.7	0.7	1.5	0.5	1.4	ns	
DDRDQS[1:0]	Tdo_7i	DDRCKP	-0.75	0.75	-0.75	0.75	-0.7	0.7	-0.7	0.7	ns	
DDRADDR[13:0], DDRBA[1:0], DDRCASN, DDRCKE, DDRCSN, DDRRASN, DDRWEN	Tdo_7m	DDRCKP	1.0	4.0	1.0	4.3	1.0	4.0	1.0	4.0	ns	

Table 7 DDR SDRAM Timing Characteristics

1. Meets DDR timing requirements for 150MHz clock rate DDR SDRAMs with 300 ps remaining margin to compensate for PCB propagation mismatches, which is adequate to guarantee functional timing, provided the RC32435 DDR layout guidelines are adhered to.

2. Setup times are calculated as applicable clock period - Tdo max. For example, if the DDR is running at 266MHz, it uses a 133MHz input clock. The period for a 133MHz clock is 7.5ns. If the Tdo max value is 4.6ns, the T_{IS} parameter is 7.5ns minus 4.6ns = 2.9ns. The DDR spec for this parameter is 1ns, so there is 1.9ns of slack left over for board propagation. Calculations for T_{DS} are similar, but since this parameter is taken relative to the DDRDQS signals, which are referenced on both edges, the effective period with a 133MHz input clock is only 3.75ns. So, if the max Tdo is 1.9ns, we have 3.75ns minus 1.9ns = 1.85ns for T_{DS}. The DDR data sheet specs a value of 0.5ns for 266MHz, so this leaves 1.35ns slack for board propagation delays.



[1] DDRCMD contains DDRRASN, DDRCASN and DDRWEN.

[2] DDRDATA is either 32-bits or 16-bits wide depending on the DBW control bit in DDRC Register (see Chapter 7, DDR Controller, in the RC32435 User Reference Manual).

Figure 7 DDR SDRAM Timing Waveform — Write Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
Memory and Peripheral Bus[1]													See Figures 8 and 9.
MADDR[21:0]	Tdo_8a	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8a[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8a[2]		—	—	—	—	—	—	—	—	ns		
MADDR[25:22]	Tdo_8b	EXTCLK rising	0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8b[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8b[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 1 of 2)

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Conditions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
MDATA[7:0]	Tsu_8c	EXTCLK rising	6.0	—	6.0	—	6.0	—	6.0	—	ns		See Figures 8 and 9 (cont.).
	Thld_8c		0	—	0	—	0	—	0	—	ns		
	Tdo_8c		0.4	4.5	0.4	4.5	0.4	4.5	0.4	4.5	ns		
	Tdz_8c[2]		0	0.5	0	0.5	0	0.5	0	0.5	ns		
	Tzd_8c[2]		0.4	3.3	0.4	3.3	0.4	3.3	0.4	3.3	ns		
EXTCLK[3]	Tper_8d	none	7.5	—	6.66	—	6.66	—	6.66	—	ns		
BDIRN	Tdo_8e	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8e[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8e[2]		—	—	—	—	—	—	—	—	ns		
BOEN	Tdo_8f	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8f[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8f[2]		—	—	—	—	—	—	—	—	ns		
WAITACKN[4]	Tsu_8h	EXTCLK rising	6.5	—	6.5	—	6.5	—	6.5	—	ns		
	Thld_8h		0	—	0	—	0	—	0	—	ns		
	Tpw_8h[2]	none	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	2(EXTCLK)	—	ns		
CSN[3:0]	Tdo_8i	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8i[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8i[2]		—	—	—	—	—	—	—	—	ns		
RWN	Tdo_8j	EXTCLK rising	0.4	3.8	0.4	3.8	0.4	3.8	0.4	3.8	ns		
	Tdz_8j[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8j[2]		—	—	—	—	—	—	—	—	ns		
OEN	Tdo_8k	EXTCLK rising	0.4	4.0	0.4	4.0	0.4	4.0	0.4	4.0	ns		
	Tdz_8k[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8k[2]		—	—	—	—	—	—	—	—	ns		
WEN	Tdo_8l	EXTCLK rising	0.4	3.7	0.4	3.7	0.4	3.7	0.4	3.7	ns		
	Tdz_8l[2]		—	—	—	—	—	—	—	—	ns		
	Tzd_8l[2]		—	—	—	—	—	—	—	—	ns		

Table 8 Memory and Peripheral Bus AC Timing Characteristics (Part 2 of 2)

1. The RC32435 provides bus turnaround cycles to prevent bus contention when going from read to write, write to read, and during external bus ownership. For example, there are no cycles where an external device and the RC32435 are both driving. See Chapter 6, Device Controller, in the RC32435 User Reference Manual.

2. The values for this symbol were determined by calculation, not by testing.

3. The frequency of EXTCLK is programmable. See the External Clock Divider (MDATA[5:4]) description in Table 3 of this data sheet.

4. WAITACKN must meet the setup and hold times if it is synchronous or the minimum pulse width if it is asynchronous.

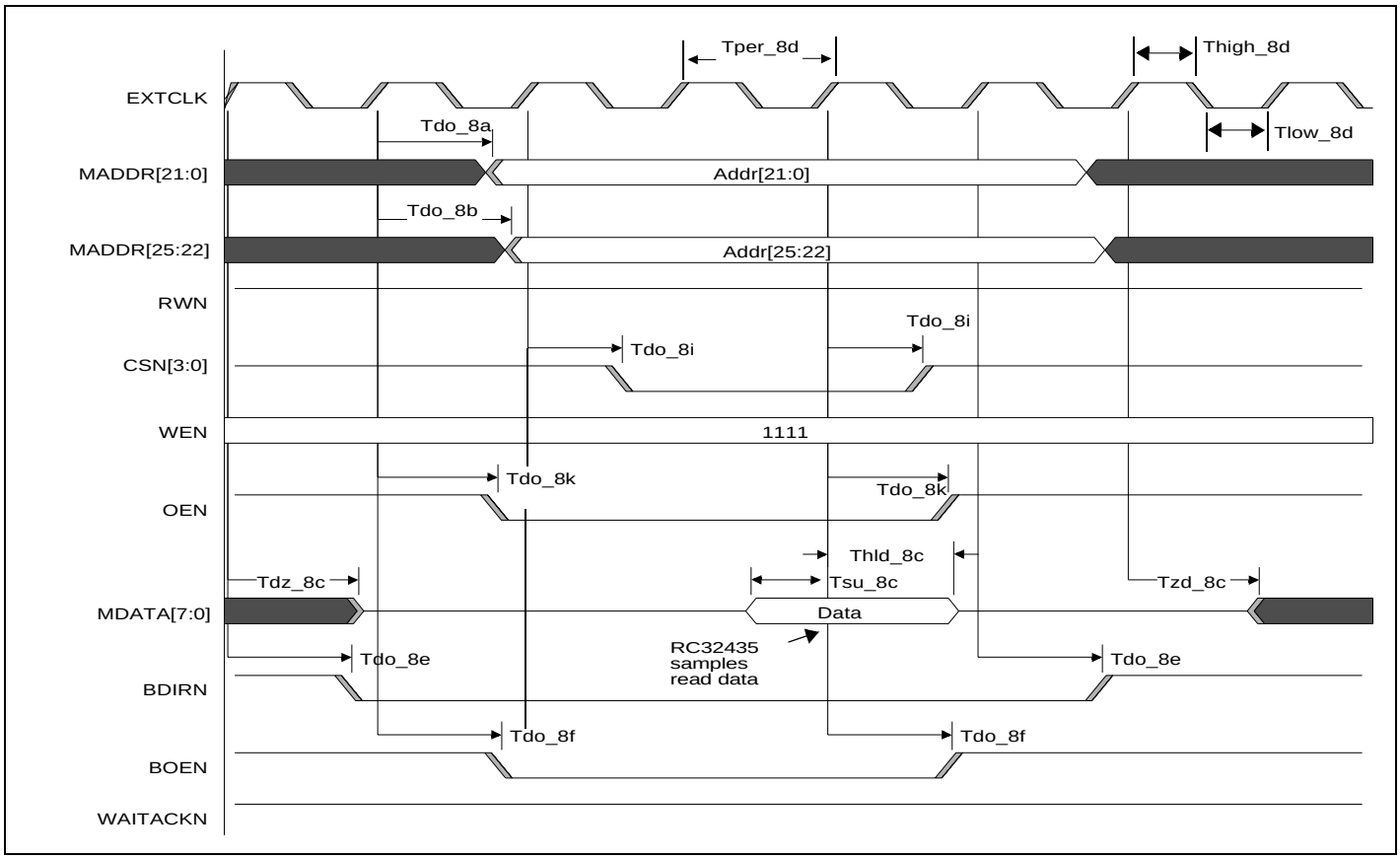


Figure 8 Memory and Peripheral Bus AC Timing Waveform — Read Access

Signal	Symbol	Reference Edge	266MHz		300MHz		350MHz		400MHz		Unit	Condi-tions	Timing Diagram Reference
			Min	Max	Min	Max	Min	Max	Min	Max			
PCI[1]													
PCICLK[2]	Tper_10a	none	15.0	30.0	15.0	30.0	15.0	30.0	15.0	30.0	ns	66 MHz PCI	See Figure 11.
	Thigh_10a, Tlow_10a		6.0	—	6.0	—	6.0	—	6.0	—	ns		
	Tslew_10a		1.5	4.0	1.5	4.0	1.5	4.0	1.5	4.0	V/ns		
PCIAD[31:0], PCIBEN[3:0], PCIDEVSELN, PCIFRA-MEN,PCIIR-DYN, PCILOCKN, PCIPAR, PCI-PERRN, PCIS-TOPN, PCITRDY	Tsu_10b	PCICLK rising	3.0	—	3.0	—	3.0	—	3.0	—	ns		
	Thld_10b		0	—	0	—	0	—	0	—	ns		
	Tdo_10b		2.0	6.0	2.0	6.0	2.0	6.0	2.0	6.0	ns		
	Tdz_10b[3]		—	14.0	—	14.0	—	14.0	—	14.0	ns		
	Tzd_10b[3]		2.0	—	2.0	—	2.0	—	2.0	—	ns		
PCIGNTN[3:0], PCIREQN[3:0]	Tsu_10c	PCICLK rising	5.0	—	5.0	—	5.0	—	5.0	—	ns		
	Thld_10c		0	—	0	—	0	—	0	—	ns		
	Tdo_10c		2.0	6.0	2.0	6.0	2.0	6.0	2.0	6.0	ns		
PCIRSTN (out-put)[4]	Tpw_10d[3]	None	4000 (CLK)	—	4000 (CLK)	—	4000 (CLK)	—	4000 (CLK)	—	ns		See Figures 15 and 16
PCIRSTN (input)[4,5]	Tpw_10e[3]	None	2(CLK)	—	2(CLK)	—	2(CLK)	—	2(CLK)	—	ns		
	Tdz_10e[3]	PCIRSTN falling	6(CLK)	—	6(CLK)	—	6(CLK)	—	6(CLK)	—	ns		
PCISERRN[6]	Tsu_10f	PCICLK rising	3.0	—	3.0	—	3.0	—	3.0	—	ns		See Figure 11
	Thld_10f		0	—	0	—	0	—	0	—	ns		
	Tdo_10f		2.0	6.0	2.0	6.0	2.0	6.0	2.0	6.0	ns		
PCIMUINTN[6]	Tdo_10g	PCICLK rising	4.7	11.1	4.7	11.1	4.7	11.1	4.7	11.1	ns		

Table 10 PCI AC Timing Characteristics

1. This PCI interface conforms to the PCI Local Bus Specification, Rev 2.2.

2. PCICLK must be equal to or less than two times ICLK (PCICLK <= 2(ICLK)) with a maximum PCICLK of 66 MHz.

3. The values for this symbol were determined by calculation, not by testing.

4. PCIRSTN is an output in host mode and an input in satellite mode.

5. To meet the PCI delay specification from reset asserted to outputs floating, the PCI reset should be logically combined with the COLDRSTN input, instead of input on PCIRSTN.

6. PCISERRN and PCIMUINTN use open collector I/O types.

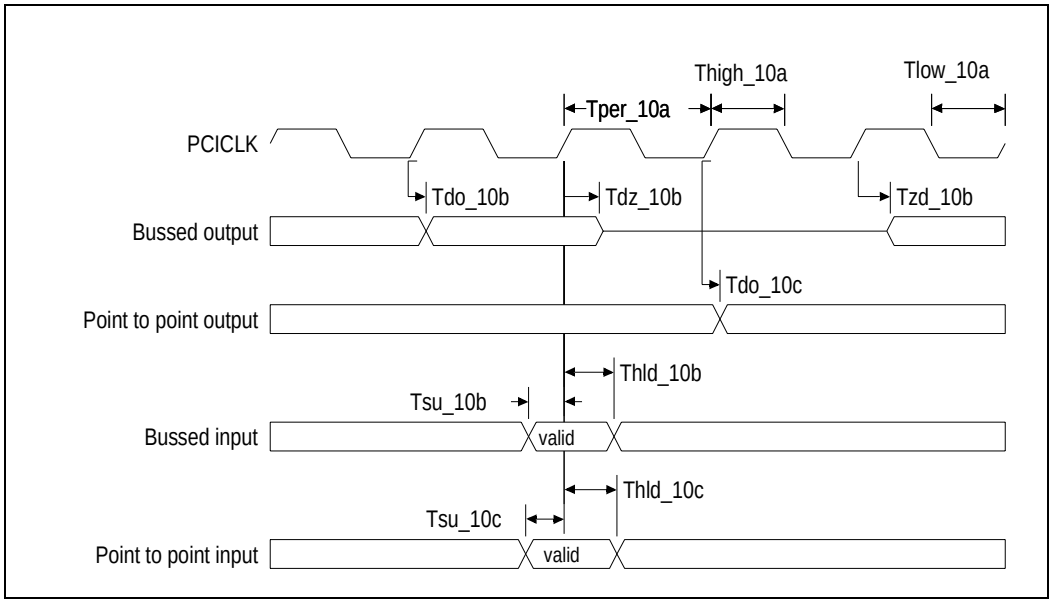
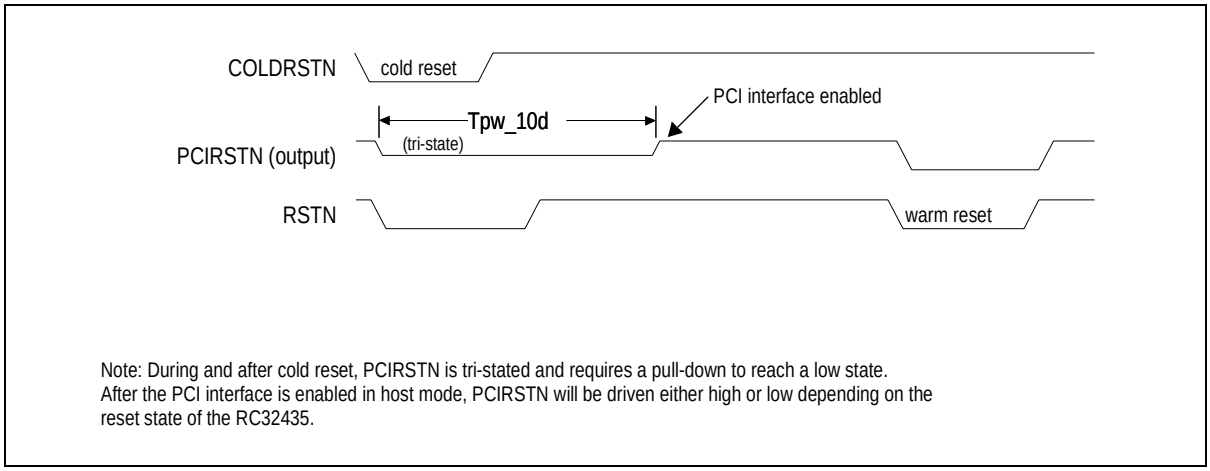


Figure 11 PCI AC Timing Waveform



Note: During and after cold reset, PCIRSTN is tri-stated and requires a pull-down to reach a low state. After the PCI interface is enabled in host mode, PCIRSTN will be driven either high or low depending on the reset state of the RC32435.

Figure 12 PCI AC Timing Waveform — PCI Reset in Host Mode

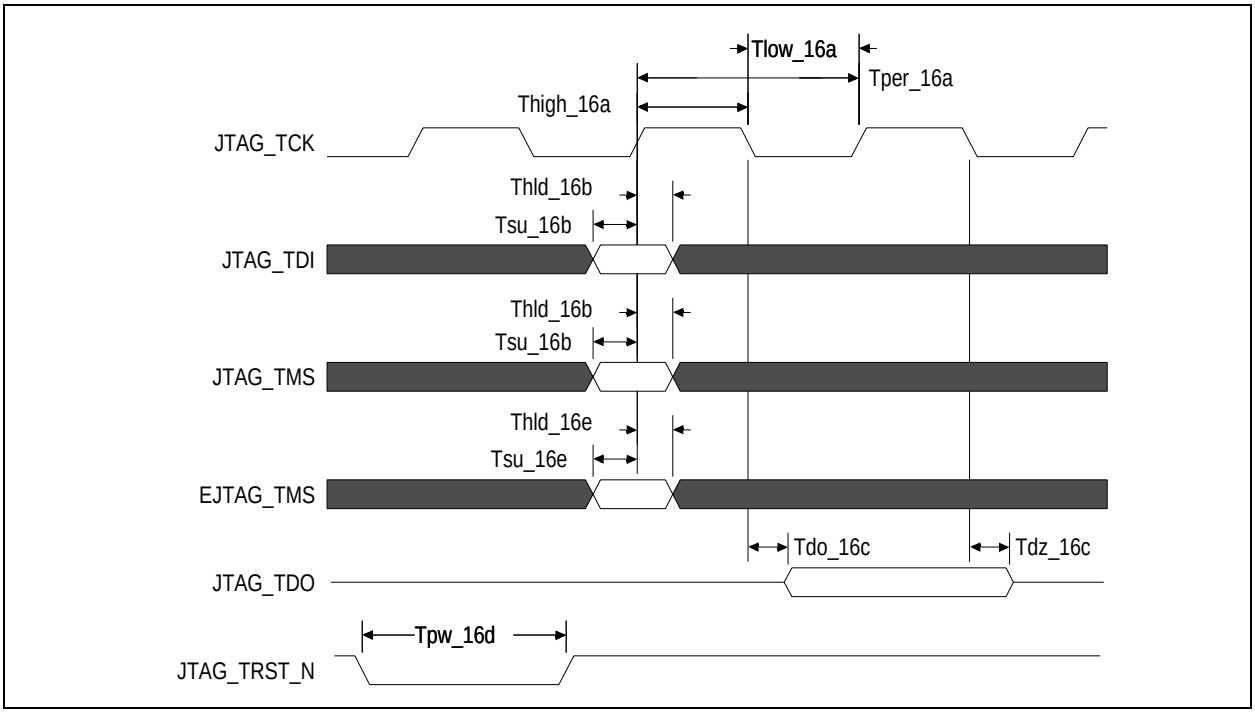


Figure 19 JTAG AC Timing Waveform

The IEEE 1149.1 specification requires that the JTAG and EJTAG TAP controllers be reset at power-up whether or not the interfaces are used for a boundary scan or a probe. Reset can occur through a pull-down resistor on JTAG_TRST_N if the probe is not connected. However, on-chip pull-up resistors are implemented on the RC32435 due to an IEEE 1149.1 requirement. Having on-chip pull-up and external pull-down resistors for the JTAG_TRST_N signal requires special care in the design to ensure that a valid logical level is provided to JTAG_TRST_N, such as using a small external pull-down resistor to ensure this level overrides the on-chip pull-up. An alternative is to use an active power-up reset circuit for JTAG_TRST_N, which drives JTAG_TRST_N low only at power-up and then holds JTAG_TRST_N high afterwards with a pull-up resistor.

Figure 20 shows the electrical connection of the EJTAG probe target system connector.

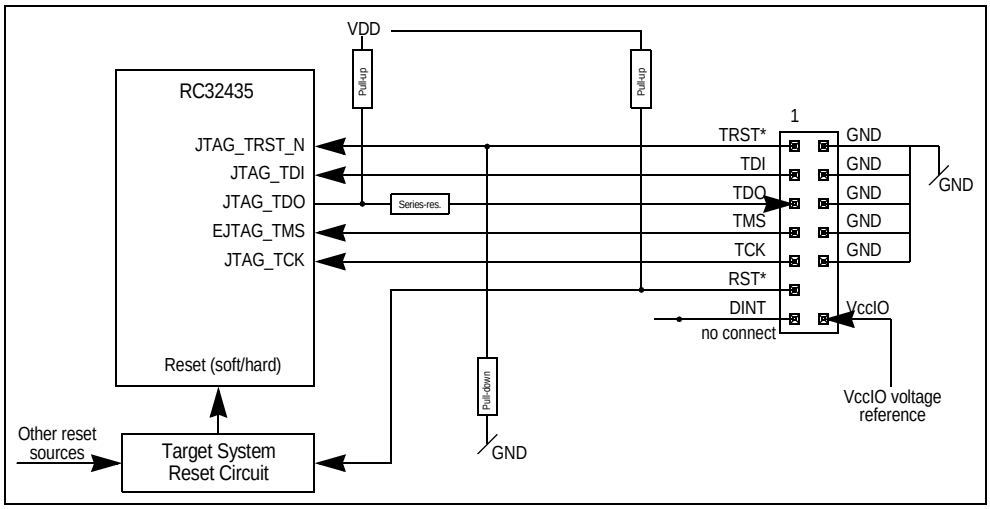


Figure 20 Target System Electrical EJTAG Connection

Using the EJTAG Probe

In Figure 20, the pull-up resistors for JTAG_TDO and RST*, the pull-down resistor for JTAG_TRST_N, and the series resistor for JTAG_TDO must be adjusted to the specific design. However, the recommended pull-up/down resistor is 1.0 kΩ because a low value reduces crosstalk on the cable to the connector, allowing higher JTAG_TCK frequencies. A typical value for the series resistor is 33 Ω. Recommended resistor values have ± 5% tolerance.

If a probe is used, the pull-up resistor on JTAG_TDO must ensure that the JTAG_TDO level is high when no probe is connected and the JTAG_TDO output is tri-stated. This requirement allows reliable connection of the probe if it is hooked-up when the power is already on (hot plug). The pull-up resistor value of around 47 kΩ should be sufficient. Optional diodes to protect against overshoot and undershoot voltage can be added on the signals of the chip with EJTAG.

If a probe is used, the RST* signal must have a pull-up resistor because it is controlled by an open-collector (OC) driver in the probe, and thus is actively pulled low only. The pull-up resistor is responsible for the high value when not driven by the probe of 25pF. The input on the target system reset circuit must be able to accept the rise time when the pull-up resistor charges the capacitance to a high logical level. Vcc I/O must connect to a voltage reference that drops rapidly to below 0.5V when the target system loses power, even with a capacitive load of 25pF. The probe can thus detect the lost power condition.

For additional information on EJTAG, refer to Chapter 17 of the RC32435 User Reference Manual.

Phase-Locked Loop (PLL)

The phase-locked loop (PLL) multiplies the external oscillator input (pin CLK) according to the parameter provided by the boot configuration vector to create the processor clock (PCLK). Inherently, PLL circuits are only capable of generating clock frequencies within a limited range.

PLL Filters

It is recommended that the system designer provide a filter network of passive components for the PLL analog and digital power supplies. The PLL circuit power and PLL circuit ground should be isolated from power and ground with a filter circuit such as the one shown in Figure 21. Because the optimum values for the filter components depend upon the application and the system noise environment, these values should be considered as starting points for further experimentation within your specific application.

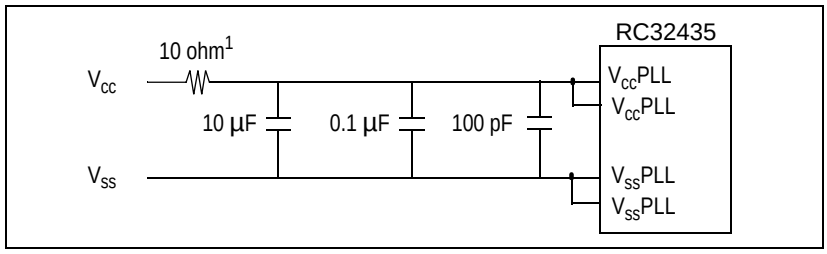


Figure 21 PLL Filter Circuit for Noisy Environments

Recommended Operating Supply Voltages

Symbol	Parameter	Minimum	Typical	Maximum	Unit
V_{SS}	Common ground	0	0	0	V
V_{SS}PLL	PLL ground				
V_{CC}I/O	I/O supply except for SSTL_2[1]	3.135	3.3	3.465	V
V_{CC}SI/O (DDR)	I/O supply for SSTL_2[1]	2.375	2.5	2.625	V
V_{CC}PLL	PLL supply (digital)	1.1	1.2	1.3	V
V_{CC}APLL	PLL supply (analog)	3.135	3.3	3.465	V
V_{CC}Core	Internal logic supply	1.1	1.2	1.3	V
DDRVREF[2]	SSTL_2 input reference voltage	0.5(VccSI/O)	0.5(VccSI/O)	0.5(VccSI/O)	V
V_{TT}[3]	SSTL_2 termination voltage	DDRVREF - 0.04	DDRVREF	DDRVREF + 0.04	V

Table 15 RC32435 Operating Voltages

1. SSTL_2 I/Os are used to connect to DDR SDRAM.
2. Peak-to-peak AC noise on DDRVREF may not exceed ± 2% DDRVREF (DC).
3. V_{TT} of the SSTL_2 transmitting device must track DDRVREF of the receiving device.

Recommended Operating Temperatures

Grade	Temperature
Commercial	0°C to +70°C Ambient
Industrial	-40°C to +85°C Ambient

Table 16 RC32435 Operating Temperatures

Capacitive Load Deration

Refer to the 79RC32435 IBIS Model on the IDT web site (www.idt.com).

Power-on Sequence

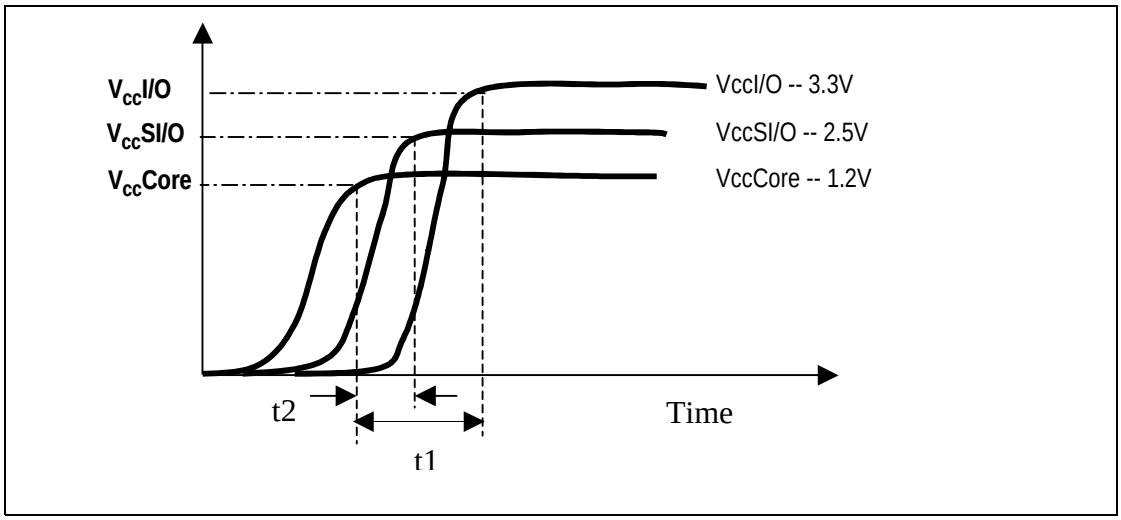
Three power-on sequences are given below. Sequence #1 is recommended because it will prevent I/O conflicts and will also allow the input signals to propagate when the I/O powers are brought up.

Note: The ESD diodes may be damaged if one of the voltages is applied and one of the other voltages is at a ground level.

A. Recommended Sequence

t2 > 0 whenever possible (V_{cc}Core)

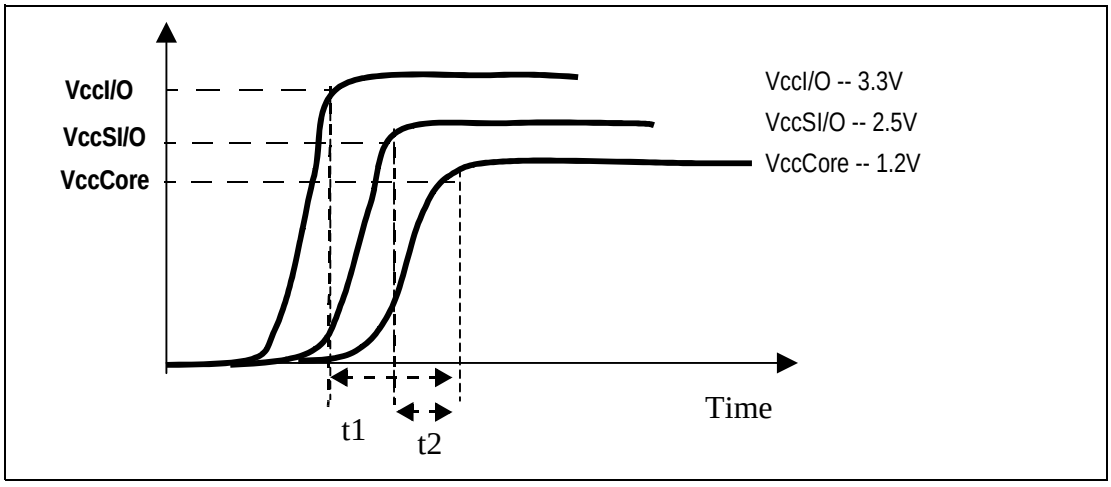
t1 - t2 can be 0 (V_{cc}SI/O followed by V_{cc}I/O)



B. Reverse Voltage Sequence

If sequence A is not feasible, then Sequence B can be used:

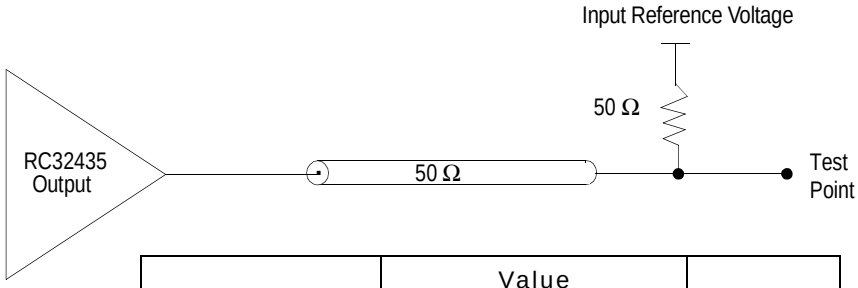
t1 <50ms and t2 <50ms to prevent damage.



C. Simultaneous Power-up

VccI/O, VccSI/O, and VccCore can be powered up simultaneously.

AC Test Conditions



Parameter	Value		Units
	SSTL I/O	Other I/O	
Input pulse levels	0 to 2.5	0 to 3.3	V
Input rise/fall	0.8	1.0	ns
Input reference level	0.5(VccSI/O)	0.5(VccI/O)	V
Output reference levels	1.25	1.5	V
AC test load	35	35	pF

Figure 23 AC Test Conditions

Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt	Pin	Function	Alt
C2	BDIRN		G2	MIITXER		L2	SCL		R2	PCICBEN[3]	
C3	COLDRSTN		G3	MIIRXER		L3	GPIO[8]	1	R3	PCIAD[23]	
C4	WEN		G4	MIITXCLK		L4	SDI		R4	PCIAD[21]	
C5	MDATA[3]		G5	V_{CC} I/0		L5	V_{CC} I/0		R5	PCIAD[17]	
C6	MDATA[5]		G6	V_{SS}		L6	V_{SS}		R6	PCIRSTN	
C7	GPIO[6]	1	G7	V_{SS}		L7	V_{SS}		R7	PCICBEN[2]	
C8	MADDR[21]		G8	V_{SS}		L8	V_{CC} CORE		R8	PCITRDYN	
C9	MADDR[18]		G9	V_{SS}		L9	V_{SS}		R9	PCICBEN[1]	
C10	MADDR[14]		G10	V_{SS}		L10	V_{SS}		R10	PCIAD[12]	
C11	JTAG_TMS		G11	V_{SS}		L11	V_{SS}		R11	PCIAD[8]	
C12	V_{CC} APLL		G12	V_{CC} DDR		L12	V_{CC} DDR		R12	PCIAD[5]	
C13	CLK		G13	DDRDM[1]		L13	DDRADDR[9]		R13	PCIAD[3]	
C14	MADDR[4]		G14	DDRDQS[1]		L14	DDRWEN		R14	PCIAD[0]	
C15	MADDR[0]		G15	DDRDATA[10]		L15	DDRCASN		R15	PCIGNTN[2]	
C16	DDRDATA[0]		G16	DDRDATA[11]		L16	DDRADDR[8]		R16	DDRADDR[1]	
D1	MIIRXD[0]		H1	MIIMDIO		M1	GPIO[12]	1	T1	PCIAD[24]	
D2	MIICL		H2	MIIMDC		M2	PCIAD[31]		T2	GPIO[13]	1
D3	MIICRS		H3	GPIO[0]	1	M3	GPIO[11]	1	T3	PCIAD[22]	
D4	MIIRXD[1]		H4	GPIO[1]	1	M4	GPIO[9]	1	T4	PCIAD[19]	
D5	MDATA[7]		H5	V_{CC} CORE		M5	V_{CC} I/0		T5	PCIAD[16]	
D6	MDATA[2]		H6	V_{CC} CORE		M6	V_{CC} I/0		T6	PCICLK	
D7	MDATA[0]		H7	V_{SS}		M7	V_{CC} I/0		T7	PCIGNTN[0]	
D8	MADDR[20]		H8	V_{SS}		M8	V_{CC} CORE		T8	PCIDEVSELN	
D9	MADDR[19]		H9	V_{SS}		M9	V_{CC} CORE		T9	PCIPAR	
D10	MADDR[15]		H10	V_{SS}		M10	V_{CC} I/0		T10	PCIAD[13]	
D11	EXTBCV		H11	V_{SS}		M11	V_{CC} DDR		T11	PCIAD[9]	
D12	JTAG_TRSTN		H12	V_{CC} CORE		M12	V_{CC} DDR		T12	PCIAD[6]	
D13	WAITACKN		H13	DDRDATA[15]		M13	DDRRASN		T13	PCIAD[2]	
D14	DDRDATA[2]		H14	DDRDATA[14]		M14	DDRBA[1]		T14	PCIAD[1]	
D15	DDRDATA[3]		H15	DDRDATA[12]		M15	DDRADDR[6]		T15	PCIGNTN[1]	
D16	DDRDATA[1]		H16	DDRDATA[13]		M16	DDRADDR[7]		T16	PCIGNTN[3]	

Table 20 RC32435 Pinout (Part 2 of 2)

RC32435 Alternate Signal Functions

Pin	GPIO	Alternate	Pin	GPIO	Alternate
A7	GPIO[7]	MADDR[25]	J3	GPIO[2]	U0RTSN
A8	GPIO[4]	MADDR[22]	L3	GPIO[8]	CPU
B8	GPIO[5]	MADDR[23]	M1	GPIO[12]	PCIGNTN[5]
C7	GPIO[6]	MADDR[24]	M3	GPIO[11]	PCIREQN[5]
H3	GPIO[0]	U0SOUT	M4	GPIO[9]	PCIREQN[4]
H4	GPIO[1]	U0SINP	P3	GPIO[10]	PCIGNTN[4]
J1	GPIO[3]	U0CTSN	T2	GPIO[13]	PCIMUINTN

Table 21 RC32435 Alternate Signal Functions

RC32435 Power Pins

V_{cc} I/O	V_{cc} DDR	V_{cc} Core	V_{cc} PLL	V_{cc} APLL
E5	E11	E8	B11	C12
E6	E12	E9		
E7	F12	F9		
E10	G12	H5		
F5	K12	H6		
G5	L12	H12		
K5	M11	J5		
K6	M12	J11		
L5		J12		
M5		L8		
M6		M8		
M7		M9		
M10				

Table 22 RC32435 Power Pins

Signal Name	I/O Type	Location	Signal Category
MADDR[0]	O	C15	Memory and Peripheral Bus
MADDR[1]	O	B16	
MADDR[2]	O	A16	
MADDR[3]	O	B15	
MADDR[4]	O	C14	
MADDR[5]	O	A15	
MADDR[6]	O	B14	
MADDR[7]	O	A14	
MADDR[8]	O	B13	
MADDR[9]	O	A13	
MADDR[10]	O	A5	
MADDR[11]	O	B5	
MADDR[12]	O	B10	
MADDR[13]	O	A10	
MADDR[14]	O	C10	
MADDR[15]	O	D10	
MADDR[16]	O	A9	
MADDR[17]	O	B9	
MADDR[18]	O	C9	
MADDR[19]	O	D9	
MADDR[20]	O	D8	
MADDR[21]	O	C8	
MDATA[0]	I/O	D7	
MDATA[1]	I/O	B6	
MDATA[2]	I/O	D6	
MDATA[3]	I/O	C5	
MDATA[4]	I/O	B7	
MDATA[5]	I/O	C6	
MDATA[6]	I/O	A6	
MDATA[7]	I/O	D5	

Table 24 RC32435 Alphabetical Signal List (Part 4 of 7)

Signal Name	I/O Type	Location	Signal Category
MIICL	I	D2	Ethernet Interface
MIICRS	I	D3	
MIIMDC	O	H2	
MIIMDIO	I/O	H1	
MIIRXCLK	I	F2	
MIIRXD[0]	I	D1	
MIIRXD[1]	I	D4	
MIIRXD[2]	I	E2	
MIIRXD[3]	I	E1	
MIIRXDV	I	G1	
MIIRXER	I	G3	
MIITXCLK	I	G4	
MIITXD[0]	O	E3	
MIITXD[1]	O	E4	
MIITXD[2]	O	F1	
MIITXD[3]	O	F3	
MIITXENP	O	F4	
MIITXER	O	G2	
OEN	O	A2	Memory and Peripheral Bus
PCIAD[0]	I/O	R14	PCI Bus Interface
PCIAD[1]	I/O	T14	
PCIAD[2]	I/O	T13	
PCIAD[3]	I/O	R13	
PCIAD[4]	I/O	P13	
PCIAD[5]	I/O	R12	
PCIAD[6]	I/O	T12	
PCIAD[7]	I/O	P12	
PCIAD[8]	I/O	R11	
PCIAD[9]	I/O	T11	
PCIAD[10]	I/O	P11	
PCIAD[11]	I/O	N11	
PCIAD[12]	I/O	R10	
PCIAD[13]	I/O	T10	
PCIAD[14]	I/O	P10	
PCIAD[15]	I/O	N10	
PCIAD[16]	I/O	T5	

Table 24 RC32435 Alphabetical Signal List (Part 5 of 7)

Signal Name	I/O Type	Location	Signal Category
PCISTOPN	I/O	P8	PCI Bus Interface
PCITRDYN	I/O	R8	
RSTN	I/O	B2	System
RWN	O	A1	Memory and Peripheral Bus
SCK	I/O	K2	Serial Peripheral Interface
SCL	I/O	L2	I^2C
SDA	I/O	L1	
SDI	I/O	L4	Serial Peripheral Interface
SDO	I/O	K4	
Vcc APLL		C12	Power
Vcc Core		E8, E9, F9, H5, H6, H12, J5, J11, J12, L8, M8, M9	
Vcc DDR		E11, E12, F12, G12, K12, L12, M11, M12	
Vcc I/O		E5, E6, E7, E10, F5, G5, K5, K6, L5, M5, M6, M7, M10	
Vcc PLL		B11	
Vss		F6, F7, F8, F10, F11, G6, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J6, J7, J8, J9, J10, K7, K8, K9, K10, K11, L6, L7, L9, L10, L11	Ground
Vss APLL		B12	
Vss PLL		A11	
WAITACKN	I	D13	Memory and Peripheral Bus
WEN	O	C4	
Reserved		K3, L1, L2	

Table 24 RC32435 Alphabetical Signal List (Part 7 of 7)